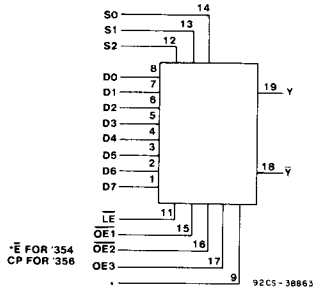
CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

File Number **1690**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

8-Input Multiplexer/Register, 3-State

CD54/74HC/HCT354 — Transparent Data & Select Latches
CD54/74HC/HCT356 — Edge-Triggered Data Flip-Flops
Transparent Select Latches

Type Features:

- *Buffered inputs*
- *3-State Complementary Outputs*
- *Bus Line Driving Capability*
- *Typical propagation delay: V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*
  Data to Output (354) = 18 ns
  Clock to Output (356) = 22 ns

The RCA-CD54/74HC/HCT354 and CD54/74HC/HCT356 are data selectors/multiplexers that select one of eight sources. In both the HC/HCT354 and HC/HCT356 the data select bits S0, S1, and S2 are stored in transparent latches that are enabled by a low latch enable input, $\overline{LE}$.

In the HC/HCT354 the data enable input, $\overline{E}$, controls transparent latches that pass data to the outputs when $\overline{E}$ is high and latches in new data when $\overline{E}$ is low.

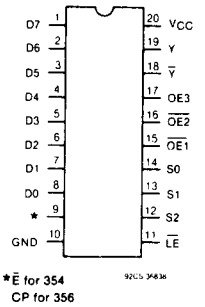
In the HC/HCT356 the data is stored in edge-triggered flip-flops that are triggered by a low-to-high clock transition.

In both types the three-state outputs are controlled by three output-enable inputs $\overline{OE1}$, $\overline{OE2}$, and OE3.

The CD54HC/HCT354/356 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT354/356 are supplied in 20-lead plastic dual-in-line plastic packages (E suffix). The CD54/74HC/HCT354/356 are also supplied in chip form (H suffix). The CD74HC/HCT354/356 are also available in plastic surface mounted packages (M suffix).

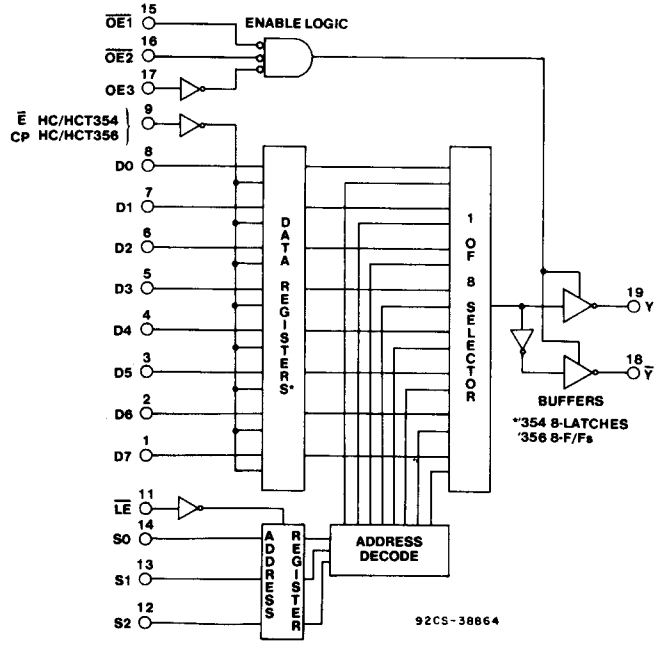
Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356



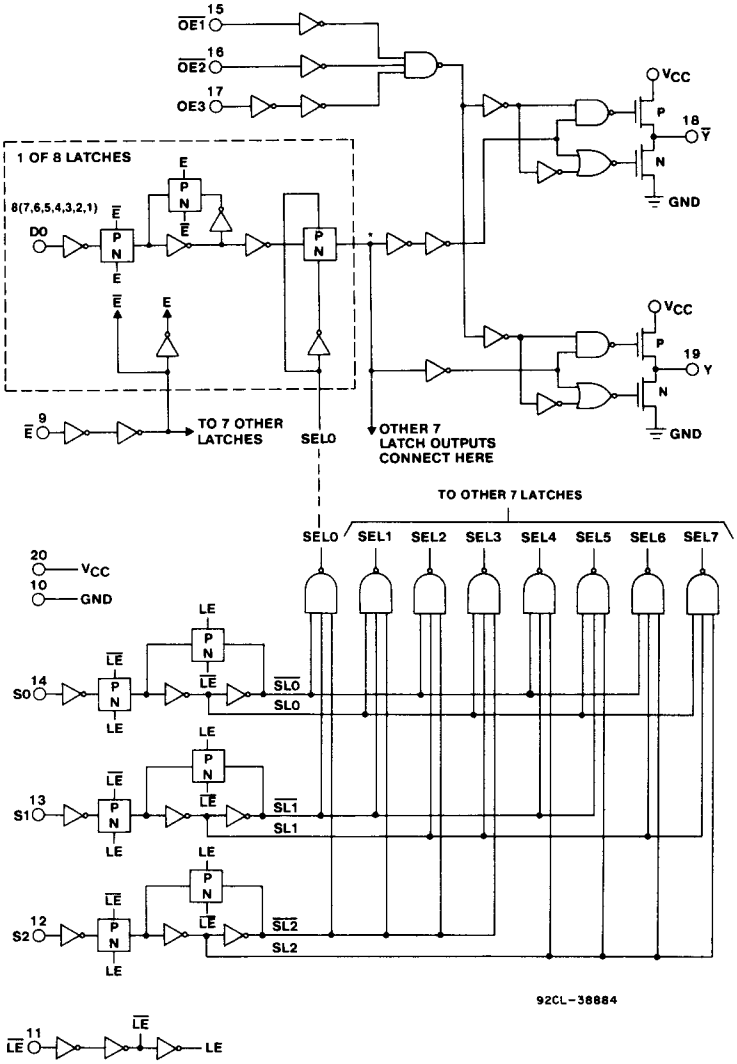
Block Diagram

TRUTH TABLE

Inputs								Outputs	
Select #			Enable Data 'HC354 'HCT354	Clock 'HC356 'HCT356	Output Enables				
S2	S1	S0	E	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	Y	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↗	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0_n}$	$D0_n$
L	L	H	L	↗	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1_n}$	$D1_n$
L	H	L	L	↗	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2_n}$	$D2_n$
L	H	H	L	↗	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3_n}$	$D3_n$
H	L	L	L	↗	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4_n}$	$D4_n$
H	L	H	L	↗	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5_n}$	$D5_n$
H	H	L	L	↗	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6_n}$	$D6_n$
H	H	H	L	↗	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7_n}$	$D7_n$

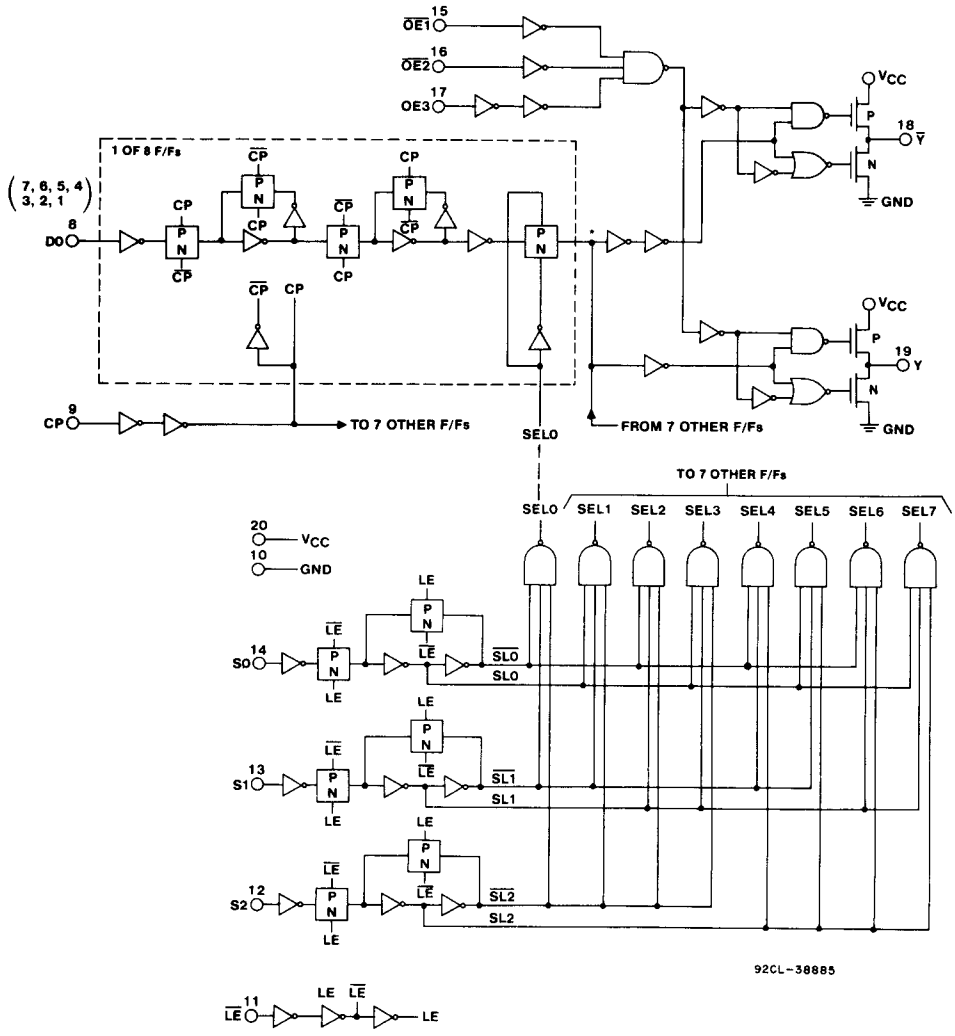
Notes
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↗ = transition from low to high level
D0 ... D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of HC356
$D0_n$ ... $D7_n$ = the level of steady state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock
This column shows the input address setup with $\overline{LE}$ low

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356



HC/HCT354 Logic Diagram

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356



HC/HCT356 Logic Diagram

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC})
(Voltages referenced to ground) ..... -0.5 to +7V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5V$) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_I < -0.5$ V OR $V_I > 0.5$ V $+V_{CC}$) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{V}$) ..... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) CD54/74HC Types CD54/74HCT Types	 2 4.5	 6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: CD74 Types CD54 Types	 -40 -55	 +85 +125	°C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	 0 0 0	 1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC354/356/CD54HC354/356										CD74HCT354/356/CD54HCT354/356										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—		V
			4.5	3.15	—	—	3.15	—	3.15	—											
			6	4.2	—	—	4.2	—	4.2	—											
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8		V
			4.5	—	—	1.35	—	1.35	—	1.35											
			6	—	—	1.8	—	1.8	—	1.8											
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V
		-7.8	6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1		V
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4		V
		7.8	6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160		μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490		μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10		μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

HCT354 Input Loading Table

Input	Unit Loads*
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE1}$, $\overline{OE2}$	0.80
OE3	0.25
$\overline{LE}$	0.25
$\overline{E}$	0.60

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

HCT356 Input Loading Table

Input	Unit Loads*
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE1}$, $\overline{OE2}$	0.80
OE3	0.25
$\overline{LE}$	0.25
CP	0.60

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns) — HC/HCT354

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay					
Dn → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	18	20	ns
$\overline{E}$ → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	21	23	ns
Sn → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	22	25	ns
$\overline{LE}$ → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	24	25	ns
Output Disabling Time	15	t_{PLZ}, t_{PHZ}	13	13, 16	ns
Output Enabling Time	15	t_{PZL}, t_{PZH}	12, 13	14	ns
Power Dissipation Capacitance*	—	C_{PD}	90	92	pF

*C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency,
C_L = output load capacitance.
V_{CC} = supply voltage

PREREQUISITE FOR SWITCHING FUNCTION — HC/HCT354

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{E}$ pulse width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{LE}$ pulse width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set Up Times															
Dn → $\overline{E}$	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Sn → $\overline{LE}$	t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Times															
Dn → $\overline{E}$	t_H	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	
Sn → $\overline{LE}$	t_H	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns) — HC/HCT354

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Dn → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	ns
		4.5	—	42	—	47	—	53	—	59	—	63	—	71	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
$\overline{E}$ → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	250	—	—	—	315	—	—	—	375	—	—	ns
		4.5	—	50	—	54	—	63	—	68	—	75	—	81	
		6	—	43	—	—	—	54	—	—	—	64	—	—	
Sn → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	260	—	—	—	325	—	—	—	390	—	—	ns
		4.5	—	52	—	59	—	65	—	74	—	78	—	89	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
$\overline{LE}$ → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
		4.5	—	58	—	63	—	73	—	79	—	87	—	94	
		6	—	49	—	—	—	62	—	—	—	74	—	—	
Output Disabling Time		2	—	155	—	—	—	195	—	—	—	235	—	—	ns
		4.5	—	31	—	33	—	39	—	41	—	47	—	50	
$\overline{OE}$n to Y, $\overline{Y}$	t_{PLZ}	6	—	26	—	—	—	33	—	—	—	40	—	—	
	t_{PHZ}	2	—	155	—	—	—	195	—	—	—	235	—	—	
OE3 to Y, $\overline{Y}$		4.5	—	31	—	39	—	39	—	49	—	47	—	59	
		6	—	26	—	—	—	33	—	—	—	40	—	—	
Output Enabling Time		2	—	150	—	—	—	190	—	—	—	225	—	—	ns
		4.5	—	30	—	34	—	38	—	43	—	45	—	51	
$\overline{OE}$n to Y, $\overline{Y}$	t_{PZL}	6	—	26	—	—	—	33	—	—	—	38	—	—	
	t_{PZH}	2	—	160	—	—	—	200	—	—	—	240	—	—	
OE3 to Y, $\overline{Y}$		4.5	—	32	—	34	—	40	—	43	—	48	—	51	
		6	—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition Time	t_{TLH} t_{THL}	**2**	—	**60**	—	—	—	**75**	—	—	—	**90**	—	—	**ns**
		4.5	—	**12**	—	**12**	—	**15**	—	**15**	—	**18**	—	**18**	
		6	—	**10**	—	—	—	**13**	—	—	—	**15**	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-state Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns) — HC/HCT356

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			54/74HC	54/74HCT	
Propagation Delay CP → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	22	22	ns
Sn → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	22	25	ns
$\overline{LE}$ → Y, $\overline{Y}$	15	t_{PLH}, t_{PHL}	24	25	ns
Output Disabling Time	15	t_{PLZ}, t_{PHZ}	13	13, 15	ns
Output Enabling Time	15	t_{PZL}, t_{PZH}	12, 13	14	ns
Power Dissipation Capacitance*	—	C_{PD}	51	52	pF

*C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356

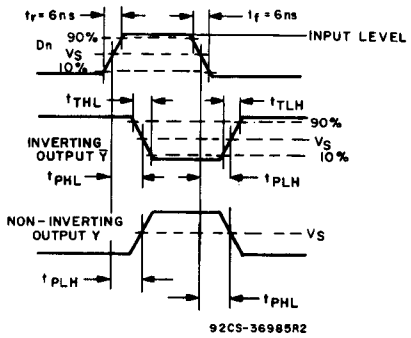
PREREQUISITE FOR SWITCHING FUNCTION — HC/HCT356

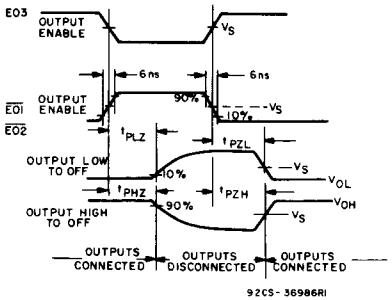
CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CP Pulse Width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{LE}$ Pulse Width	t_{PLH} t_{PHL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Set Up Times Dn → CP	t_{SU}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	7	—	5	—	9	—	5	—	11	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Sn → $\overline{LE}$	t_{su}	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
		4.5	5	—	7	—	5	—	9	—	5	—	11	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Hold Times Dn → CP	t_h	2	45	—	—	—	55	—	—	—	70	—	—	—	ns
		4.5	9	—	9	—	11	—	11	—	14	—	14	—	
		6	8	—	—	—	9	—	—	—	12	—	—	—	
Sn → $\overline{LE}$	t_h	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns) — HC/HCT356

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay: CP → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	255	—	—	—	320	—	—	—	385	—	—	ns
		4.5	—	51	—	51	—	64	—	64	—	77	—	77	
		6	—	43	—	—	—	54	—	—	—	65	—	—	
Sn → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	260	—	—	—	325	—	—	—	390	—	—	ns
		4.5	—	52	—	59	—	65	—	74	—	78	—	89	
		6	—	44	—	—	—	55	—	—	—	66	—	—	
$\overline{LE}$ → Y, $\overline{Y}$	t_{PLH} t_{PHL}	2	—	290	—	—	—	365	—	—	—	435	—	—	ns
		4.5	—	58	—	63	—	73	—	79	—	87	—	94	
		6	—	49	—	—	—	62	—	—	—	74	—	—	
Output Disabling Time	t_{PLZ} t_{PHZ}	2	—	155	—	—	—	195	—	—	—	235	—	—	ns
$\overline{OE1}$, $\overline{OE2}$ to Y, $\overline{Y}$			—	31	—	33	—	39	—	41	—	47	—	50	
OE3 to Y, $\overline{Y}$		4.5	—	26	—	—	—	33	—	—	—	40	—	—	
		6	—	155	—	—	—	195	—	—	—	235	—	—	
			—	31	—	37	—	39	—	46	—	47	—	56	
			—	26	—	—	—	33	—	—	—	40	—	—	
Output Enabling Time	t_{PZL} t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
$\overline{OE1}$, $\overline{OE2}$ to Y, $\overline{Y}$			—	30	—	34	—	38	—	43	—	45	—	51	
OE3 to Y, $\overline{Y}$		4.5	—	26	—	—	—	33	—	—	—	38	—	—	
		6	—	160	—	—	—	200	—	—	—	240	—	—	
			—	32	—	34	—	40	—	43	—	48	—	51	
			—	27	—	—	—	34	—	—	—	41	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-state Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC354, CD54/74HCT354
CD54/74HC356, CD54/74HCT356





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 1 — Transition times and propagation delay times.

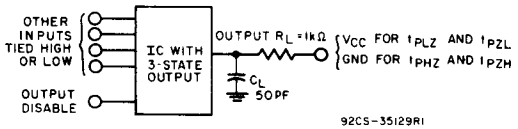


Fig. 2 — Three-state propagation delay test circuit.