

For more information, please visit: http://hero.terasic.com

Hero Connector Layout











For any technical questions, please e-mail us at Email: support@terasic.com

B oot test

Please perform the boot test in the following order. Make sure the FPGA board power-on procedure is done before the CPU board is turn on.





- 3 Connect the 12V DC power supply
- Power on the FPGA board (rear switch)
- 5 Turn on the power of the CPU board (front switch)
- 6 Set up the Linux Desktop on the display monitor
 - (Username: robot Password: intel123)

| 67108864 3088 | | | 22 3887 58 | |
|----------------|-------------|---------|------------------------|--|
| 134217728 311 | | | | |
| 268435456 310 | | | | |
| Deading 26714 | t kBr ut+h | black | size (in bytes) below: | |
| Reducing roris | T NDS HECH | DIOCK | size (in bytes) betow. | |
| Block Size Av |) Max | Min | End-End (MB/s) | |
| 524288 1910 | 68 2352.4 | 2 711.0 | 3 1820.29 | |
| 1048576 1887 | 27 2074.0 | 1 1378. | 67 1817.74 | |
| 2097152 2289 | .52 2460.00 | 8 1962. | 77 2252.79 | |
| 4194304 3057 | | | | |
| 8388608 3093 | 06 3199.8 | 7 2731 | 07 3086.55 | |
| 16777216 3083 | | | | |
| 33554432 3075 | 25 3210.5 | 6 2922. | 92 3073 75 | |
| 67108864 3036 | | | | |
| 134217728 323 | | | | |
| 268435456 328 | | | | |
| 200433450 320 | | | | |
| Write top spe | d = 3221. | 57 MB/s | | |
| Read top speed | | | | |
| Throughput - | | | | |
| | | | | |
| DIAGNOSTIC_PA | SED | | | |
| robot@hero:-/ | | | | |

- Perform FPGA OpenCL DDR4 read and write tests:
 - a. Open Linux Terminal
 - b. Execute "cd ~/data"
 - c. Execute "source altera_rte.sh"
 - d. Execute "aocl diagnose all"
 - Cobserve the DDR4 test results, as shown on the left

D esign Resource Download Link

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