TPS23750 Buck-Converter Evaluation Board – HPA107

This user's guide describes the function and operation of the HPA107 evaluation module (EVM). A complete description, schematic, bill of materials, assembly drawing, and printed-circuit board artwork are included.

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1 Introduction

The HPA107 evaluation module implements an IEEE 802.3af-compliant class-3 power interface and a non-isolated DC/DC switching converter using the Texas Instruments TPS23750 powered device (PD) controller in a typical power-over-Ethernet (PoE) configuration. The DC/DC converter is a 5-V output buck converter with a BOM option for 3.3 V. A small prototype area is included on the printed-circuit board. The EVM accepts a TPS23770 in place of the TPS23750 to support a PD with a legacy undervoltage lockout (UVLO) threshold.

The EVM has separate LEDs that show when the DC/DC converter and the PoE interface are active. Test points are provided at all critical nodes. Power to the EVM is provided over the spare or data lines in an Ethernet cable or by an auxiliary source like a wall adapter.

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2 Specification, Schematic, and Bill of Materials

2.1 Electrical Specification

Table 1 shows the electrical specification over a –40°C to 85°C operating temperature range. Input voltages are measured at the RJ-45 connector unless otherwise noted.

Table 1. HPA107 Electrical Specification

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
POWER INTERFACE						
Input voltage, V_{IN}	Applied to the power pins of connectors J1 or J3		0	–	57	V
Operating voltage	After startup		36	–	57	V
Input UVLO	Rising input voltage		–	–	42	V
	Falling input voltage		30	–	–	
Detection voltage range			2.7	–	10.1	V
Classification voltage range			14.5	–	20.5	V
Classification current			26	–	30	mA
Inrush current limit			100	–	180	mA
Operating current limit			405	–	495	mA
DC/DC CONVERTER						
Output voltage	36 V ≤ V_{IN} ≤ 57 V, I_{LOAD} ≤ I_{LOAD} (max)	3.3-V output	3.13	3.3	3.47	V
		5-V output	4.75	5.0	5.25	
Output current, I_{LOAD}	36 V ≤ V_{IN} ≤ 57 V	3.3-V output	–	–	2.5	A
		5-V output	–	–	2	
Output ripple voltage, peak-to-peak	V_{IN} = 44 V, I_{LOAD} = 2.5 A	3.3-V output	–	30	–	mV
	V_{IN} = 44 V, I_{LOAD} = 2 A	5-V output	–	32	–	
Efficiency, end-to-end	V_{IN} = 44 V, I_{LOAD} = 2.5 A	3.3-V output	–	75%	–	
	V_{IN} = 44 V, I_{LOAD} = 2 A	5-V output	–	80%	–	
Switching frequency			164	–	236	kHz

The end-to-end efficiency curves in Figure 1 and Figure 3 include the losses at the PD switch, bridge diode, and data transformer. The DC/DC converter efficiency curves in Figure 2 and Figure 4 exclude these losses. The curves are plotted for the RJ-45 connector voltages shown.

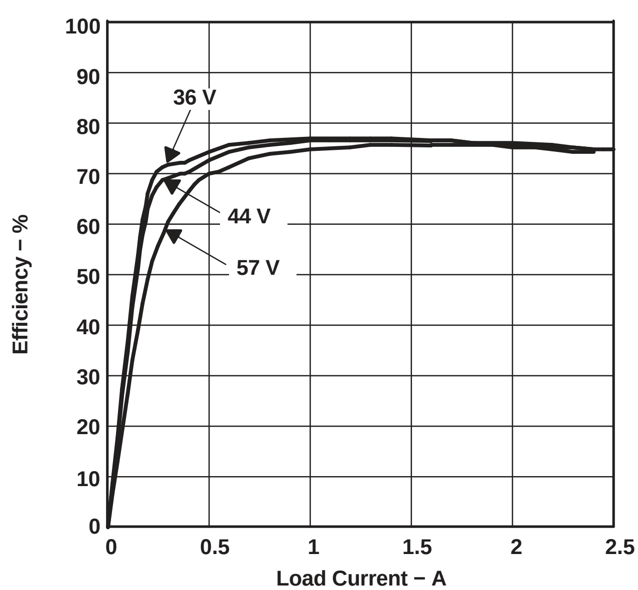

Figure 1. Typical 3.3-V PD End-to-End Efficiency

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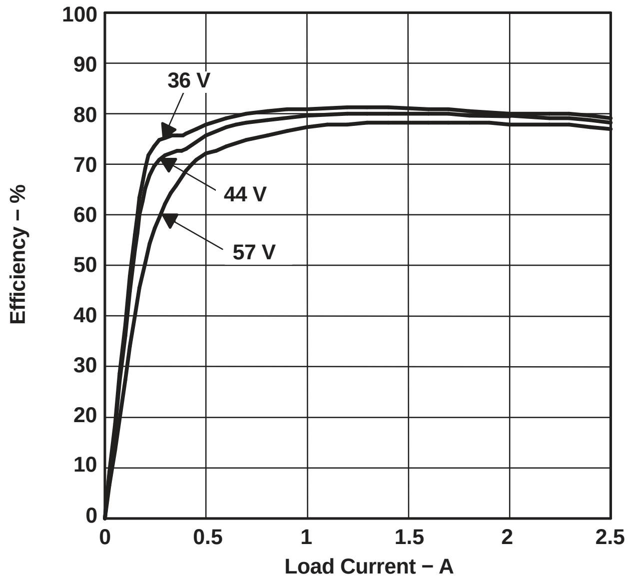

Figure 2. Typical 3.3-V DC/DC Converter Efficiency

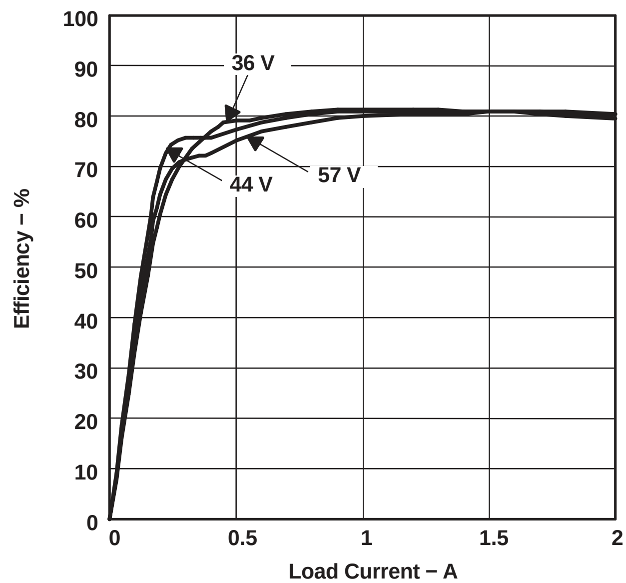

Figure 3. Typical 5-V PD End-to-End Efficiency

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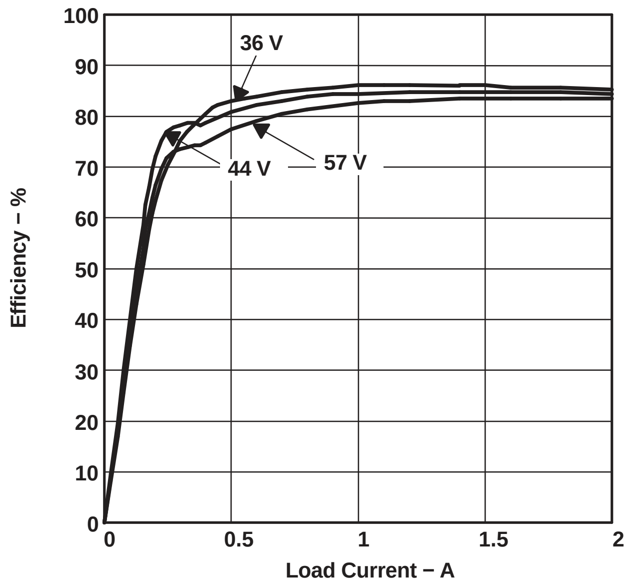

Figure 4. Typical 5-V DC/DC Converter Efficiency

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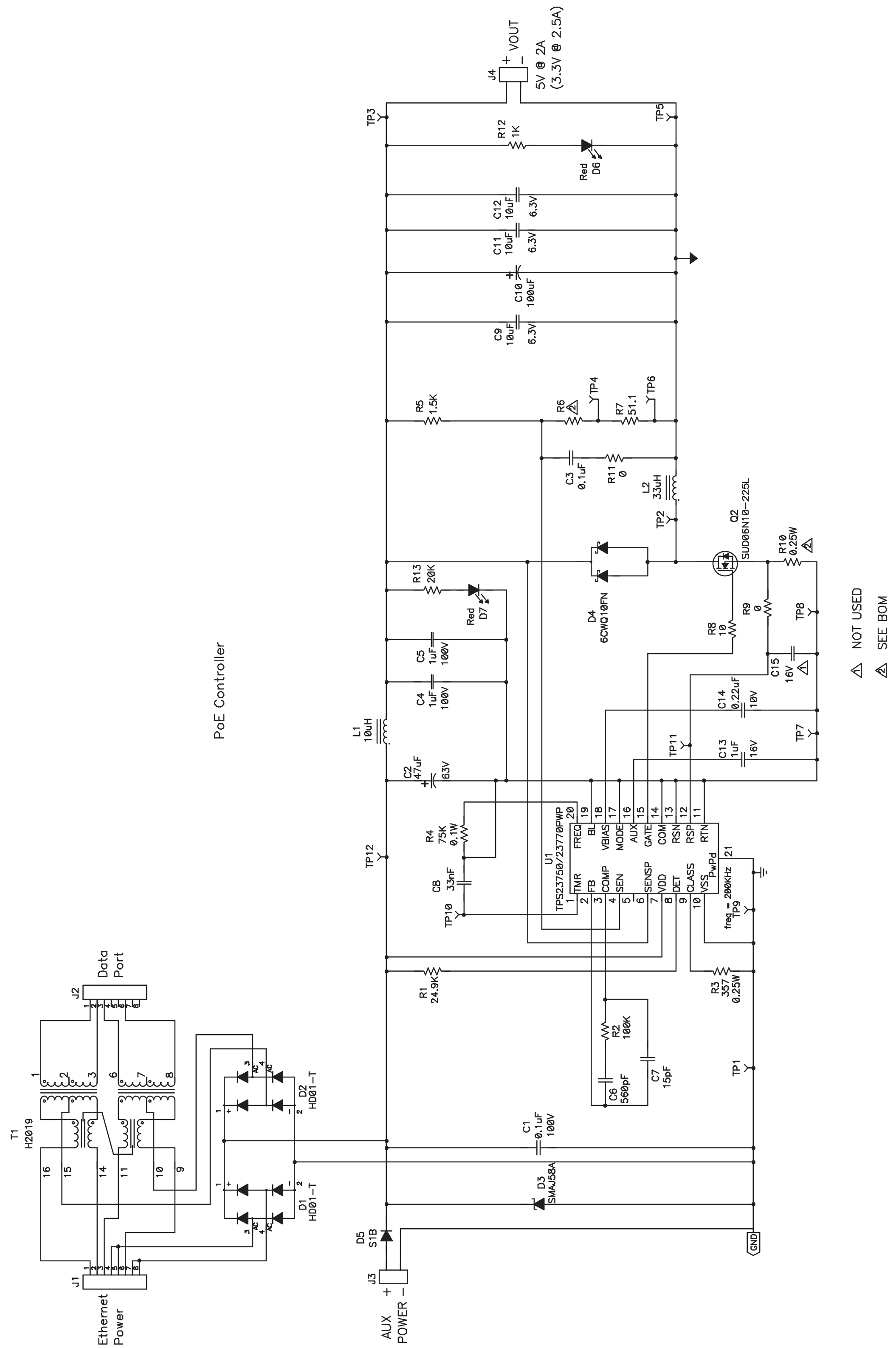
2.2 Schematic



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2.3 Bill of Material

Table 2. HPA107 Bill of Materials

–001 3.3 V Count	–002 5 V Count	Ref Des	Description	Size	MFR	Part No.
1	1	C1	Capacitor, Ceramic, 0.1 μF, 100 V, X7R, 10%	1206	Vishay	Std
1	1	C10	Capacitor, Aluminum, 100 μF, 6.3-V, 20%	6.3 × 5.8	Panasonic	EEVFK0J101P
1	1	C13	Capacitor, Ceramic, 1 μF, 16-V, X7R, 10%	805	Murata	GRM21BR71C105KA01L
1	1	C14	Capacitor, Ceramic, 0.22 μF, 10V, X7R, 10%	805	Std	Std
1	1	C8	Capacitor, Ceramic, 33 nF, 25V, X7R, 10%	603	Std	Std
1	1	C2	Capacitor, Aluminum, 47 μF, 63V, 20%	8×10 mm	Panasonic	EEVFK1J470P
1	1	C3	Capacitor, Ceramic, X7R, 0.1 μF, 25V, 10%	603	Vishay	Std
0	0	C15	Not used	603		
2	2	C4, C5	Capacitor, Ceramic, 1 μF, 100 V, X7R, 10%	1210	Murata	GRM32ER72A105KA01L
1	1	C6	Capacitor, Ceramic, 560 pF, 50 V, X7R, 10%	603	Std	Std
1	1	C7	Capacitor, Ceramic, 15 pF, 50 V, C0G, 5%	603	Std	Std
3	3	C9, C11, C12	Capacitor, Ceramic, 10 μF, 6.3V, X5R, 10%	805	Murata	GRM21BR60J106KE19L
2	2	D1, D2	Bridge Rectifier, 100V, 0.8A, Glass Passivated, SMD	MINI DIP4	Diodes Inc	HD01-T
2	2	D6, D7	Diode, LED, Red	0.114 × 0.049	Panasonic	LN1271R
1	1	D3	Diode, TVS, 58V, 1W	SMA	Diodes Inc., STMicro	SMAJ58A
1	1	D4	Diode, Dual Schottky, 7-A, 100-V	DPAK	IR	6CWQ10FN
1	1	D5	Diode, Rectifier, 1A, 100V	SMA	Diodes Inc.	S1B
2	2	J1, J2	Connector, Jack, Modular, 8 POS	TH	AMP	520252
2	2	J3, J4	Terminal Block, 2-pin, 6-A, 3,5 mm	TH	OST	ED1514
1	1	L1	Inductor, SMT, 10 μH, 1.1A, 160 mΩ	4.45×6.6 mm	Coilcraft	DO1608C-103
					Wurth Electronics	7445510
1	1	L2	Inductor, SMT, 33 μH, 3.9A, 41 mΩ	0.472 sq	Sumida	CDRH127/LD-330
1	1	Q2	MOSFET, N-ch, 100V, 3.75A, 0.25 Ω	DPAK	Vishay	SUD06N10-225L
1	1	R1	Resistor, Chip, 24.9 kΩ, 1/16W, 1%	603	Std	Std
0	1	R10	Resistor, Chip, 0.18 Ω, 1/4W, 1%	1206	Vishay, Susuma	WSL1206R1800FEA18,
						RL1632R-R180-F
1	0	R10	Resistor, Chip, 0.15 Ω, 1/4W, 1%	1206	Vishay	WSL1206R1500FEA18
1	1	R2	Resistor, Chip, 100 kΩ, 1/16W, 1%	603	Std	Std
1	1	R12	Resistor, Chip, 1 kΩ, 1/10-W, 5%	805	Std	Std
1	1	R13	Resistor, Chip, 20 kΩ, 1/10-W, 5%	805	Std	Std
1	1	R3	Resistor, Chip, 357 Ω, 1/4-W	1206	Std	Std
1	1	R4	Resistor, Chip, 75 kΩ, 1/16-W, 1%	603	Std	Std
1	1	R5	Resistor, Chip, 1.5 kΩ, 1/16W, 1%	603	Std	Std
0	1	R6	Resistor, Chip, 3.48 kΩ, 1/16W, 1%	603	Std	Std
1	0	R6	Resistor, Chip, 1.78 kΩ, 1/16W, 1%	603	Std	Std
1	1	R7	Resistor, Chip, 51.1 Ω, 1/16W, 1%	603	Std	Std
1	1	R8	Resistor, Chip, 10 Ω, 1/16W, 1%	603	Std	Std
2	2	R9, R11	Resistor, Chip, 0 Ω, 1/16W, 1%	603	Std	Std
1	1	T1	Xfmr, Center-tapped, Voice Over IP	0.500 × 0.370	Pulse	H2019
					Wurth Electronics	749013011
5	5	TP1, TP5 TP7–TP9	Test Point, Black	0.038	Keystone	5001
7	7	TP2–TP4, TP6, TP10–TP12	Test Point, Red	0.038	Keystone	5000
1	1	U1	IC, IEEE 802.3af Integrated Primary Side Controller	PWP20	TI	TPS23750PWP
1	1	–	PCB, 2.250 In × 4.350 In × 0.062 In	–	Any	HPA107A

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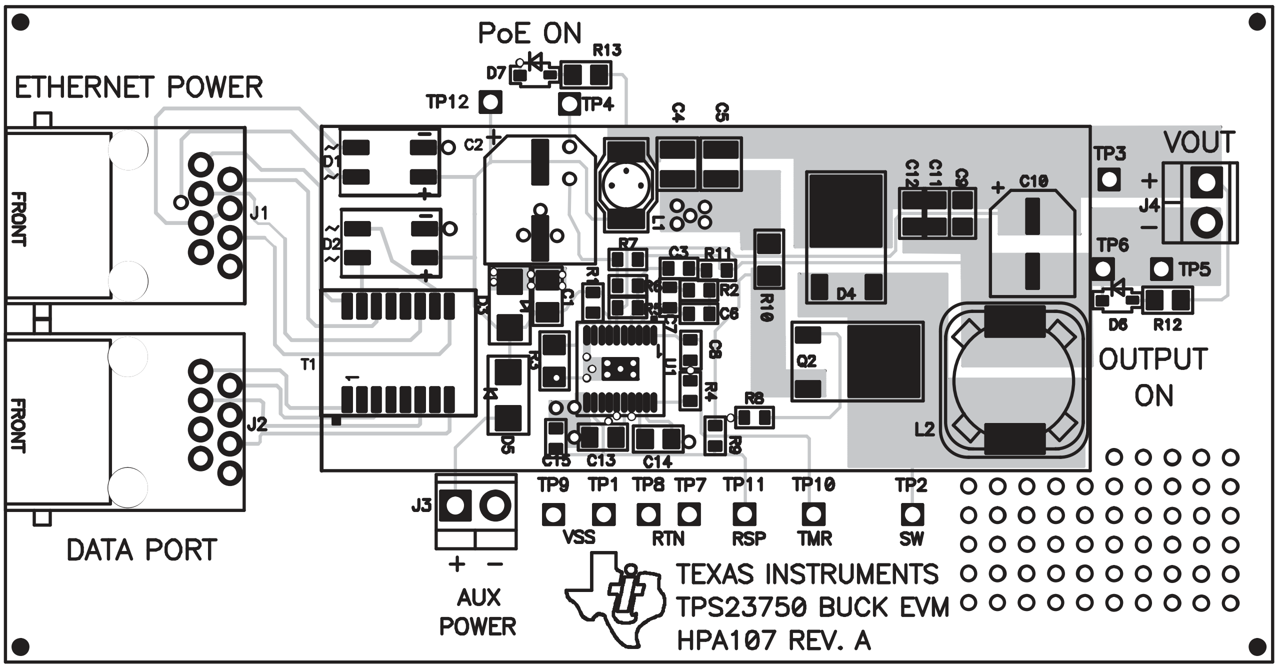
Table 2. HPA107 Bill of Materials (continued)

–001	–002	Ref Des	Description	Size	MFR	Part No.
3.3 V Count	5 V Count					
4	4	–	Rubber Bumper	–	SPC TECH	2566

3 Board Layout

3.1 Top-Side Layout



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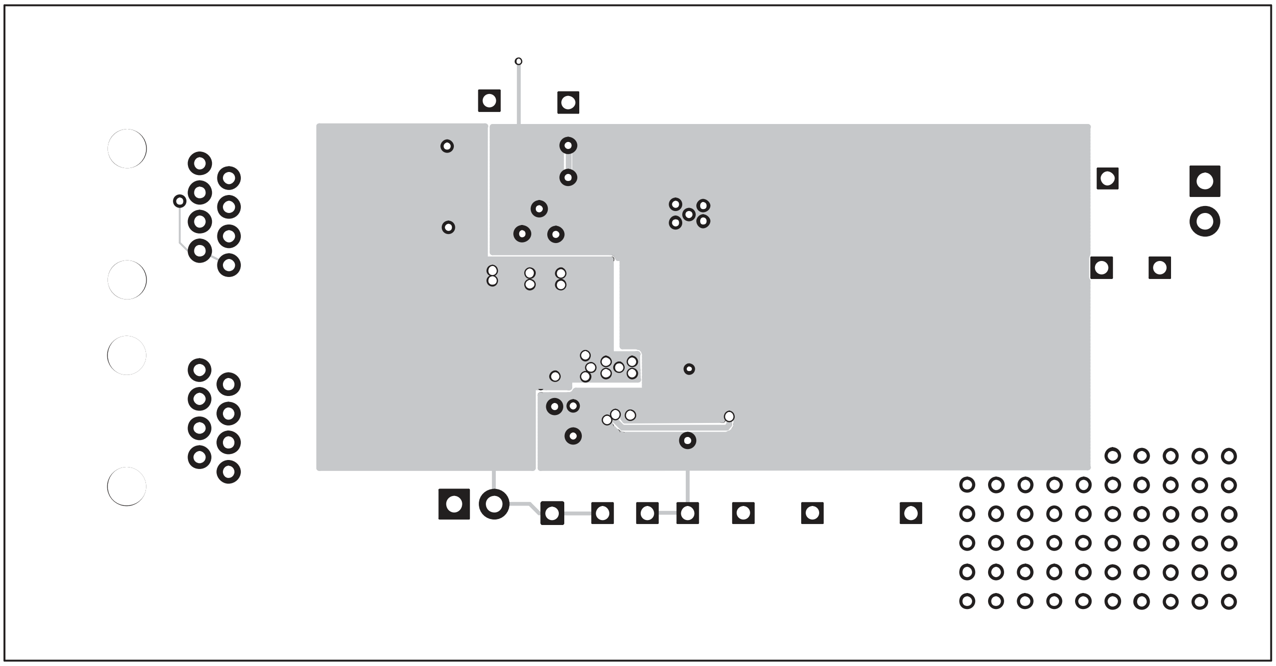
3.2 Bottom-Side Layout



3.3 Layout Considerations

The layout of the PoE front end must use good practice for power and EMI/ESD. A basic set of recommendations include:

- The parts placement must be driven by the power flow in a point-to-point manner such as RJ-45 → Ethernet transformer → diode bridges → TVS and 0.1-μF capacitor → TPS23750 → bulk capacitor → converter input.
- There should not be any crossovers of signals from one part of the flow to another.
- All leads should be as short as possible with wide power traces and paired signal and return.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS23750 should be located over split, local ground planes referenced to V_{SS} for the PoE input and to RTN for the converter operation. Whereas the PoE side may operate without a ground plane, the converter side must have one. The PowerPad™ must be tied to the V_{SS} plane or fill area, especially if power dissipation is a concern. Logic ground and power layers should not be present under the Ethernet input or the converter primary side.
- Large copper fills and *traces* should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.

Converter layout benefits from basic rules such as:

1. Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses which include the power semiconductors and magnetics.
2. Reduce the length of all the traces in step 1.
3. Where possible, use vertical pairing.
4. Use the *ground plane* for the switching currents carefully.
5. Keep the high-current and high-voltage switching away from low-level sensing circuits including those outside the power supply.
6. The current sensing on RSP/RSN is the most critical, noise-sensitive signal. It must be protected as in step 5, including exposure to the gate drive sign.
7. Pay special attention to spacing around the high-voltage sections of the converter.

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4 Using the EVM

4.1 Setup

Figure 5 shows a typical EVM setup. The user is encouraged to read the TPS23750 data sheet before using the EVM.

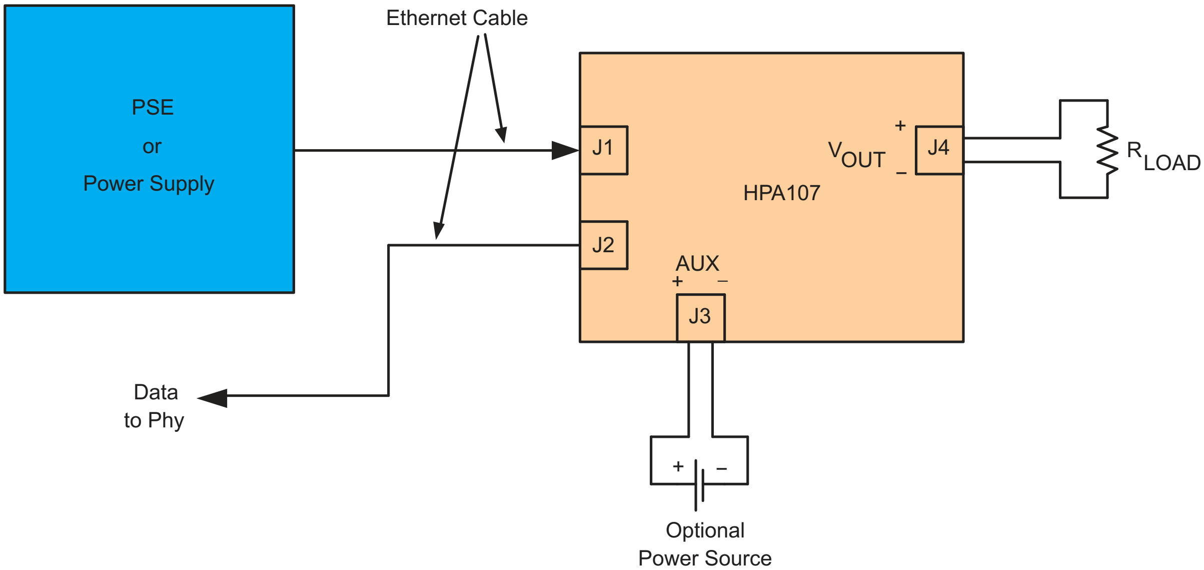

Figure 5. Typical Setup

4.2 Interface

Table 2 describes the EVM interface.

Table 3. EVM I/O Interfaces

Reference Designator	Description
J1	An Ethernet cable connects this port to the power-sourcing equipment (PSE). This port carries both data and power.
J2	This port carries only data. Do not apply power to this port.
J3	This terminal block accepts auxiliary power from a source like a wall adapter.
J4	Output voltage
D6	This LED is lit if the DC/DC converter output is on.
D7	This LED is lit if the PD FET switch is on.

4.3 Making Measurements

Stray magnetic fields from inductor L2 can couple noise into measurements. This noise may be noticeable when measuring a low-level signal like output ripple voltage. Keep the ground lead of the oscilloscope probe short and away from L2 to reduce the amount of noise pick-up.

Ground loops can be created if test equipment is connected to the EVM. Avoid ground loops by floating the test equipment and/or the power supply to the EVM.

4.4 EVM Operation

The TPS23750 data sheet describes the electrical operation and function of the various components in the buck converter powered device. The circuit provided in the data sheet is similar to the circuit in this EVM.

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5 Related Documentation

1. *TPS23750, TPS23770, Integrated 100 V IEEE 802.3af PD and DC/DC Controller* data sheet (SLVS590)
2. *IEEE Std 802.3af*

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It is important to operate this EVM within the input voltage range of 0 V to 57 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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