2-Phase Stepper-Motor Driver **TLE4726G**

AEC Qualified RoHS

Bipolar IC

Overview

Features

- 2× 0.75 A / 50 V outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Low standby-current drain
- Full, half, quarter, mini step

PG-DSO-24-13

Type	Ordering Code	Package
TLE4726G	On Request	PG-DSO-24-13

Description

TLE4726G is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate on constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 0.75 A per phase at operating voltages up to 50 V.

The direction and value of current are programmed for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in a full-bridge configuration have integrated, fast free-wheeling diodes and are free of crossover current. The logic is supplied either separately with 5 V or taken from the motor supply voltage by way of a series resistor and an integrated Z-diode. The device can be driven directly by a microprocessor with the possibility of all modes from full step through half step to mini step.

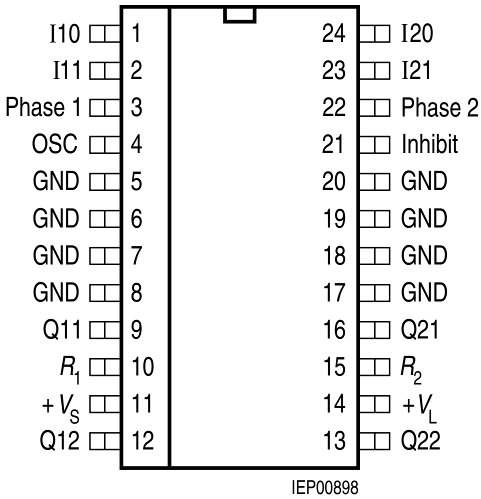


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Function
1, 2, 23, 24	**Digital control inputs IX0, IX1** for the magnitude of the **current** of the particular phase. <table><tr><th>IX1</th><th>IX0</th><th>Phase Current</th><th>Example of Motor Status</th><th></th></tr><tr><td>H</td><td>H</td><td>0</td><td>No current</td><td></td></tr><tr><td>H</td><td>L</td><td>1/3 I_{max}</td><td>Hold</td><td rowspan="3">typical I_{max} with R_{sense} = 1 Ω: 750 mA</td></tr><tr><td>L</td><td>H</td><td>2/3 I_{max}</td><td>Set</td></tr><tr><td>L</td><td>L</td><td>I_{max}</td><td>Accelerate</td></tr></table>
3	**Input Phase 1**; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.
5, 6, 7, 8, 17, 18, 19, 20	**Ground**; all pins are connected internally.
4	**Oscillator**; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.
10	**Resistor** R_1 for sensing the current in phase 1.
9, 12	**Push-pull outputs Q11, Q12** for phase 1 with integrated free-wheeling diodes.
11	**Supply voltage**; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 10 µF in parallel with a ceramic capacitor of 220 nF.
14	**Logic supply voltage**; either supply with 5 V or connect to + V_S across a series resistor. A Z-diode of approx. 7 V is integrated. In both cases block to ground directly on the IC with a stable electrolytic capacitor of 10 µF in parallel with a ceramic capacitor of 100 nF.
13, 16	**Push-pull outputs Q22, Q21** for phase 2 with integrated free-wheeling diodes.
15	**Resistor** R_2 for sensing the current in phase 2.
21	**Inhibit input**; the IC can be put on standby by low potential on this pin. This reduces the current consumption substantially.
22	**Input phase 2**; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.

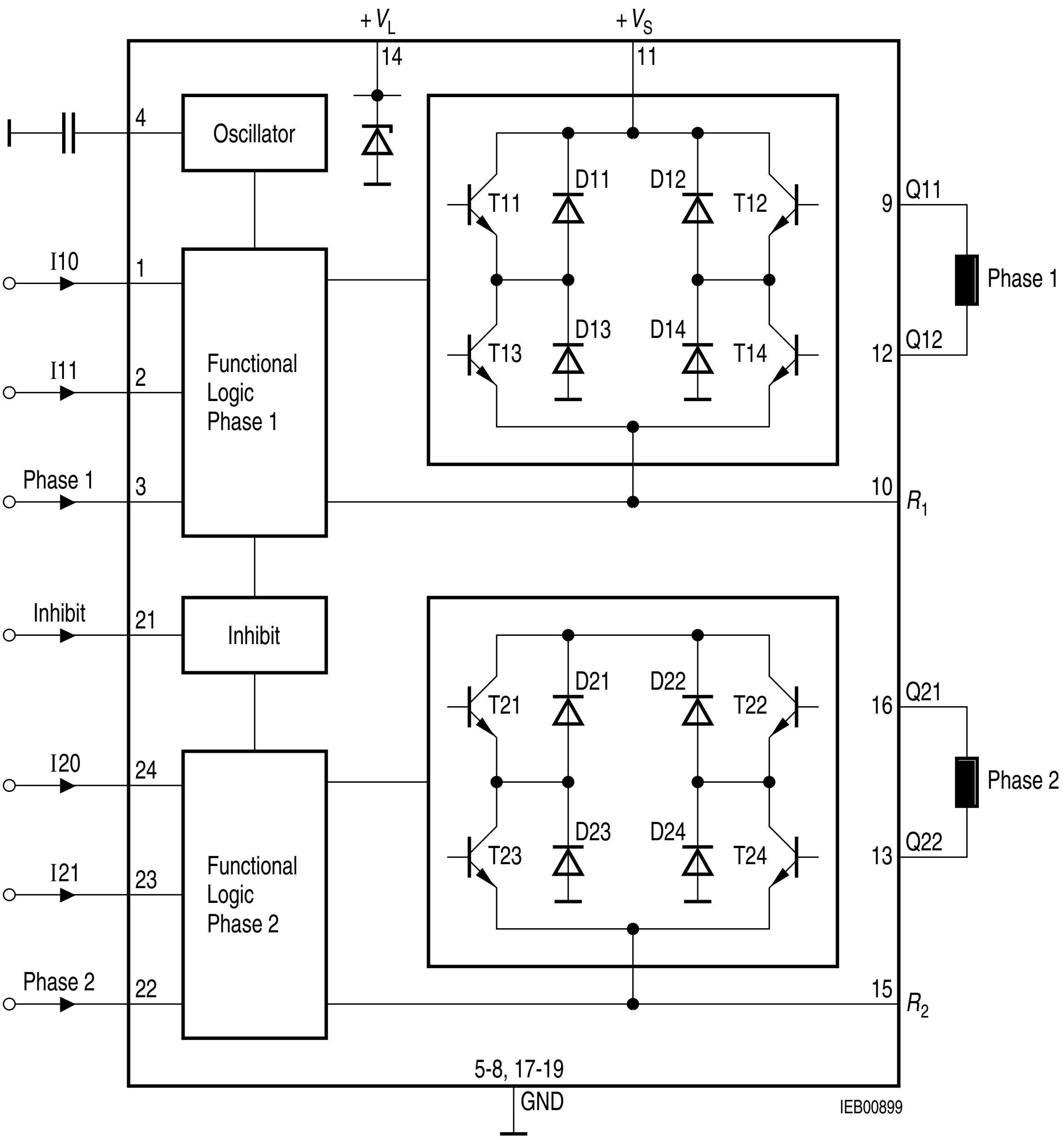


Figure 2 Block Diagram

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	0	52	V	–
Logic supply voltage	V_L	0	6.5	V	Z-diode
Z-current of V_L	I_L	–	50	mA	–
Output current	I_Q	– 1	1	A	–
Ground current	I_{GND}	– 2	2	A	–
Logic inputs	V_{Ixx}	– 6	V_L + 0.3	V	I_{XX} ; Phase 1, 2; Inhibit
R_1, R_2, oscillator input voltage	$V_{RX,}$ V_{OSC}	– 0.3	V_L + 0.3	V	–
Junction temperature	T_j T_j	– –	125 150	°C °C	– max. 10,000 h
Storage temperature	T_{stg}	– 50	125	°C	–

***Note:** Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	5	50	V	–
Logic supply voltage	V_L	4.5	6.5	V	without series resistor
Case temperature	T_C	– 25	110	°C	measured on pin 5 P_{diss} = 2 W
Output current	I_Q	– 800	800	mA	–
Logic inputs	V_{IXX}	– 5	V_L	V	I_{XX}; Phase 1, 2; Inhibit

Thermal Resistances

Parameter	Symbol	min.	max.	Unit	Remarks
Junction ambient	$R_{th\ ja}$	–	75	K/W	PG-DSO-24-13
Junction ambient (soldered on a 35 µm thick 20 cm² PC boar copper area)	$R_{th\ ja}$	–	50	K/W	PG-DSO-24-13
Junction case	$R_{th\ jc}$	–	15	K/W	measured on pin 5 PG-DSO-24-13

Note: In the operating range, the functions given in the circuit description are fulfilled.

Characteristics

V_S = 40 V; V_L = 5 V; – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
from + V_S	I_S	–	0.2	0.5	mA	V_{inh} = L
from + V_S	I_S	–	16	20	mA	V_{inh} = H, $I_{Q1/2}$ = 0, $I_{XX\ =\ L}$
from + V_L	I_L	–	1.7	3	mA	V_{inh} = L
from + V_L	I_L	–	18	25	mA	V_{inh} = H, $I_{Q1/2}$ = 0, $I_{XX\ =\ L}$

Characteristics (cont'd)
V_S = 40 V; V_L = 5 V; – 25 °C ≤ T_j ≤ 125 °C

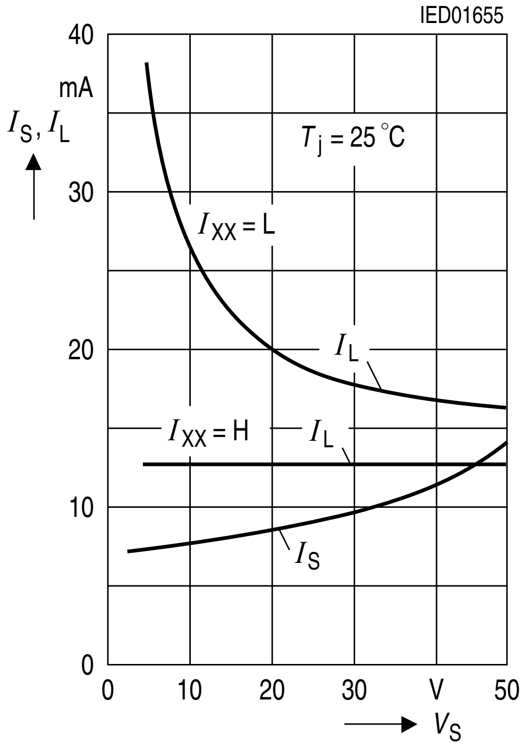
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator						
Output charging current	I_{OSC}	–	110	–	µA	–
Charging threshold	V_{OSCL}	–	1.3	–	V	–
Discharging threshold	V_{OSCH}	–	2.3	–	V	–
Frequency	f_{OSC}	18	25	40	kHz	C_{OSC} = 2.2 nF
Phase Current Selection Current Limit Threshold						
No current	$V_{sense\ n}$	–	0	–	mV	IX0 = H; IX1 = H
Hold	$V_{sense\ h}$	200	250	300	mV	IX0 = L; IX1 = H
Setpoint	$V_{sense\ s}$	420	540	680	mV	IX0 = H; IX1 = L
Accelerate	$V_{sense\ a}$	700	825	950	mV	IX0 = L; IX1 = L
Logic Inputs (I_{X1} ; I_{X0} ; Phase x)						
Threshold	V_I	1.4 (H→L)	–	2.3 (L→H)	V	–
L-input current	I_{IL}	– 10	–	–	µA	V_I = 1.4 V
L-input current	I_{IL}	– 100	–	–	µA	V_I = 0 V
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
Standby Cutout (inhibit)						
Threshold	V_{Inh} (L→H)	2	3	4	V	–
Threshold	V_{Inh} (H→L)	1.7	2.3	2.9	V	–
Hysteresis	V_{Inhhy}	0.3	0.7	1.1	V	–
Internal Z-Diode						
Z-voltage	V_{LZ}	6.5	7.4	8.2	V	I_L = 50 mA

Characteristics (cont'd)
V_S = 40 V; V_L = 5 V; – 25 °C ≤ T_j ≤ 125 °C

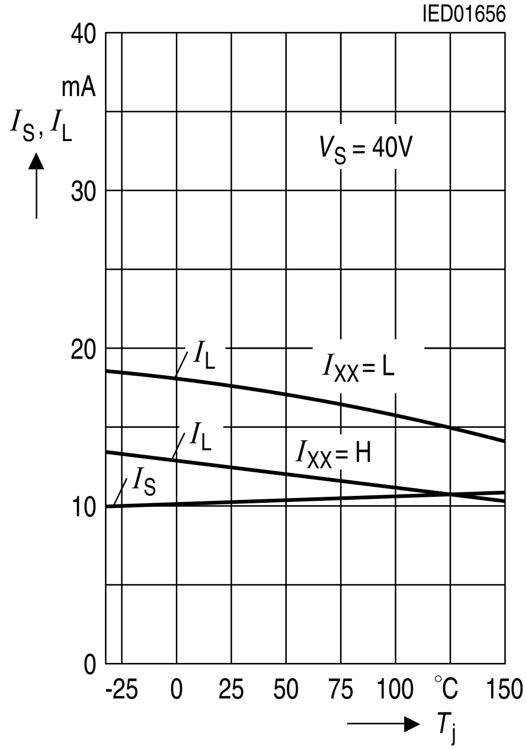
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Outputs						
Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satl}	–	0.3	0.6	V	I_Q = – 0.5 A
Saturation voltage	V_{satl}	–	0.5	1	V	I_Q = – 0.75 A
Reverse current	I_{Rl}	–	–	300	µA	V_Q = 40 V
Forward voltage	V_{Fl}	–	0.9	1.3	V	I_Q = 0.5 A
Forward voltage	V_{Fl}	–	1	1.4	V	I_Q = 0.75 A
Diode Transistor Source Pair (D11, T11; D12, T12; D21, T21; D22, T22)						
Saturation voltage	V_{satuC}	–	0.9	1.2	V	I_Q = 0.5 A; charge
Saturation voltage	V_{satuD}	–	0.3	0.7	V	I_Q = 0.5 A; discharge
Saturation voltage	V_{satuC}	–	1.1	1.4	V	I_Q = 0.75 A; charge
Saturation voltage	V_{satuD}	–	0.5	1	V	I_Q = 0.75 A; discharge
Reverse current	I_{Ru}	–	–	300	µA	V_Q = 0 V
Forward voltage	V_{Fu}	–	1	1.3	V	I_Q = – 0.5 A
Forward voltage	V_{Fu}	–	1.1	1.4	V	I_Q = – 0.75 A
Diode leakage current	I_{SL}	–	1	2	mA	I_F = – 0.75 A

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

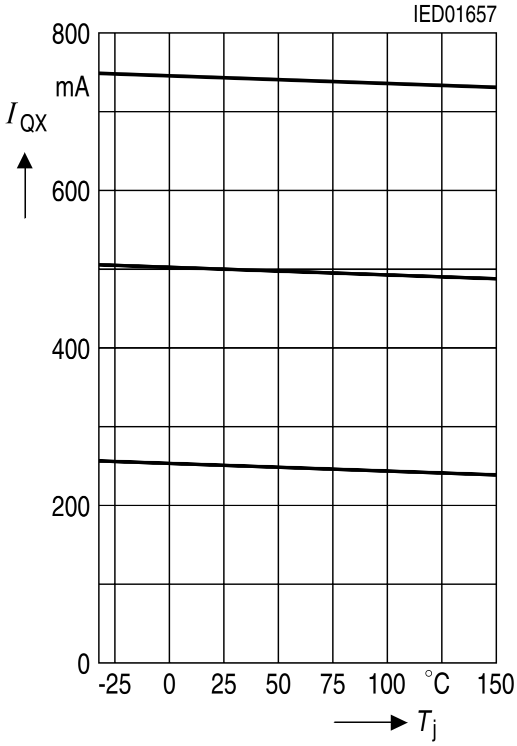
Quiescent Current I_S, I_L versus Supply Voltage V_S



Quiescent Current I_S, I_L versus Junction Temperature T_j



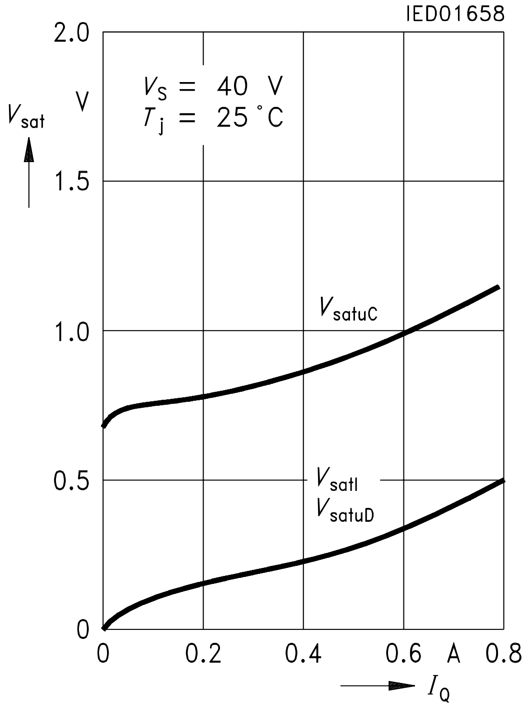
Output Current I_{QX} versus Junction Temperature T_j



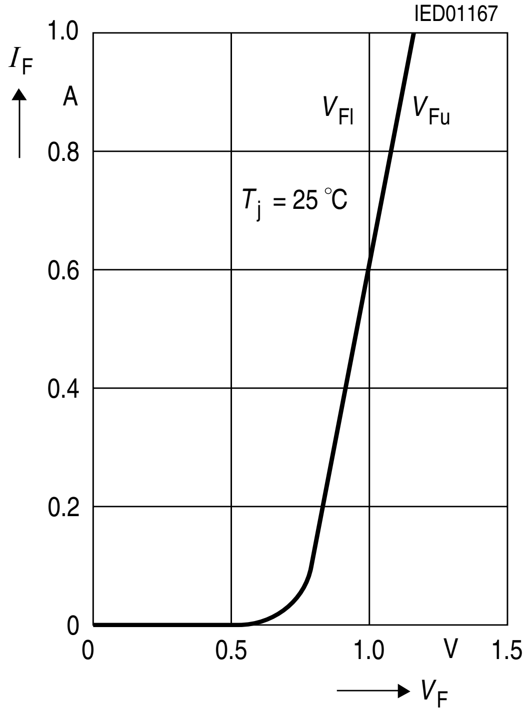
Operating Condition:

V_L = 5 V
V_{Inh} = H
C_{OSC} = 2.2 nF
R_{sense} = 1 Ω
Load: L = 10 mH
R = 2.4 Ω
f_{phase} = 50 Hz
mode: fullstep

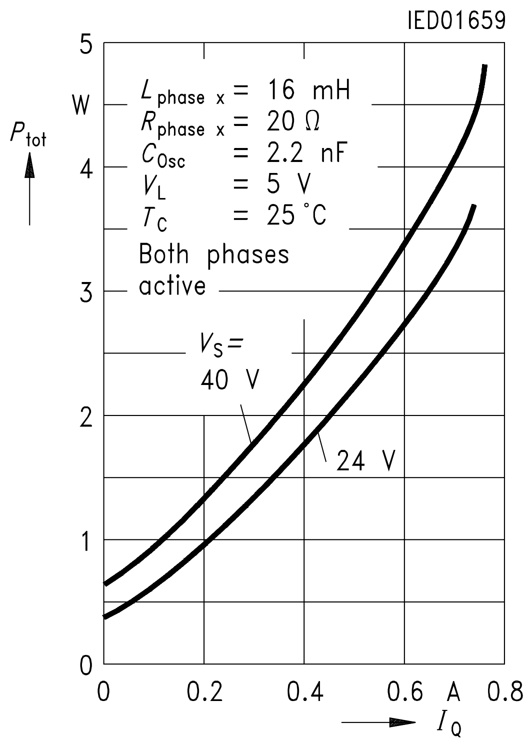
Output Saturation Voltages V_{sat} versus Output Current I_Q



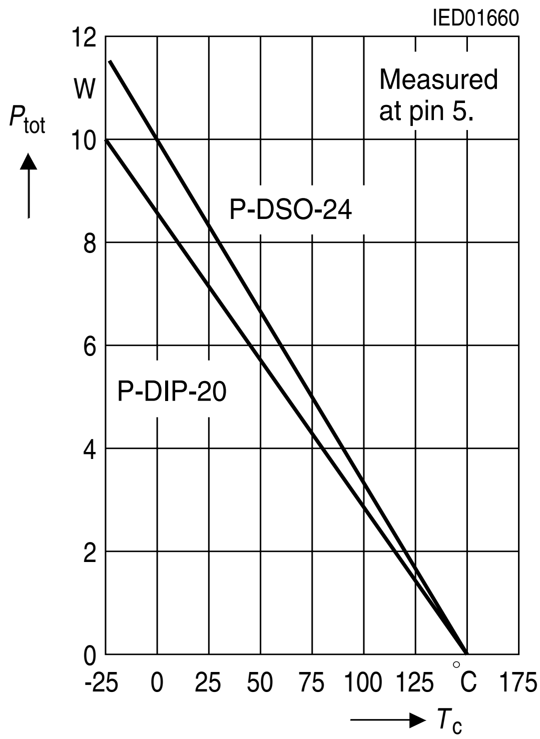
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



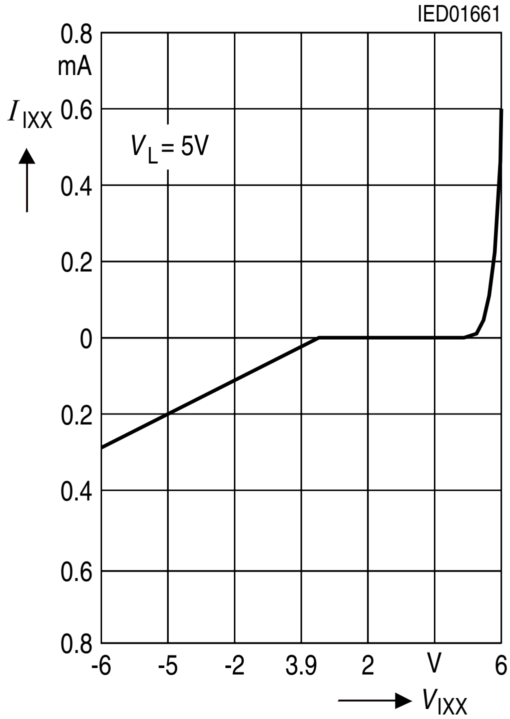
Typical Power Dissipation P_{tot} versus Output Current I_Q (Non Stepping)



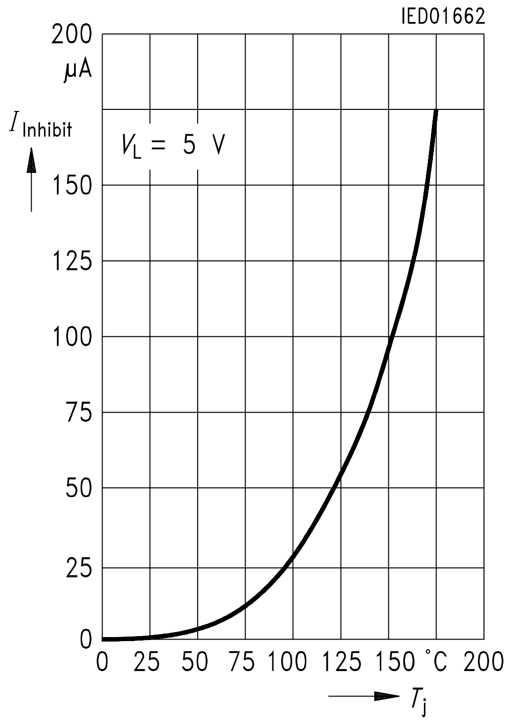
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



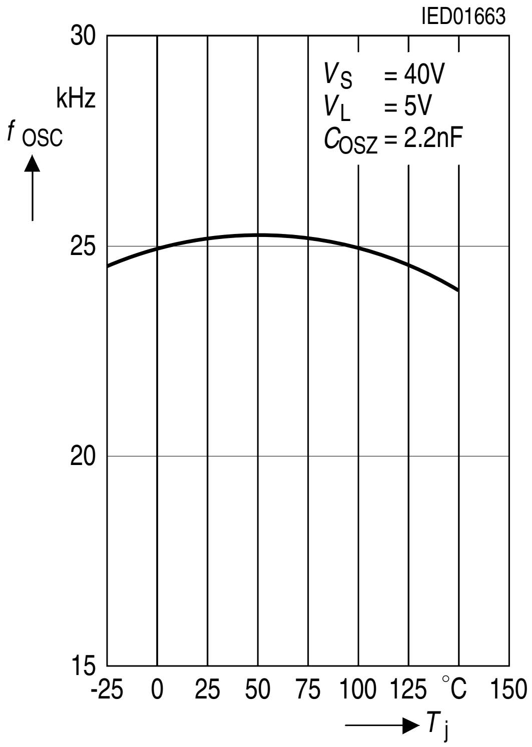
Input Characteristics of I_{xx}, Phase X, Inhibit



Input Current of Inhibit versus Junction Temperature T_j



Oscillator Frequency f_{OSC} versus Junction Temperature T_j



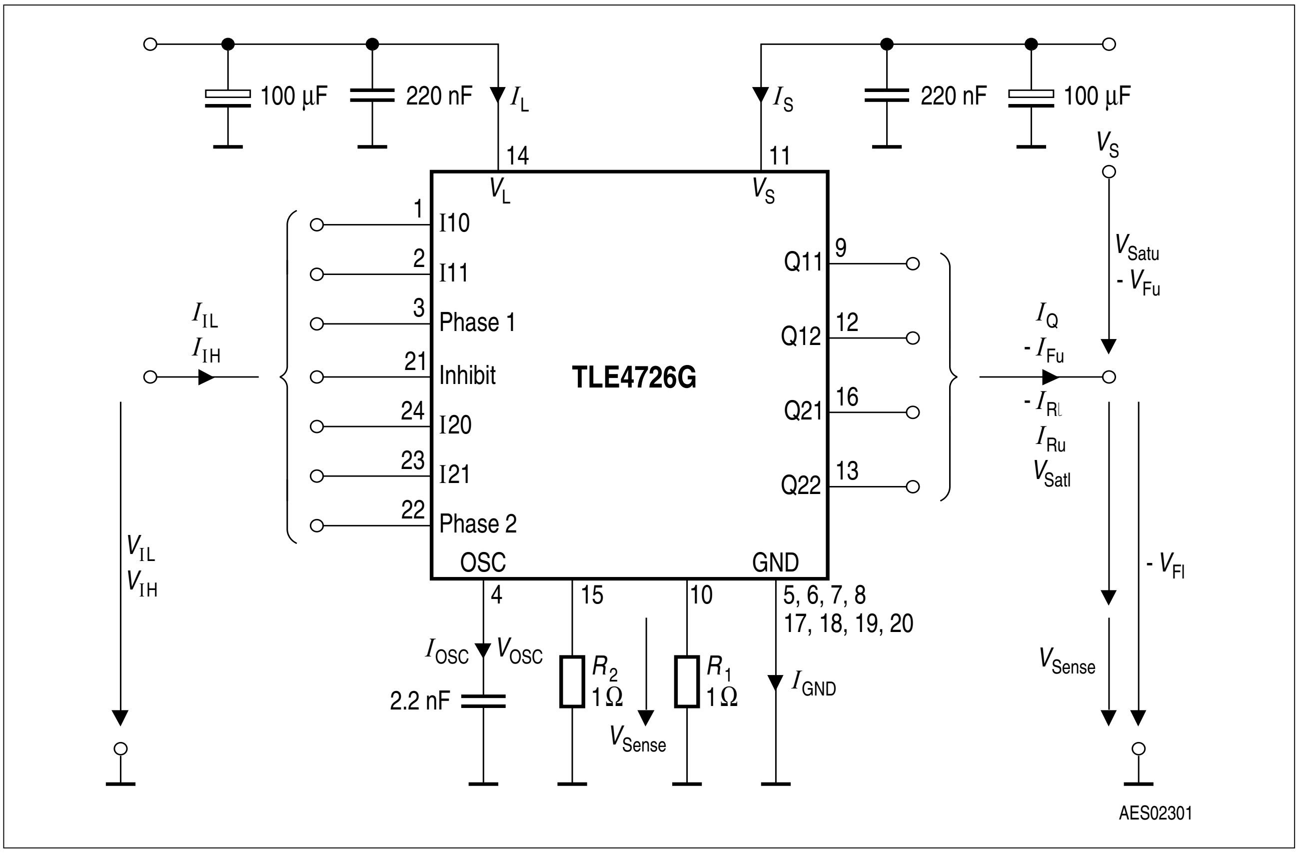


Figure 3 Test Circuit

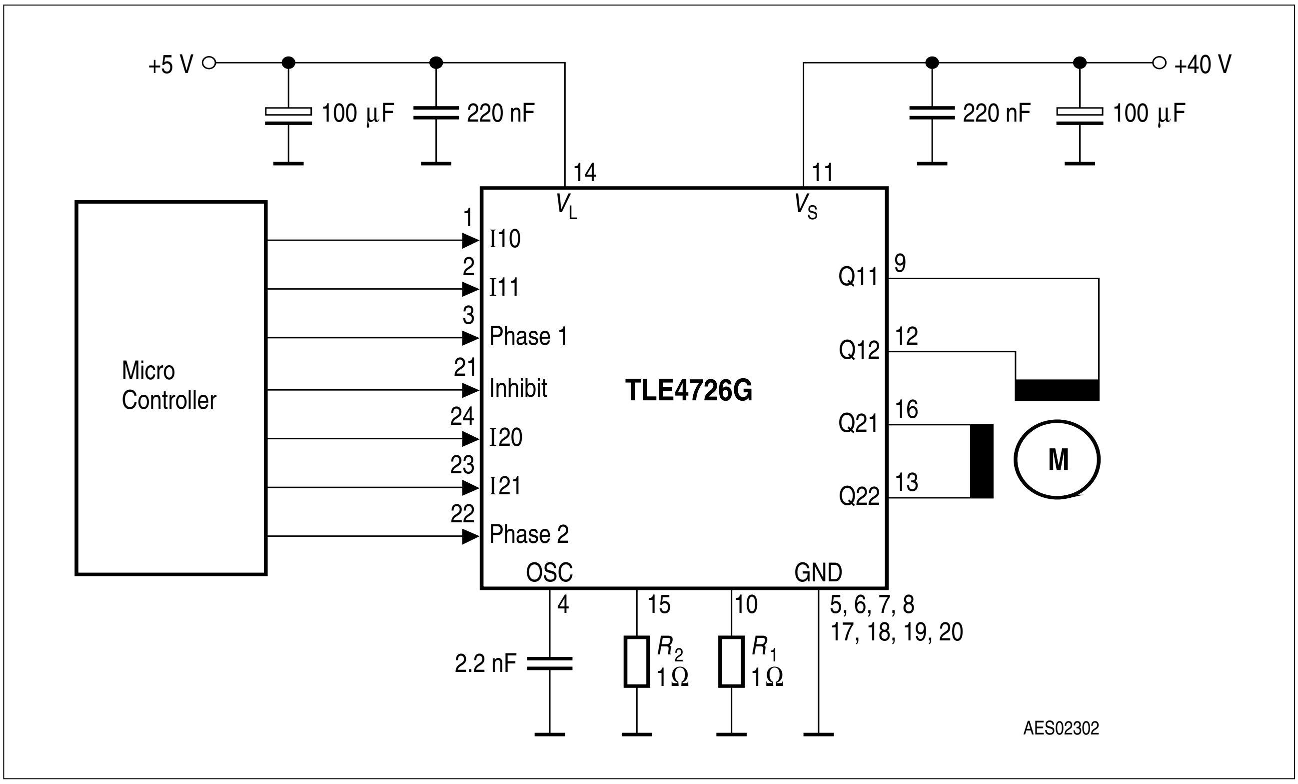


Figure 4 Application Circuit

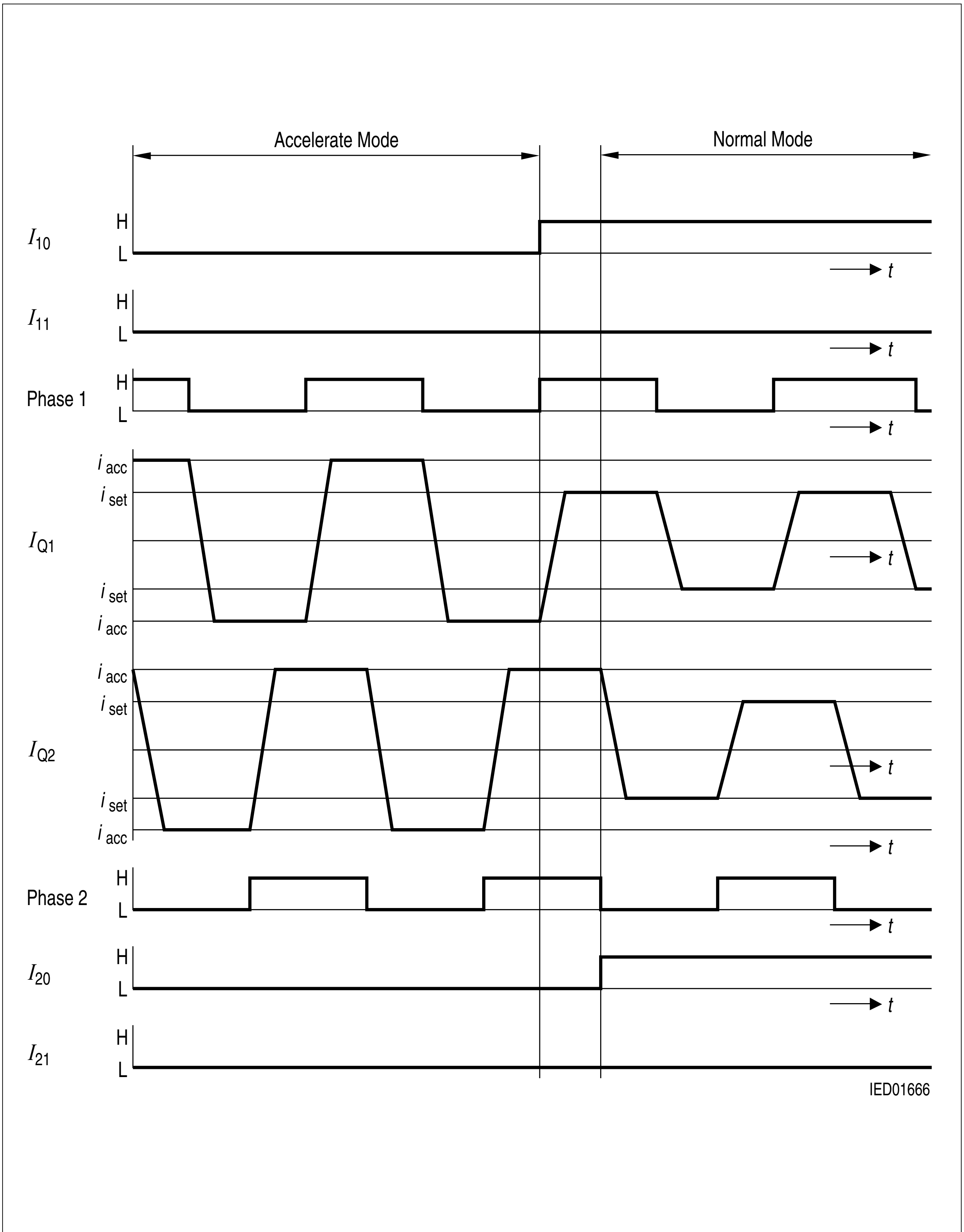


Figure 5 Full-Step Operation

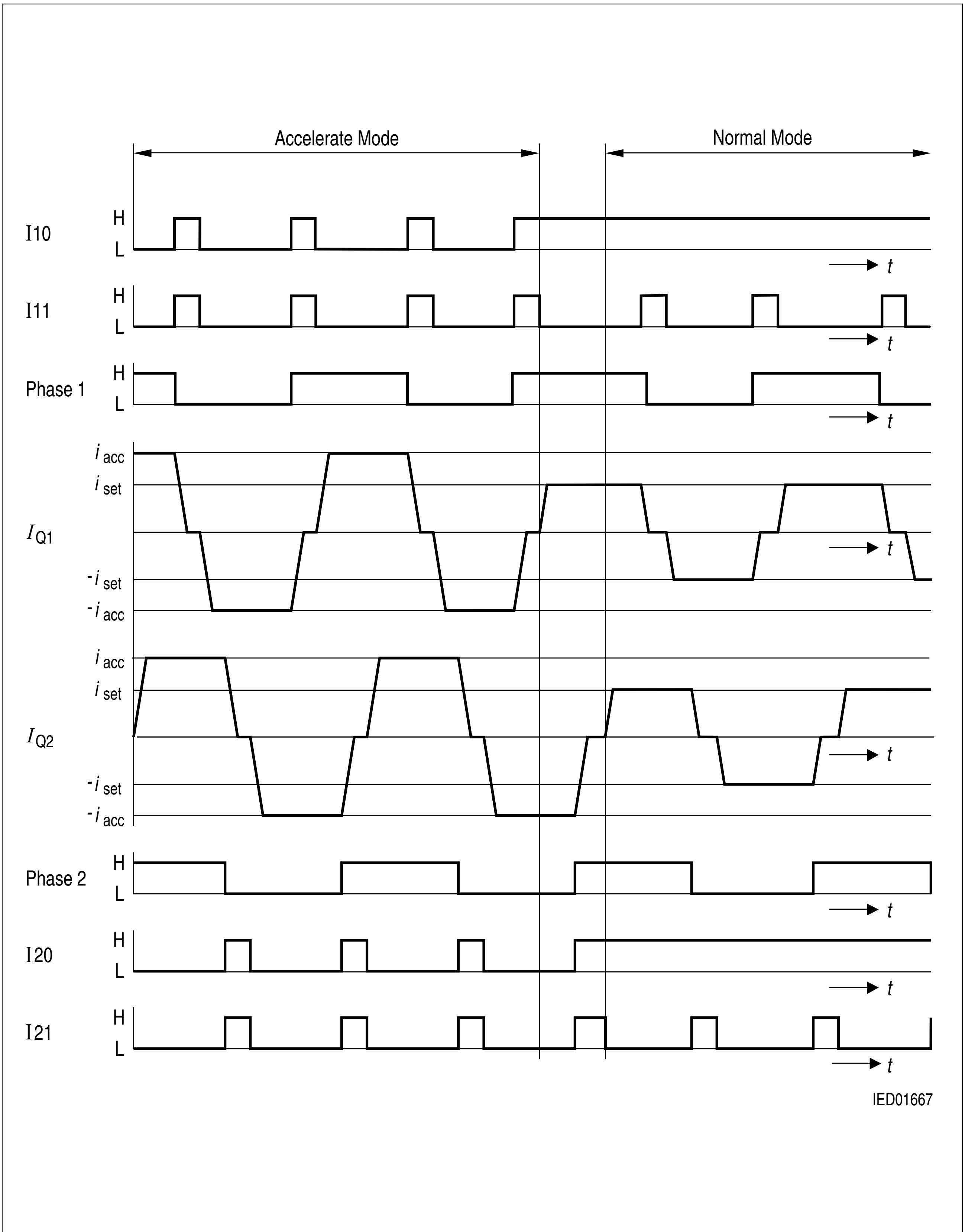


Figure 6 Half-Step Operation

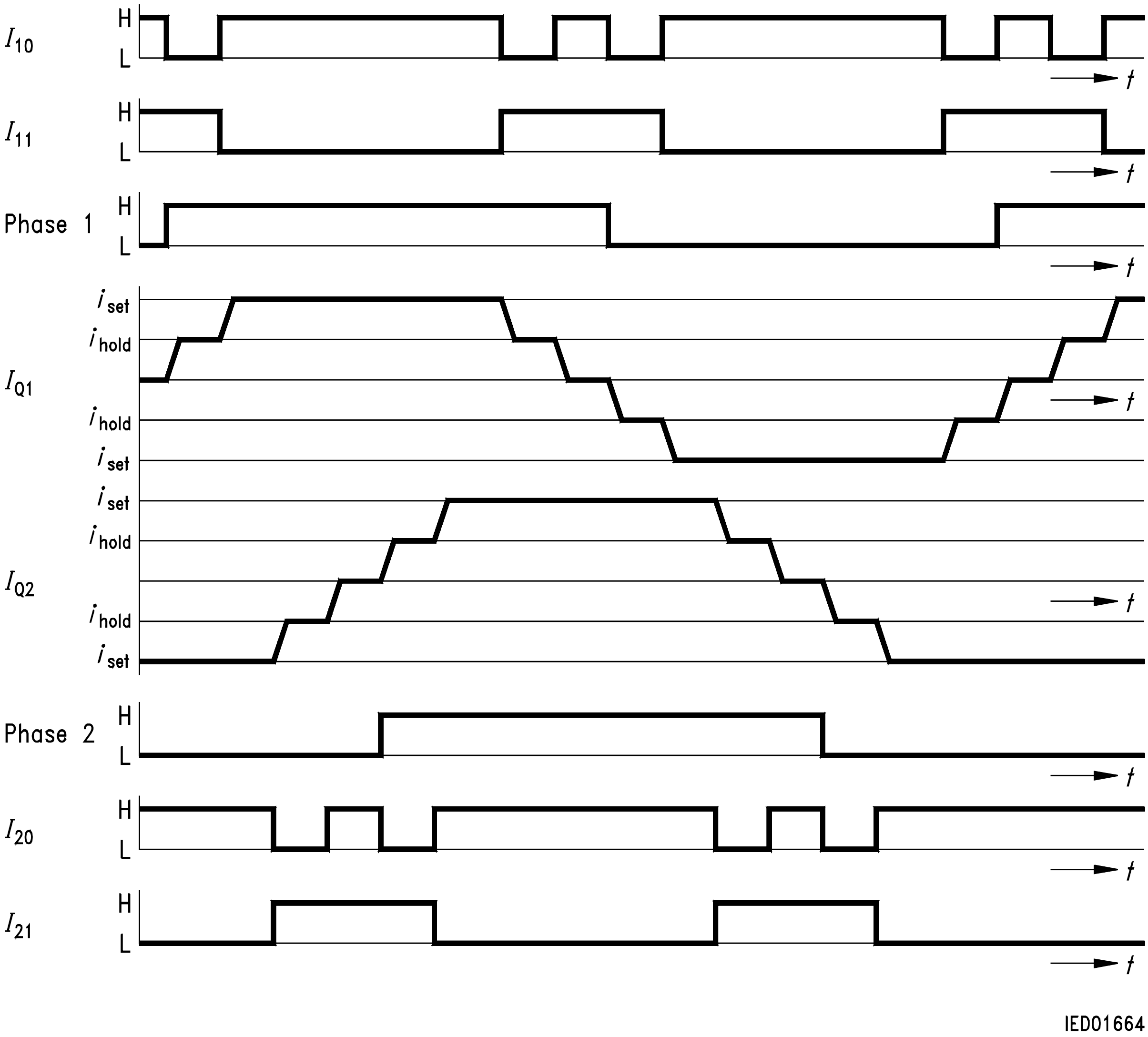


Figure 7 Quarter-Step Operation

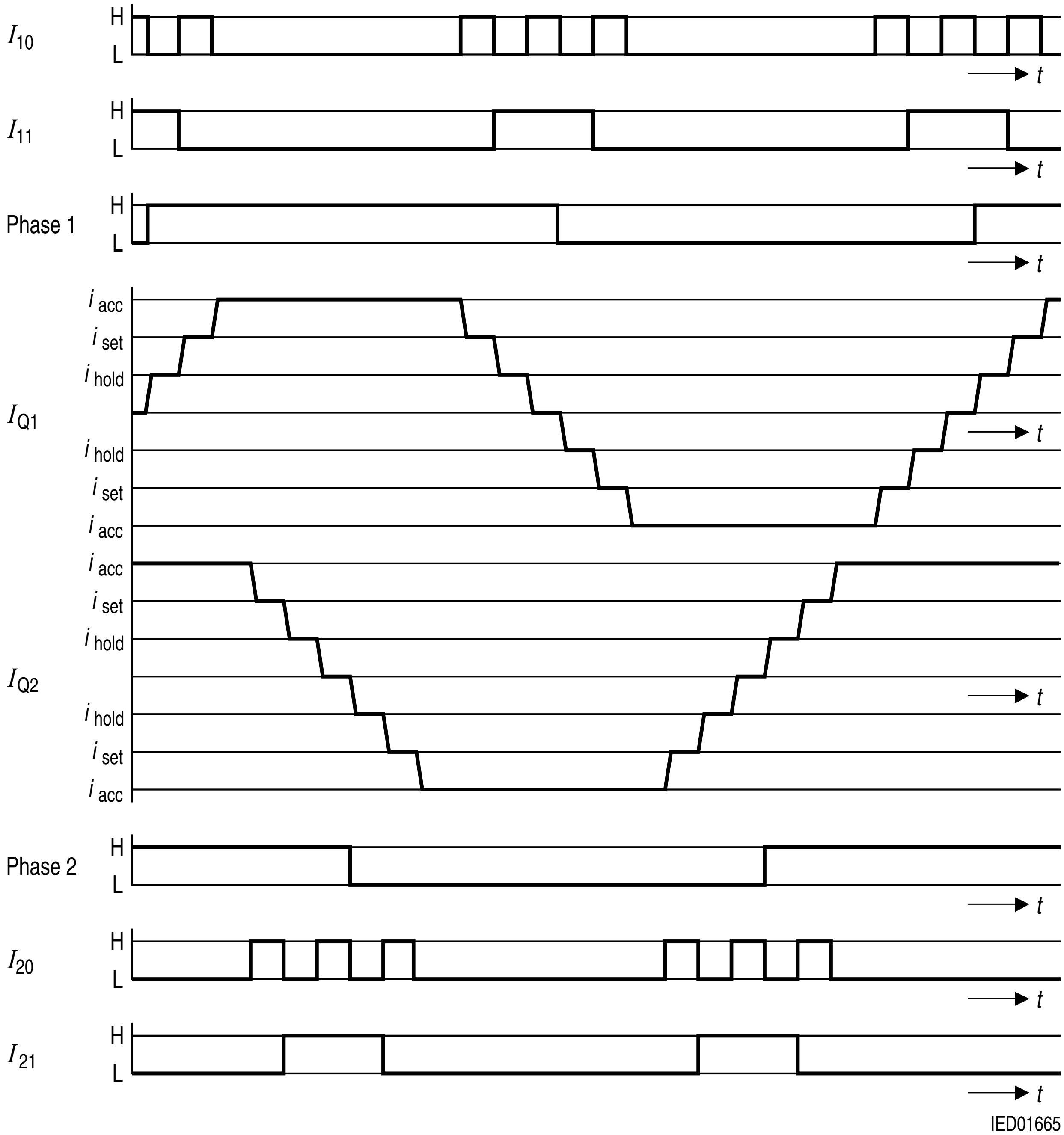
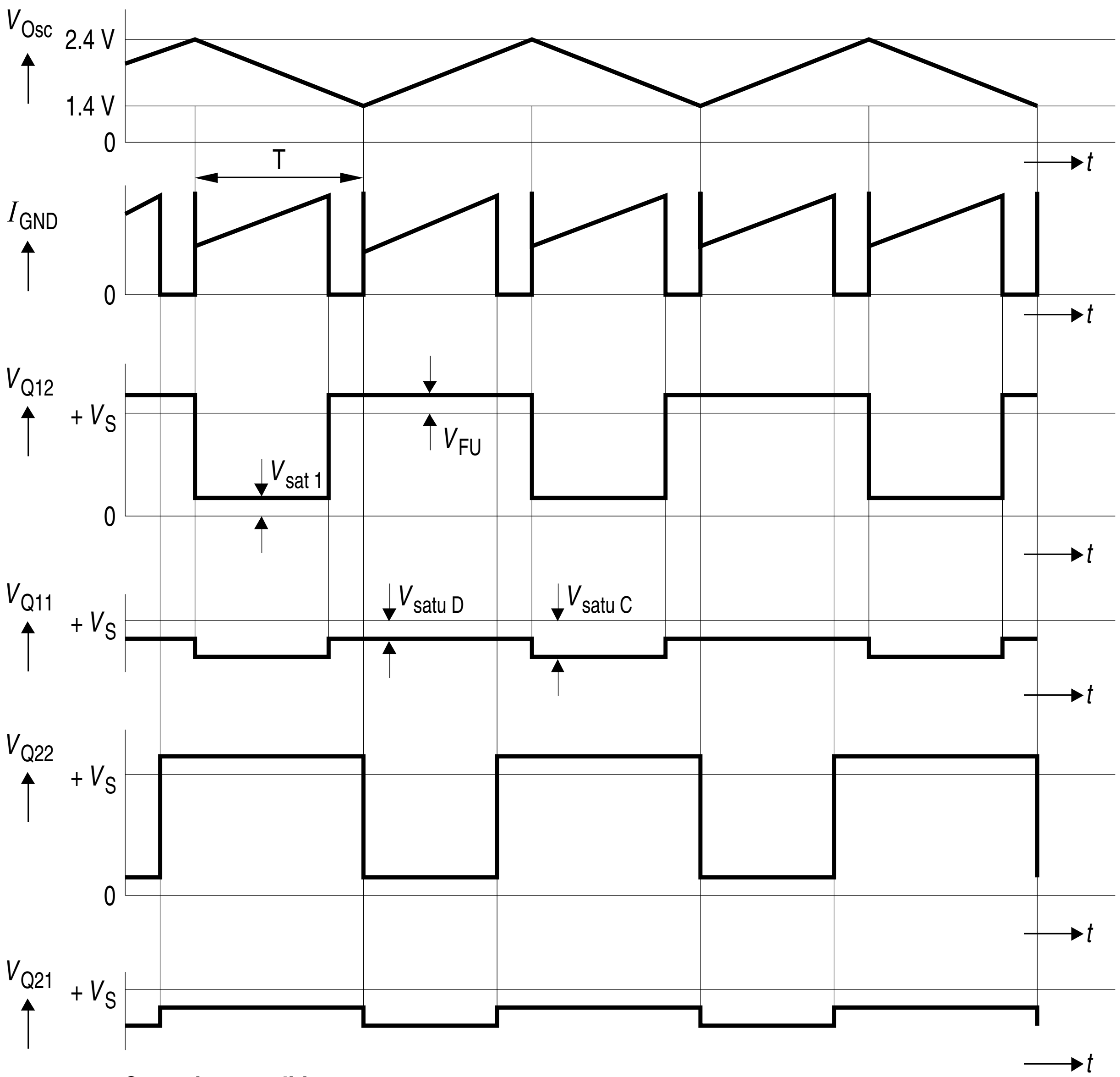


Figure 8 Mini-Step Operation



Operating conditions:

V_S = 40 V
V_L = 5 V
$L_{phase\ x}$ = 10 mH
$R_{phase\ x}$ = 20 Ω
$V_{phase\ x}$ = H
$V_{Inhibit}$ = H
V_{xx} = L

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Figure 9 Current Control

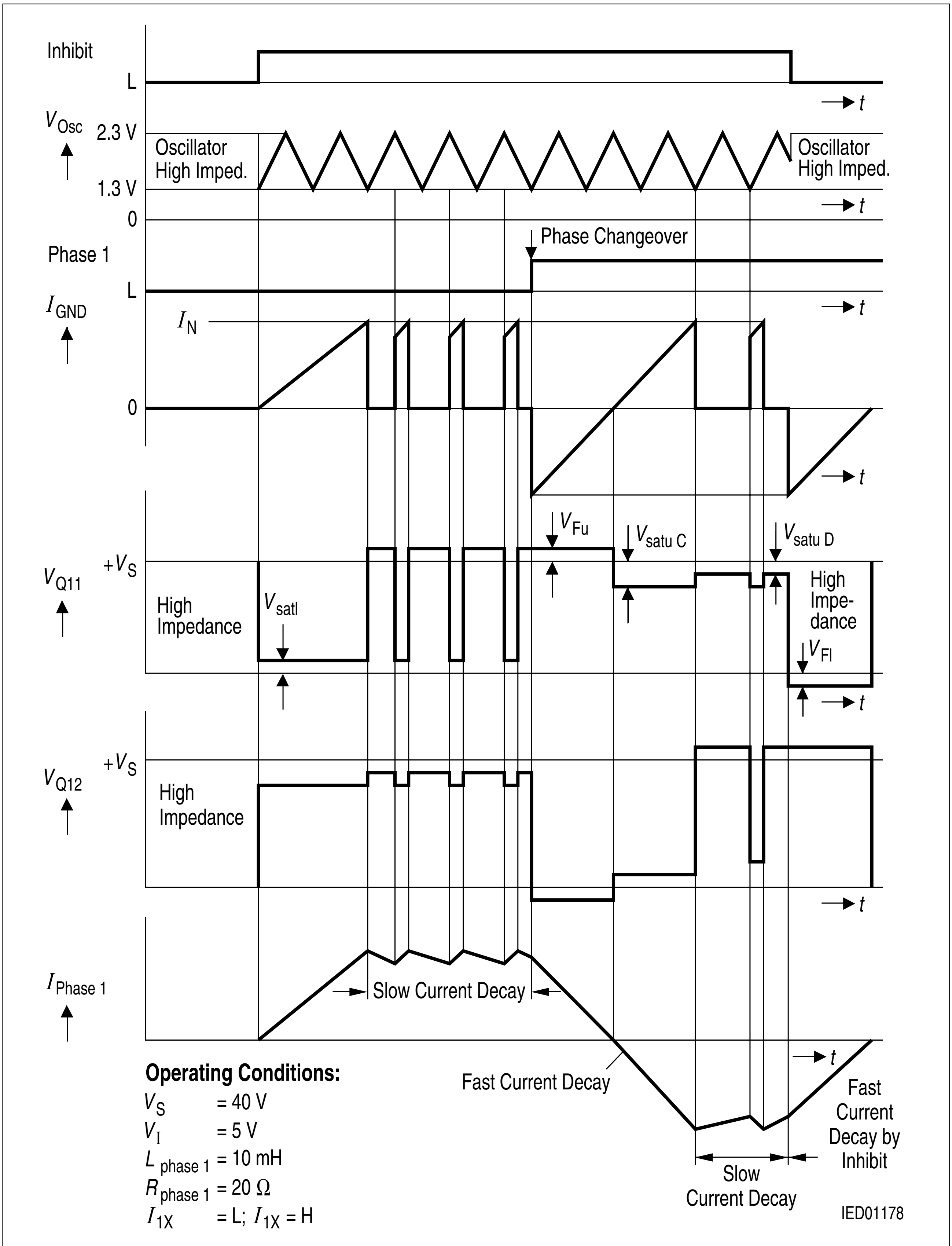


Figure 10 Phase Reversal and Inhibit

Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat} (transistor saturation voltage and diode forward voltages),
quiescent losses P_q (quiescent current times supply voltage) and
switching losses P_s (turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$$

where

$$P_{sat} \cong I_N \{ V_{satl} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d) \}$$

$$P_q = I_q \times V_S + I_L \times V_L$$

$$P_S \cong \frac{V_S}{T} \left\{ \frac{i_D \times t_{DON}}{2} + \frac{i_D + i_R \times t_{ON}}{4} + \frac{I_N}{2} t_{DOFF} + t_{OFF} \right\}$$

I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-on delay
i_R = peak reverse current
t_p = conducting time of chopper transistor
t_{ON} = turn-ON time
t_{OFF} = turn-OFF time
t_{DON} = turn-ON delay
t_{DOFF} = turn-OFF delay
T = cycle duration
d = duty cycle t_p/T
V_{satl} = saturation voltage of sink transistor (T3, T4)
V_{satuC} = saturation voltage of source transistor (T1, T2) during charge cycle
V_{satuD} = saturation voltage of source transistor (T1, T2) during discharge cycle
V_{Fu} = forward voltage of free-wheeling diode (D1, D2)
V_S = supply voltage
V_L = logic supply voltage
I_L = current from logic supply

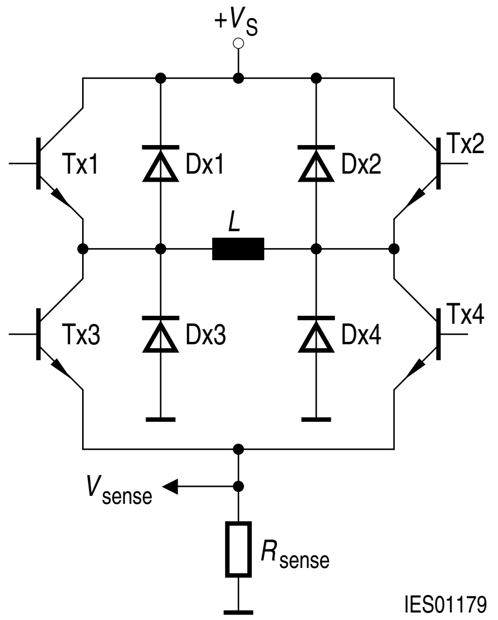


Figure 11

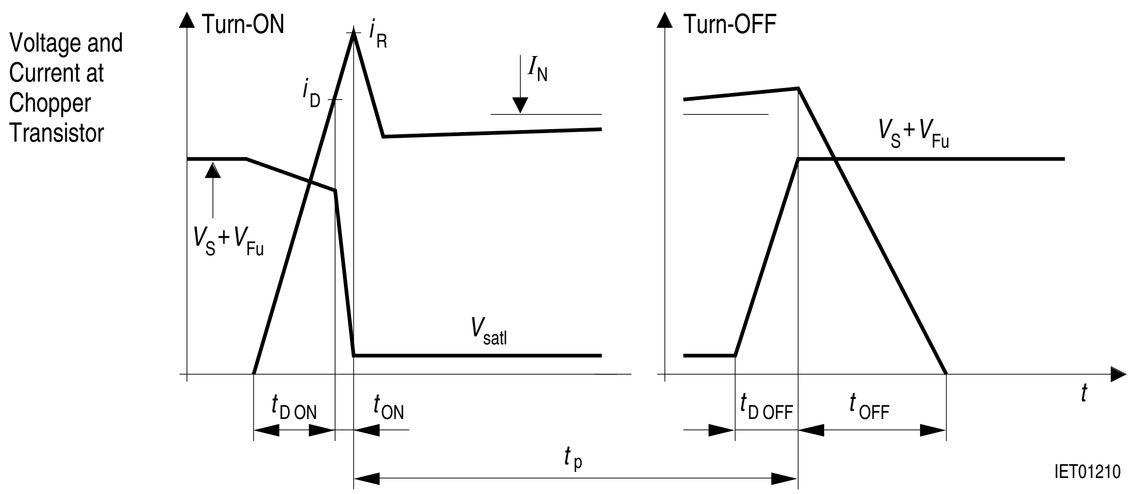


Figure 12

Application Hints

The TLE726G is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TLE726G will work with supply voltages ranging from 5 V to 50 V at pin V_S. As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.22 μF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_1 and R_2. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.25 V, 0.5 V and 0.75 V); (R_1 , R_2 = 1 Ω). These thresholds are neither affected by variations of V_L nor by variations of V_S .

Due to chopper control fast current rises (up to 10 A/μs) will occur at the sensing resistors R_1 and R_2 . To prevent malfunction of the current sensing mechanism R_1 and R_2 should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchrone chopping of several stepper motor drivers may be desireable to reduce acoustic interference. This can be done by forcing the oscillator of the TLE726G by a pulse generator overdriving the oscillator loading currents (approximately ± 100 μA). In these applications low level should be between 0 V and 1 V while high level should be between 2.6 V and V_L .

Optimizing Noise Immunity

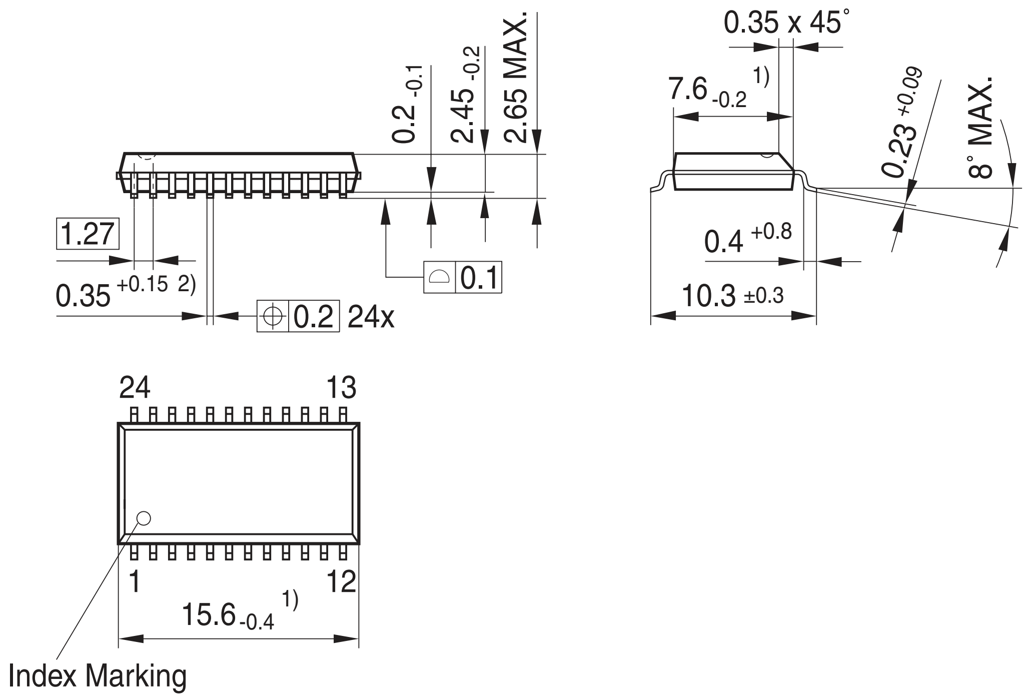
Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TLE4726G uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the Phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the Phase inputs should be avoided by proper control signals.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented. To provide a warning in critical applications, the current of the sensing element is wired to input Inhibit. Before thermal shut down occurs Inhibit will start to pull down by some hundred microamperes. This current can be sensed to build a temperature prealarm.

1 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Lead width can be 0.61 max. in dambar area

P/PG-DSO-24-1, -3, -8, -9, -13, -15, -16-PO V01

Figure 1 PG-DSO-24-13

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

2 Revision History

Revision	Date	Changes
1.1	2008-06-17	Initial version of RoHS-compliant derivate of TLE4726 Page 1: AEC certified statement added Page 1 and 23: added RoHS compliance statement and Green product feature Page 1 and 23: Package changed to RoHS compliant version Page 24-25: added Revision History, updated Legal Disclaimer

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