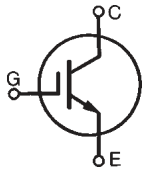
IXYS

Preliminary Technical Information

Polar™ High Speed IGBT for PDP Applications

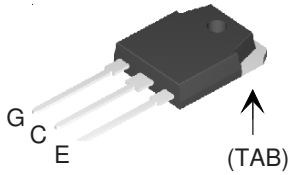
IXGQ170N30PB

V_{CES} = 300 V
I_{CP} = 360 A
$V_{CE(sat)}$ ≤ 1.70 V



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	300	V
V_{GEM}		±30	V
I_{C25}	T_C = 25°C, IGBT chip capability	170	A
I_{CP}	$T_J \le$ 150°C, tp < 10 µs	360	A
$I_{C(RMS)}$	Lead current limit	75	A
SSOA (RBSOA)	V_{GE} = 15 V, T_{VJ} = 150°C, R_G = 20 Ω Clamped inductive load, V_{CE} < 300 V	I_{CM} = 170	A
P_C	T_C = 25°C	330	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s	300	°C
T_{SOLD}	Maximum plastic body temperature for 10 s.	260	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		5.5	g

TO-3P



G = Gate C = Collector
E = Emitter TAB = Collector

Features

- International standard package
- Low $V_{CE(sat)}$
  - for minimum on-state conduction losses
- MOS Gate turn-on
  - drive simplicity

Applications

- PDP Screen Drivers

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)		Characteristic Values Min.	Typ.	Max.	
$V_{GE(th)}$	I_C = 1 mA, V_{CE} = V_{GE}		3.0		5.0	V
I_{CES}	V_{CE} = 300 V				1	µA
	V_{GE} = 0 V	T_J = 125°C			200	µA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
$V_{CE(sat)}$	V_{GE} = 15V,	I_C = 85 A		1.32	1.70	V
	Note 1	T_J = 125°C		1.36		V
		I_C = 170 A		1.73		V
		T_J = 125°C		1.89		V

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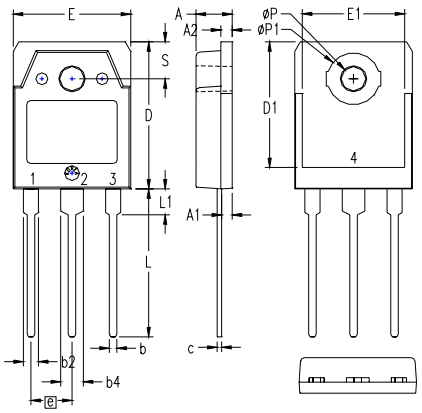
Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 85 A, V_{CE} = 10 V	50	80		S
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz		5140		pF
C_{oes}			315		pF
C_{res}			83		pF
Q_g	I_C = 85 A, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}		143		nC
Q_{ge}			26		nC
Q_{gc}			60		nC
$t_{d(on)}$	Resistive load, T_J = 25°C I_C =85 A, V_{GE} = 15 V V_{CE} = 240 V, R_G = 2.4 Ω		24		ns
t_{ri}			71		ns
$t_{d(off)}$			100		ns
t_{fi}			82		ns
$t_{d(on)}$	Resistive load, T_J = 125°C I_C = 85 A, V_{GE} = 15 V V_{CE} = 240 V, R_G = 2.4 Ω		22		ns
t_{ri}			81		ns
$t_{d(off)}$			102		ns
t_{fi}			157		ns
R_{thJC}				0.375	K/W
R_{thCS}			0.21		K/W

Note 1: Pulse test, t ≤ 300 µs, duty cycle ≤ 2 %

TO-3P (IXTQ) Outline



1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – DRAIN (COLLECTOR)

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.799	19.80	20.30
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
øP	.126	.134	3.20	3.40
øP1	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405B2 6,710,463 6,727,585 6,759,692 6,771,478 B2

Fig. 1. Output Characteristics @ 25ºC

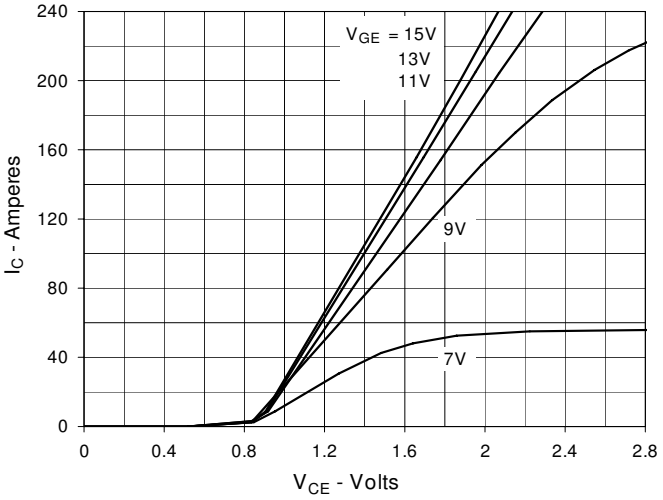

Fig. 2. Exteded Output Characteristics @ 25ºC

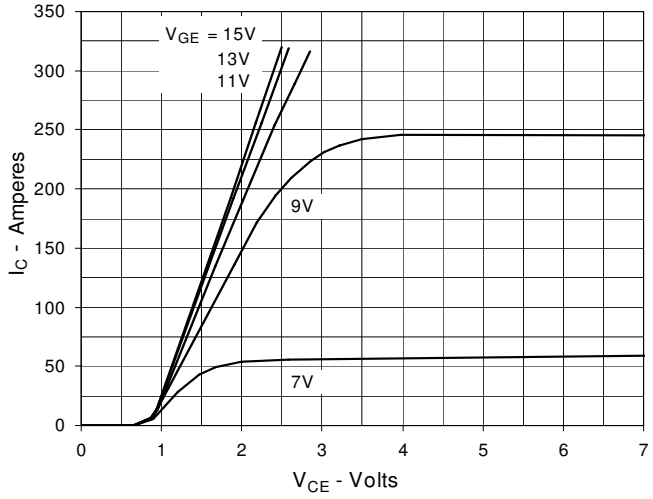

Fig. 3. Output Characteristics @ 125ºC

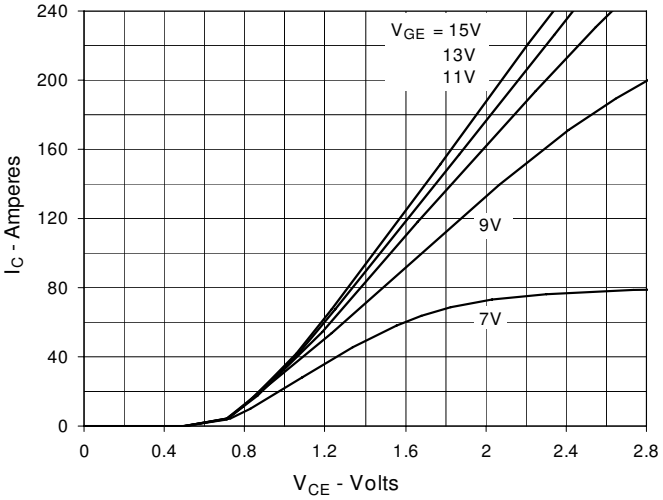

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

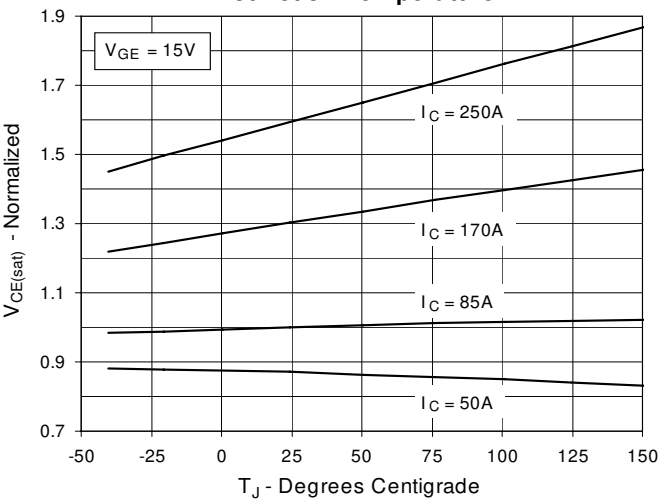

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

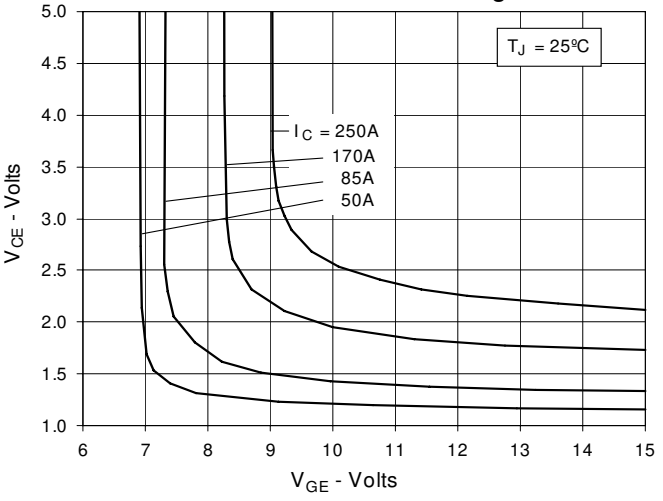

Fig. 6. Input Admittance

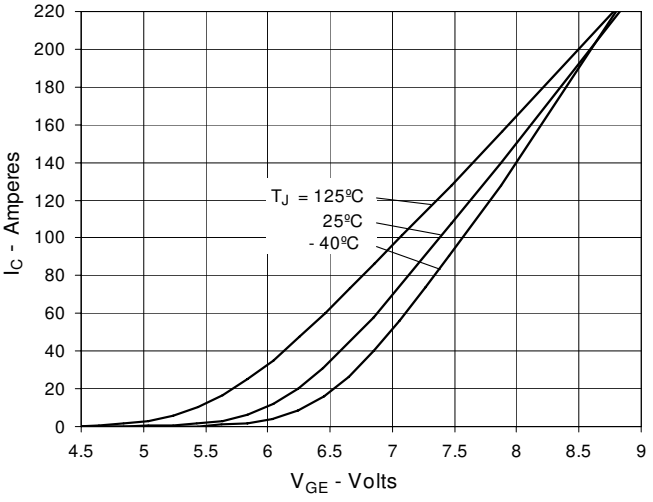

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Fig. 7. Transconductance

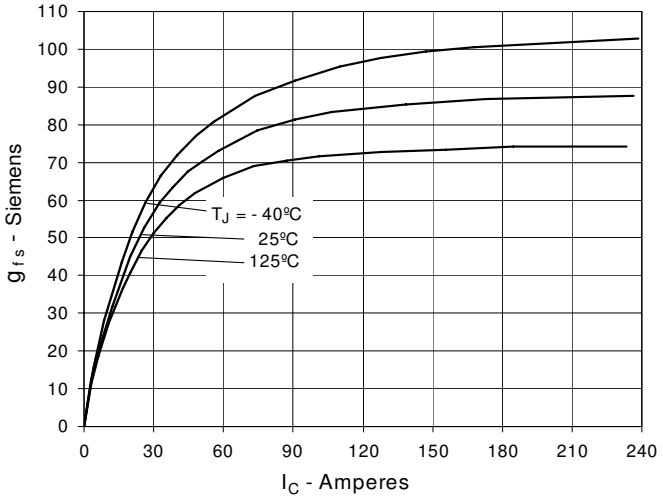

Fig. 8. Resistive Turn-on Rise Time vs. Junction Temperature

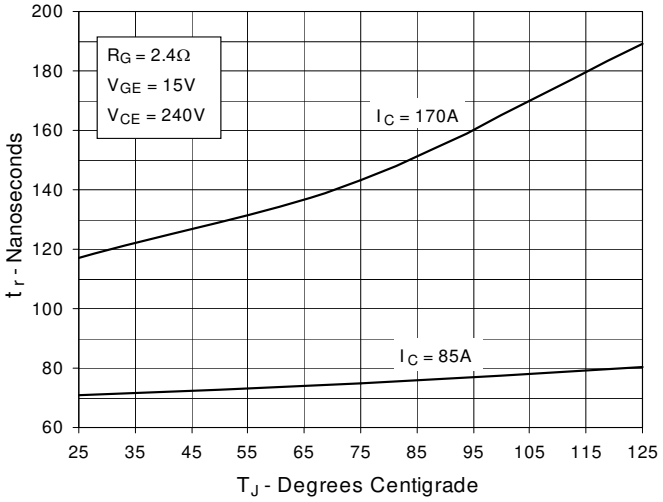

Fig. 9. Resistive Turn-on Rise Time vs. Collector Current

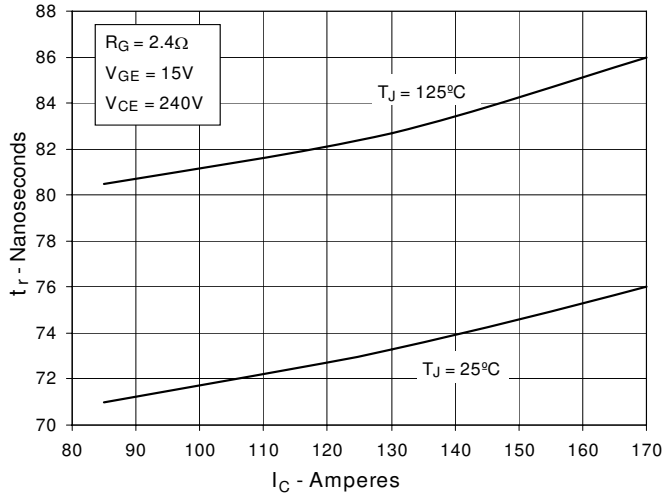

Fig. 10. Resistive Turn-on Switching Times vs. Gate Resistance

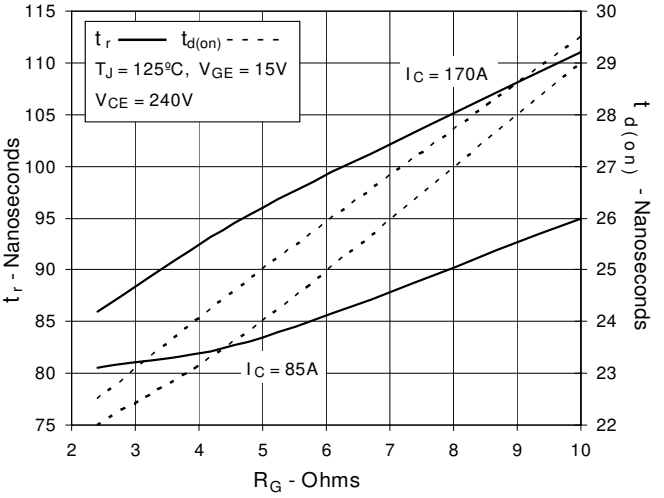

Fig. 11. Resistive Turn-off Switching Times vs. Junction Temperature

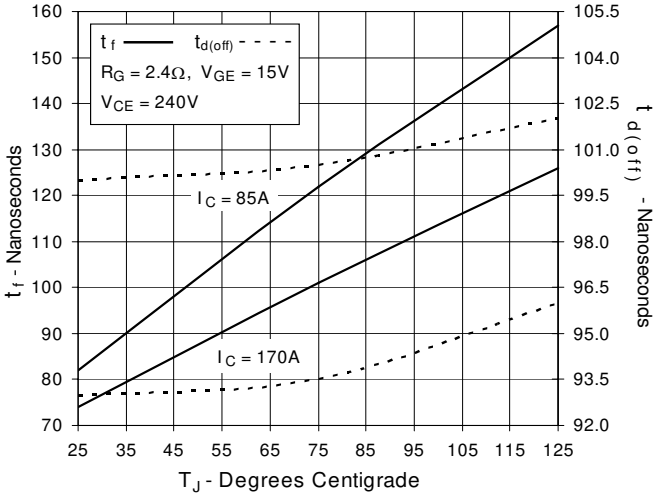

Fig. 12. Resistive Turn-off Switching Times vs. Collector Current

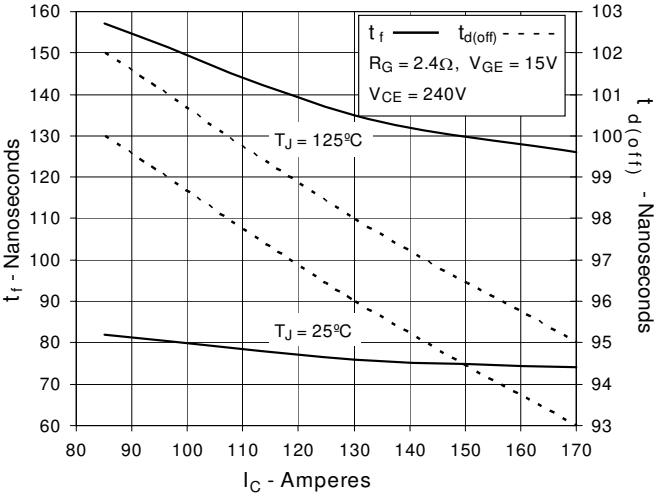

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Fig. 13. Resistive Turn-off Switching Times vs. Gate Resistance

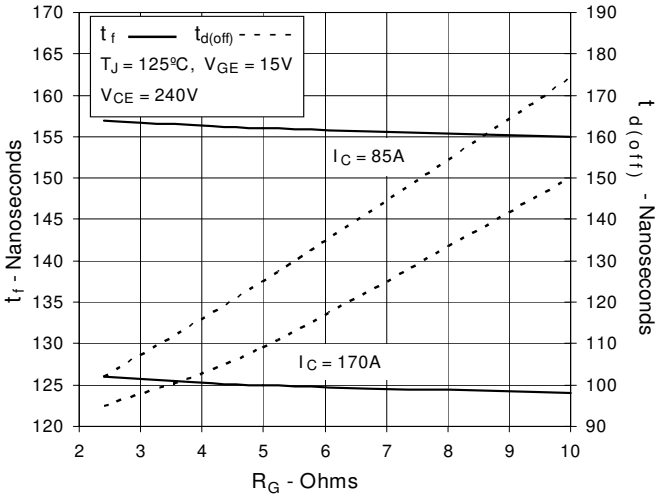


Fig. 14. Gate Charge

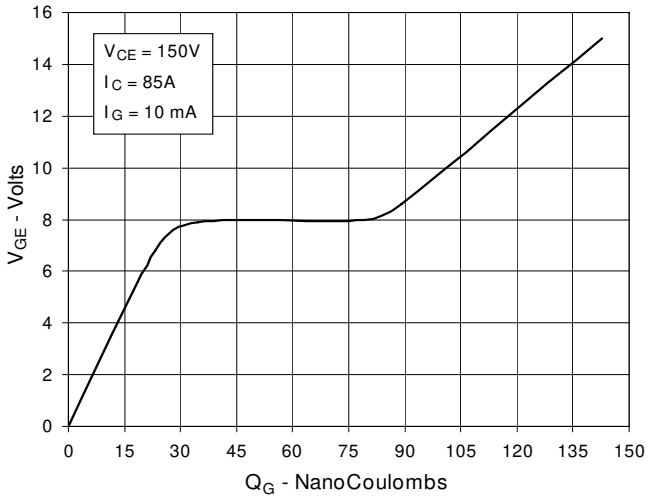


Fig. 15. Reverse-Bias Safe Operating Area

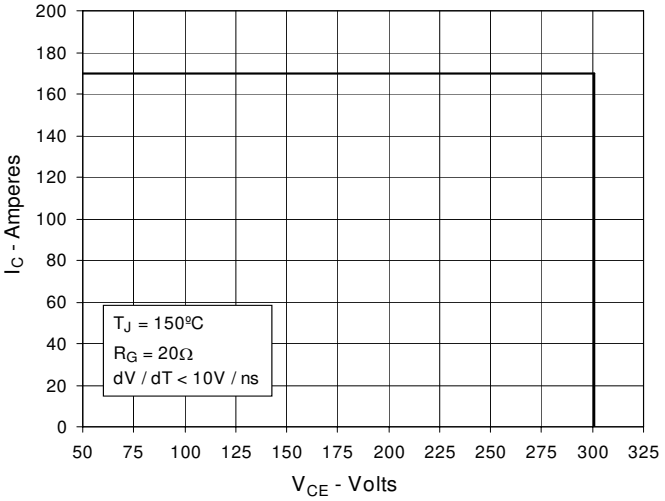


Fig. 16. Capacitance

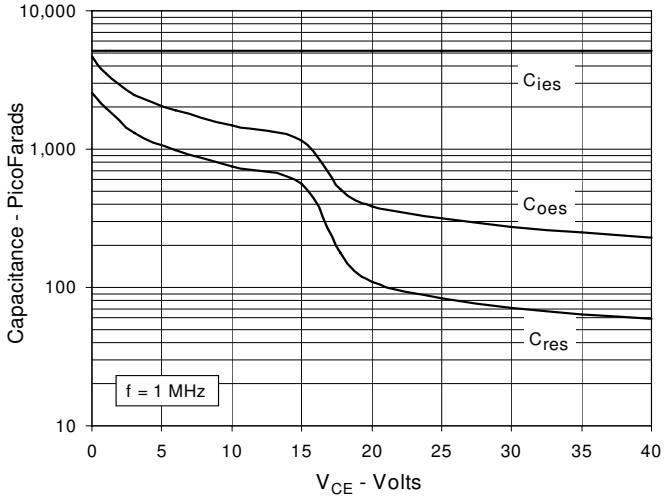
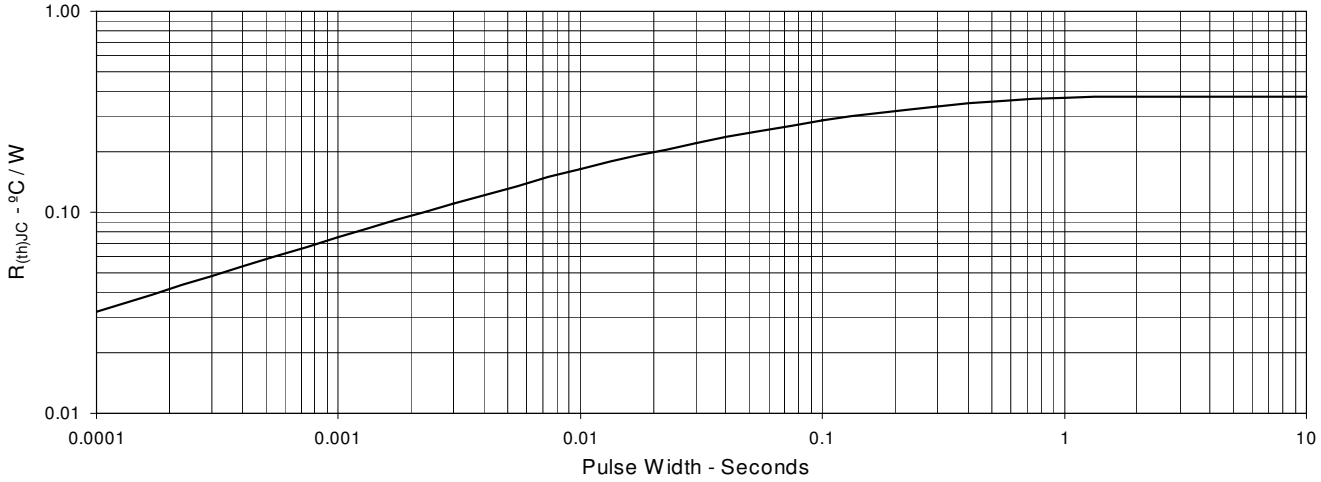


Fig. 17. Maximum Transient Thermal Resistance



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