19-3408; Rev 1; 4/05

MAXIM

MAX1213/MAX1214/MAX1215 Evaluation Kits

Evaluate: MAX1213/MAX1214/MAX1215

General Description

The MAX1213/MAX1214/MAX1215 evaluation kits (EV kits) are a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1213/MAX1214/MAX1215 analog-to-digital converters (ADCs). The MAX1213/MAX1214/MAX1215 accept differential analog inputs; however, the EV kits generate this signal from a user-provided single-ended signal source. The digital outputs produced by the ADC can be easily captured with a user-provided high-speed logic analyzer or data-acquisition system. The EV kits operate from 1.8V power supplies and includes circuitry that generates a clock signal from a user-provided AC signal.

Features

- ♦ **Up to 170Msps/210Msps/250Msps Sampling Rate**
- ♦ **Low-Voltage and Low-Power Operation**
- ♦ **Fully Differential Signal Input Configuration**
- ♦ **On-Board Differential Output Drivers**
- ♦ **Fully Assembled and Tested**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1213EVKIT	0°C to +70°C	68 QFN-EP*
MAX1214EVKIT	0°C to +70°C	68 QFN-EP*
MAX1215EVKIT	0°C to +70°C	68 QFN-EP*

**EP = Exposed pad.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C11, C13, C15, C16, C18, C19, C20, C36–C39	21	0.1µF ±10%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104K
C12, C14, C17	0	Not installed, capacitors (0402)
C21–C24	4	0.22µF ±10%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J224K
C25, C26	0	Not installed, shorted by PC trace (0603)
C27, C28, C40	3	47µF ±10%, 10V tantalum capacitors (C case) AVX TAJC476K010
C29, C41	2	10µF ±20%, 6.3V X5R ceramic capacitors (0805) TDK C2012X5R0J106M
C30	1	22µF ±10%, 6.3V X5R ceramic capacitor (0805) TDK C2012X5R0J226K
C31	0	Not installed, capacitor (0805)
C32, C42	2	1.0µF ±10%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A105K
C33	1	2.2µF ±10%, 6.3V X5R ceramic capacitor (0603) TDK C1608X5R0J225K
C34	0	Not installed, capacitor (0603)
C35	1	0.01µF ±20%, 25V X7R ceramic capacitor (0402) TDK C1005X7R1E103M
J1, CLK	2	SMA PC board vertical-mount connectors
J2	0	Not installed, vertical SMA connector
J3	1	Dual-row 8-pin header
J4–J7	4	Dual-row 40-pin headers
JU1, JU2, JU3	3	3-pin headers
R1, R3, R6, R7, R11, R13, R14, R15, R43	0	Not installed, resistors (0603)
R2	1	49.9Ω ±1% resistor (0603)
R4, R5	2	150Ω ±5% resistors (0603)
R8, R9	2	24.9Ω ±0.1% resistors (0603) IRC PFC-W0603R-02-24R9-B
R10, R12	2	0Ω resistors (0603)
R16, R17	2	10Ω ±1% resistors (0603)
R18–R24, R28–R32, R34, R35	14	100Ω ±1% resistors (0603)
R25, R26, R27, R33	4	100Ω ±5% resistors (0603)
R36, R37	2	510Ω ±5% resistors (0603)
R38, R39, R41, R44–R68	28	510Ω ±5% resistors (0402)
R40	1	100kΩ, 12-turn, 1/4in potentiometer
R42	1	13kΩ ±1% resistor (0603)

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
T1, T2	2	1:1 800MHz RF transformers Mini-Circuits ADT1-1WT
TP1, TP2	2	Test points (black)
U1	1	MAX1213/14/15EGK (68-pin QFN, 10mm x 10mm)
U2	1	3.3V ECL differential receiver (8-pin SO) ON Semiconductor MC100LVEL16D
U3–U6	4	3.3V ECL quad differential receivers (20-pin SO) ON Semiconductor MC100LVEL17DW
Y1	0	Not installed, clock oscillator
None	1	MAX1213/14/15 PC board

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
IRC	361-992-7900	361-992-3377	www.irctt.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com

Note: *Indicate that you are using the MAX1213/MAX1214/MAX1215 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Analog (VCC) 1.8V, 1A
  - Clock (VCLK) 3.3V, 200mA
  - Buffers (VLPEL) 3.3V, 400mA
- Signal generator with low-phase noise and low jitter for clock input (e.g., HP 8662A, HP 8644B)
- Signal generator for analog signal input (e.g., HP 8662A, HP 8644B)
- Logic analyzer or data-acquisition system (e.g., HP 16500C with high-speed state card HP 16517A)
- Digital voltmeter

Procedure

The MAX1213/MAX1214/MAX1215 EV kits are a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Do not turn on power supplies or enable signal generators until all connections are completed:**

1) Verify that shunts are installed in the following locations:
   JU2 (1-2) → divide-by-two disabled
   JU3 (2-3) → two's-complement output selected
   J3 (3-4) → internal reference enabled
2) Connect the clock signal generator to the SMA connector labeled CLK.
3) Connect the analog input signal generator to the SMA connector labeled J1.
4) Connect the logic analyzer with high-speed card probe to either headers J4/J5 (LVDS-compatible signals) or J6/J7 (LVPECL-compatible signals). See Table 4 for header connections.
5) Connect a 1.8V, 1A power supply to VCC. Connect the ground terminal of this supply to GND closest to the VCC pad.
6) Connect a 3.3V, 200mA power supply to VCLK. Connect the ground terminal of this supply to GND closest to the VCLK pad.
7) Connect a 3.3V, 400mA power supply to VLPEL. Connect the ground terminal of this supply to GND closest to the VLPEL pad.

8) Turn on all power supplies.
9) Enable the signal generators. Set the clock signal generator to output a 170MHz/210MHz/250MHz signal, with an amplitude of 2.4V_{P-P}. Set the analog input signal generator to output the desired frequency with an amplitude ≤ 2V_{P-P}. The signal generators should be synchronized.
10) Enable the logic analyzer.
11) Collect data using the logic analyzer.

Detailed Description

The MAX1213/MAX1214/MAX1215 EV kits are a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX1213/MAX1214/MAX1215, 12-bit LVDS output ADCS. The MAX1213/MAX1214/MAX1215 can be evaluated with a maximum clock frequency (f_{CLK}) of 170MHz/210MHz/250MHz .

The MAX1213/MAX1214/MAX1215 accept differential inputs. Applications that only have a single-ended signal source available can use the on-board transformer (T2) to convert the singled-ended signal to a differential signal.

Output level translators (U3–U6) buffer and convert the LVDS output signals of the MAX1213/MAX1214/MAX1215 to higher voltage LVPECL signals that can be captured by a wide variety of logic analyzers. The LVDS outputs are accessed at headers J4 and J5. The LVPECL outputs are accessed at headers J6 and J7.

The EV kits are designed as a four-layer PC board to optimize the performance of the MAX1213/MAX1214/MAX1215. Separate analog, clock, and buffer power planes minimize noise coupling between analog and digital signals; 50Ω coplanar transmission lines are used for analog and clock inputs and 100Ω differential coplanar transmission lines are used for all digital LVDS outputs. All LVDS differential outputs are properly terminated with 100Ω termination resistors between true and complementary digital outputs. The trace lengths of the 100Ω differential LVDS lines are matched to within a few thousandths of an inch to minimize layout-dependent delays.

Power Supplies

The MAX1213/MAX1214/MAX1215 EV kits require separate analog, clock, and buffer power supplies for best performance. A 1.8V power supply is used to power the analog and digital portion of the MAX1213/MAX1214/MAX1215. The on-board clock circuitry is powered by a 3.3V power supply. A separate 3.3V power supply is used to power the output buffers (U3–U6) on the EV kit.

Clock

The MAX1213/MAX1214/MAX1215 require a differential clock signal. However, if only a single-ended clock signal source is available, the EV kit's on-board level translator helps to convert a singled-ended clock signal to the required differential signal. An on-board clock-shaping circuit generates a differential clock signal from an AC sine-wave signal applied to the clock input SMA connector (CLK). The input signal should not exceed an amplitude of 2.6V_{P-P}. The frequency of the sinusoidal input clock signal determines the sampling frequency (f_{CLK}) of the ADC. A differential line receiver (U2) processes the input signal to generate the required clock signal. The frequency of the clock signal should not exceed 170MHz/210MHz/250MHz.

Clock Divider

The MAX1213/MAX1214/MAX1215 feature an internal divide-by-two clock divider. Use jumper JU2 to enable/disable this feature. See Table 1 for shunt positions.

Table 1. Clock-Divider Shunt Settings (JU2)

SHUNT POSITION	MAX1213/14/15 CLKDIV PIN	DESCRIPTION
1-2 (default)	Connected to VCC	Clock signal divided by 1
2-3	Connected to GND	Clock signal divided by 2

Input Signal

The MAX1213/MAX1214/MAX1215 accept differential analog input signals. However, the EV kits only require a single-ended analog input signal with an amplitude of less than 2V_{P-P} provided by the user. An on-board transformer then takes the single-ended analog input and generates a differential analog signal, which is applied to the ADC's differential input pins.

Optional Input Transformer

The MAX1213/MAX1214/MAX1215 EV kits use a second transformer to enhance THD and SFDR performance at high input frequencies (>100MHz). This transformer helps to reduce the increase of even-order harmonics at high frequencies. To use only the primary transformer, follow the directions below:

1) Remove R10 and R12.
2) Install a 0.1µF capacitor on C14.
3) Connect the analog signal source to J2 instead of J1.

Reference Voltage

There are two methods to set the full-scale range of the MAX1213/MAX1214/MAX1215. The MAX1213/MAX1214/MAX1215 EV kits can be configured to use the ADC's internal reference, or a stable, low-noise, external reference can be applied to the REFIO pad. Jumper J3 controls which reference source is used. See Table 2 for shunt settings.

Table 2. Reference Shunt Settings (J3)

SHUNT POSITION	DESCRIPTION
1-2	Internal reference disabled. Apply an external reference voltage to the REFIO pad.
3-4 (default)	Internal reference enabled.
5-6	Increases FSR through the trim potentiometer R40.
7-8	Decreases FSR through the trim potentiometer R40.

Output Signal

The MAX1213/MAX1214/MAX1215 feature a single 12-bit, parallel, LVDS-compatible, digital output bus. The digital outputs also feature a clock bit (DCOP/N) for data synchronization, and a data overrange bit (ORP/N). See Table 4 for header connections.

Output Format

The digital output coding can be chosen to be either in two's complement or straight offset binary format by configuring jumper JU3. See Table 3 for shunt settings.

Table 3. Output-Format Shunt Settings (JU3)

SHUNT POSITION	MAX1213/14/15 $\overline{T}$/B Pin	DESCRIPTION
1-2	Connected to VCC	Digital output in straight offset binary
2-3 (default)	Connected to GND	Digital output in two's complement

Output Bit Locations

The digital outputs of the ADC are connected to two 40-pin headers (J4 and J5). PC board trace lengths are matched to minimize output skew and improve performance of the device. In addition, four drivers (U3–U6) buffer and level translate the ADC's digital outputs to LVPECL-compatible signals. The drivers increase the differential voltage swing and are able to drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to two 40-pin headers (J6 and J7). See Table 4 for headers J4–J7 bit locations.

Table 4. Output Bit Locations

BIT		UNBUFFERED (LVDS)	BUFFERED (LVPECL)	BIT		DESCRIPTION
D11	P	J6-10	J4-10	P	LD11	MSB
	N	J6-9	J4-9	N		
D10	P	J6-16	J4-16	P	LD10	Data bits
	N	J6-15	J4-15	N		
D9	P	J6-22	J4-22	P	LD9	
	N	J6-21	J4-21	N		
D8	P	J6-28	J4-28	P	LD8	
	N	J6-27	J4-27	N		
D7	P	J6-34	J4-34	P	LD7	
	N	J6-33	J4-33	N		
D6	P	J6-40	J4-40	P	LD6	
	N	J6-39	J4-39	N		
D5	P	J7-8	J5-8	P	LD5	
	N	J7-7	J5-7	N		
D4	P	J7-14	J5-14	P	LD4	
	N	J7-13	J5-13	N		
D3	P	J7-20	J5-20	P	LD3	
	N	J7-19	J5-19	N		
D2	P	J7-26	J5-26	P	LD2	
	N	J7-25	J5-25	N		
D1	P	J7-32	J5-32	P	LD1	
	N	J7-31	J5-31	N		
D0	P	J7-38	J5-38	P	LD0	LSB
	N	J7-37	J5-37	N		
OR	P	J6-4	J4-4	P	LOR	Overrange bit
	N	J6-3	J4-3	N		
DCO	P	J7-2	J5-2	P	LDC0	Clock output signal
	N	J7-1	J5-1	N		

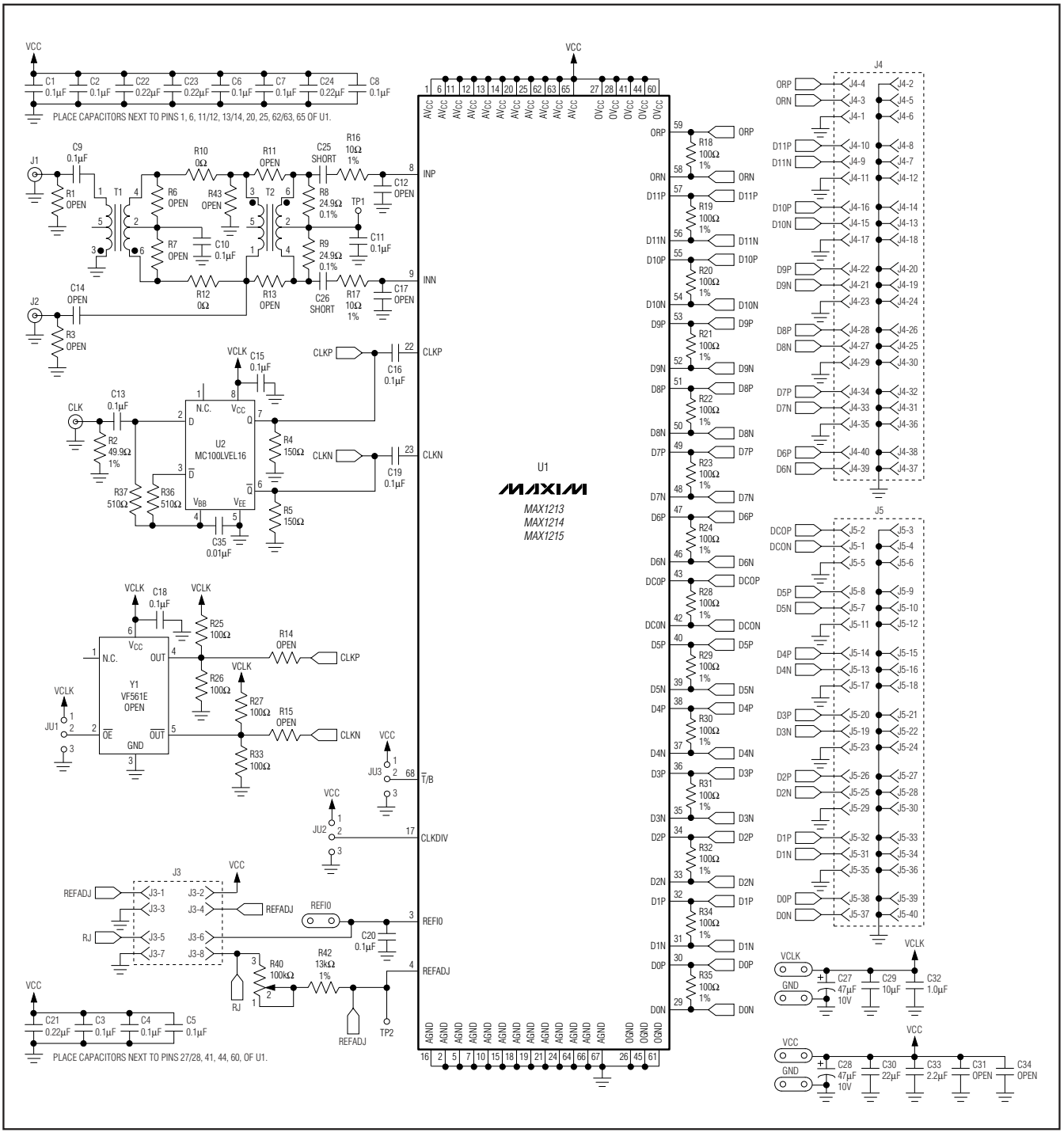

Figure 1. MAX1213/MAX1214/MAX1215 EV Kit Schematic (Sheet 1 of 2)

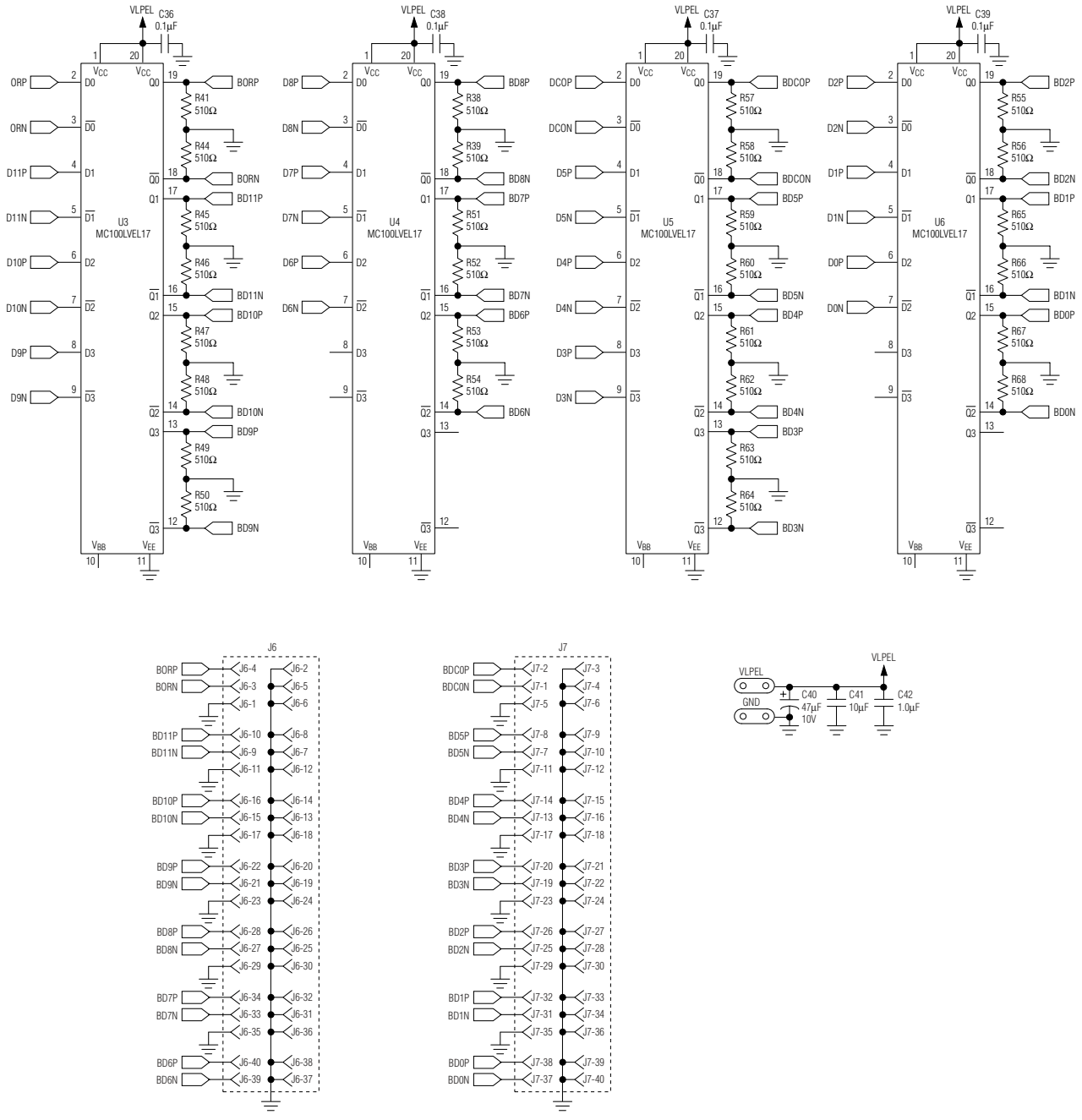

Figure 1. MAX1213/MAX1214/MAX1215 EV Kit Schematic (Sheet 2 of 2)

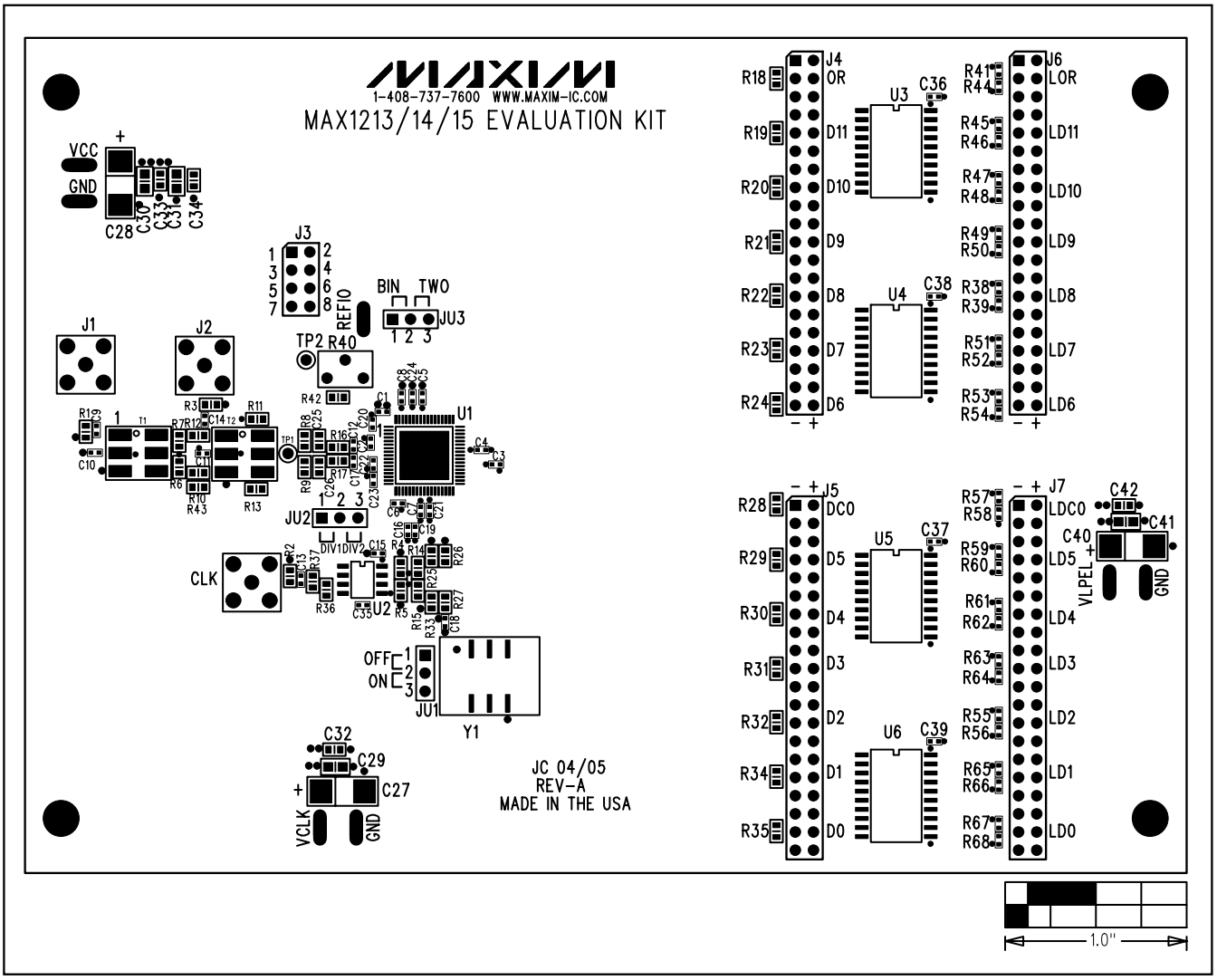

Figure 2. MAX1213/MAX1214/MAX1215 EV Kit Component Placement Guide—Component Side

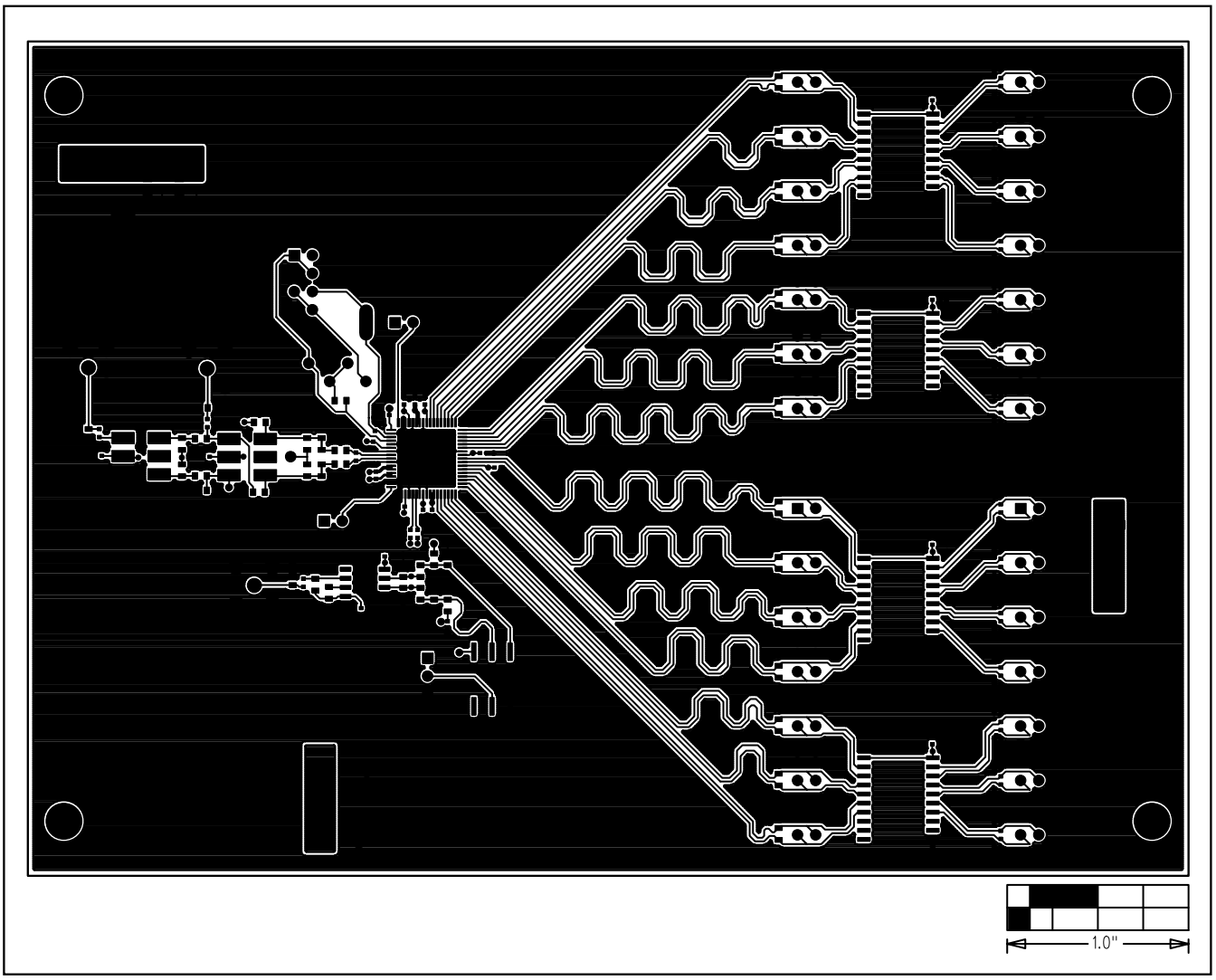

Figure 3. MAX1213/MAX1214/MAX1215 EV Kit PC Board Layout—Component Side

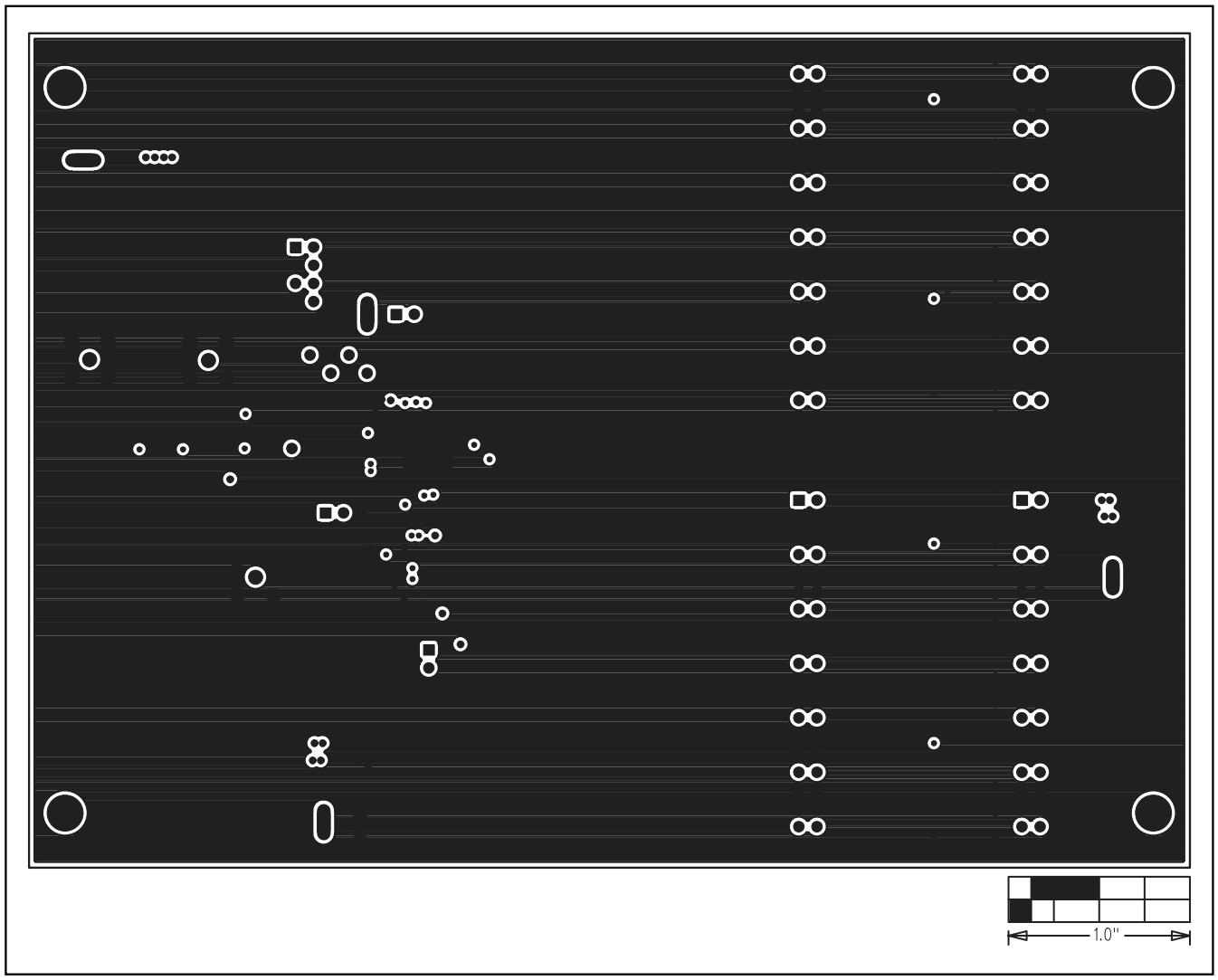

Figure 4. MAX1213/MAX1214/MAX1215 EV Kit PC Board Layout—Ground Plane (Layer 2)

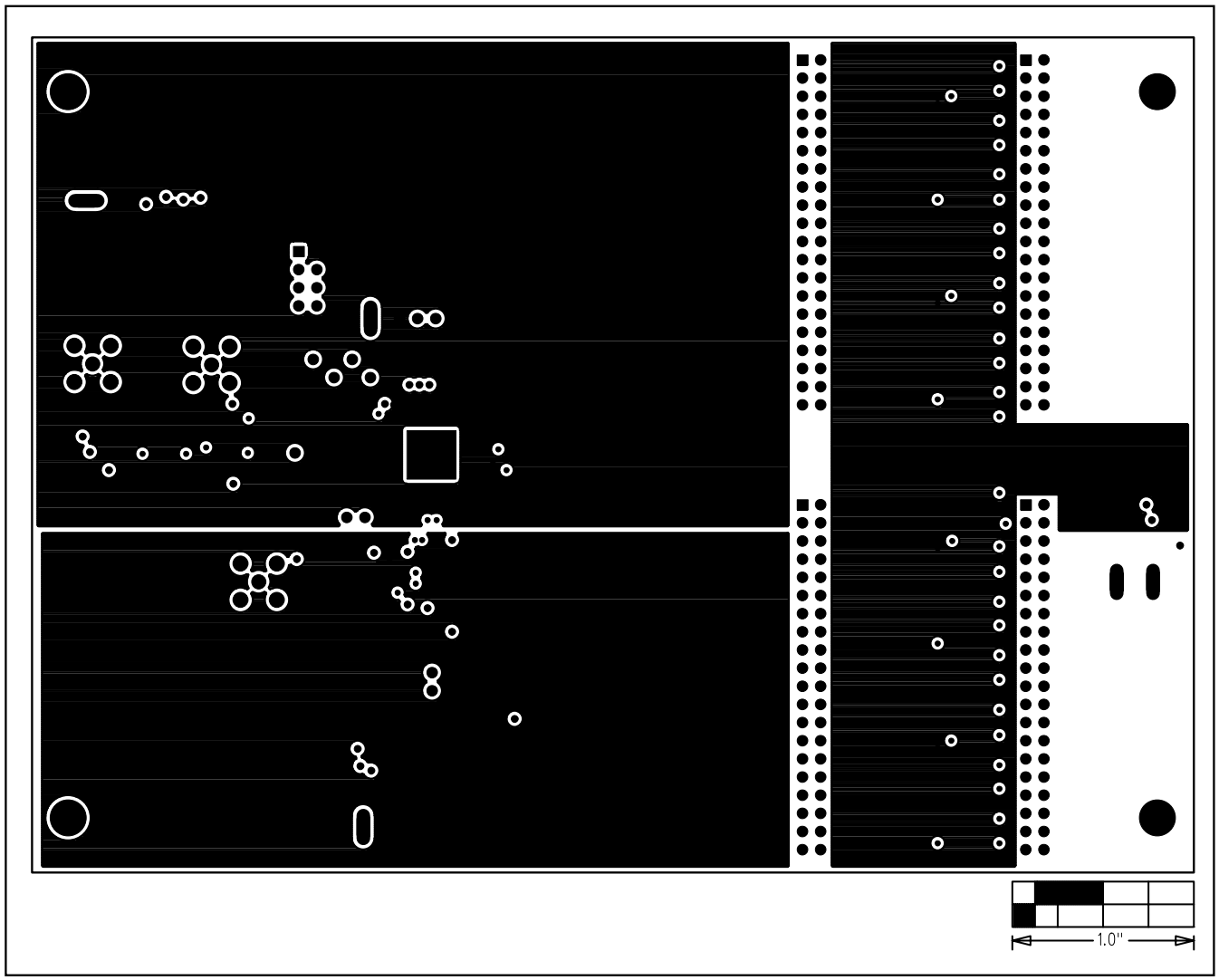

Figure 5. MAX1213/MAX1214/MAX1215 EV Kit PC Board Layout—Power Plane (Layer 3)

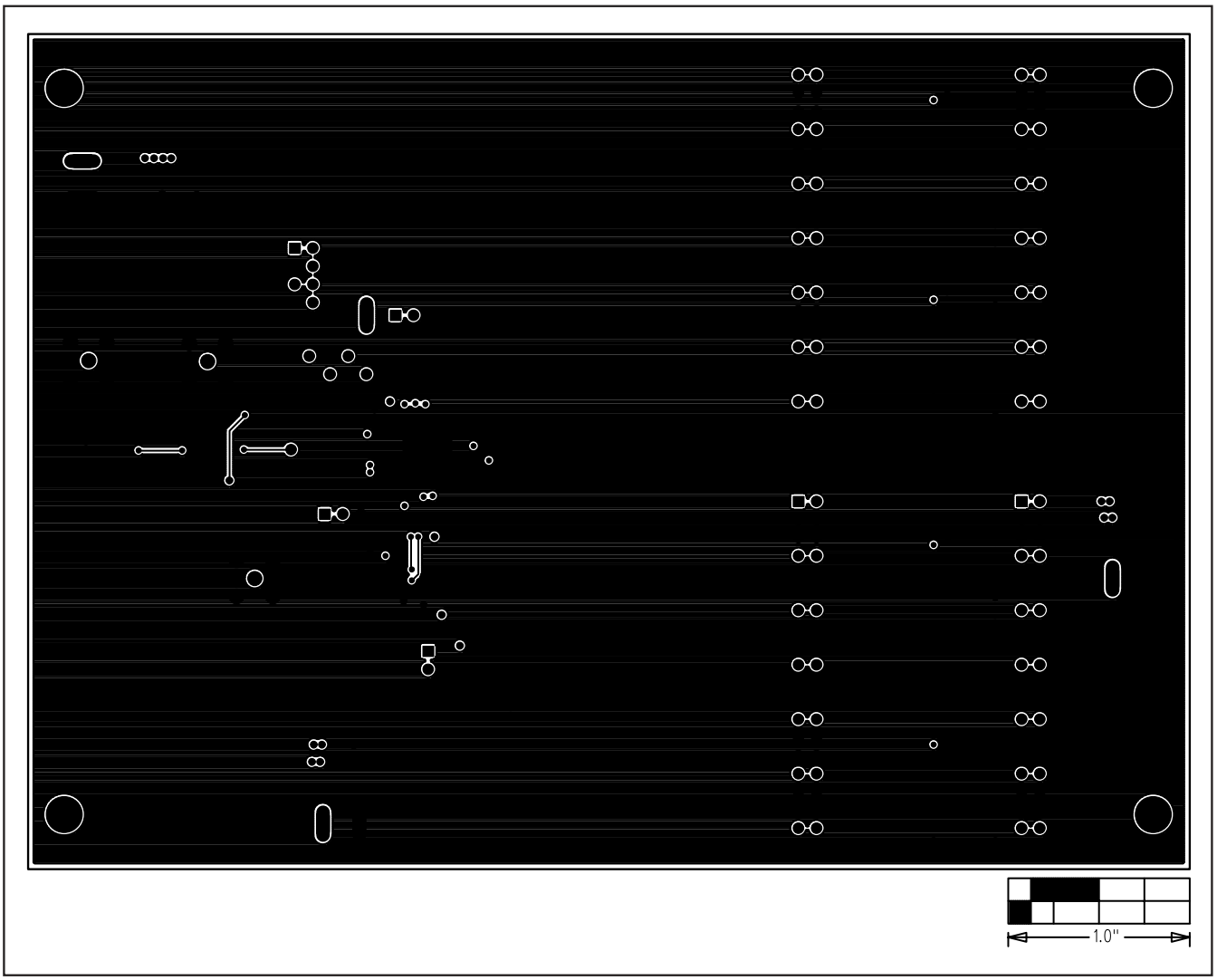

Figure 6. MAX1213/MAX1214/MAX1215 EV Kit PC Board Layout—Solder Side