CBTL06121

Gen1 hex display multiplexer

Rev. 2 — 26 October 2010 Product data sheet

1. General description

The CBTL06121 is a six-channel (‘hex’) multiplexer for DisplayPort and PCI Express applications at Generation 1 (‘Gen1’) speeds. It provides four differential channels capable of switching or multiplexing (bidirectional and AC-coupled) PCI Express or DisplayPort signals, using high-bandwidth pass-gate technology. Additionally, it provides for switching/multiplexing of the Hot Plug Detect signal as well as the AUX or DDC (Direct Display Control) signals, for a total of six channels.

The CBTL06121 is designed for Gen1 speeds, at 2.5 Gbit/s for PCI Express or 2.7 Gbit/s for DisplayPort. The device is available in two different pinouts (A and B, orderable as separate part numbers) to suit different motherboard layout requirements.

The typical application of CBTL06121 is on motherboards, docking stations or add-in cards where the graphics and I/O system controller chip utilizes I/O pins that are configurable for either PCI Express or DisplayPort operation. The hex display MUX can be used in such applications to route the signal from the controller chip to either a physical DisplayPort connector or a PCI Express connector using its 1 : 2 multiplexer topology. The controller chip selects which path to use by setting a select signal (which can be latched) HIGH or LOW.

Optionally, the hex MUX device can be used in conjunction with an HDMI/DVI level shifter device (PTN3300A, PTN3300B or PTN3301) to allow for DisplayPort as well as HDMI/DVI connectivity.

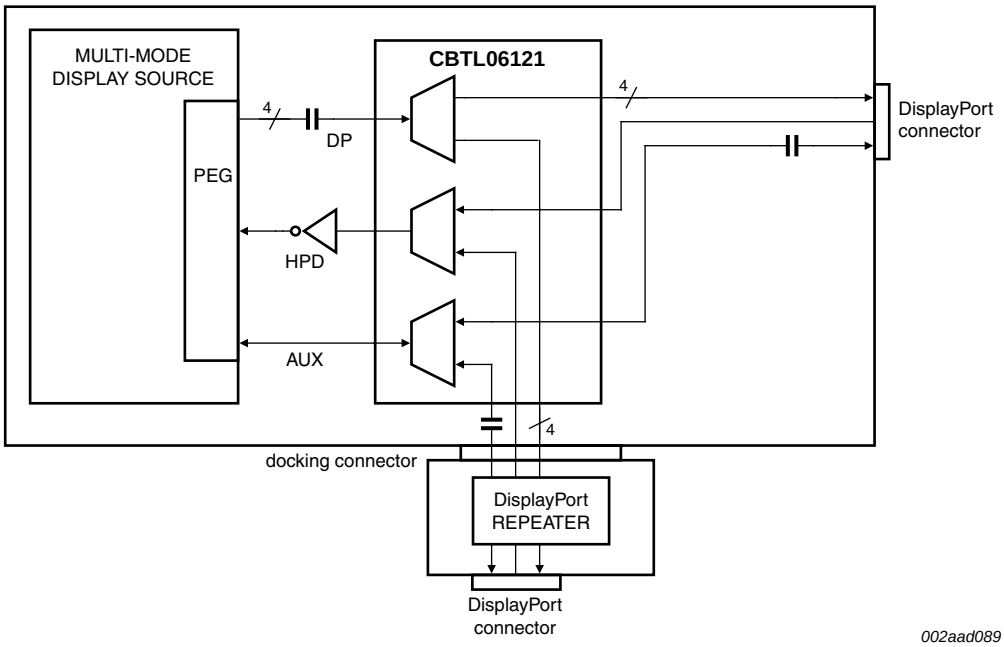


Fig 1. Intended usage 1: DisplayPort docking solution for mobile platform

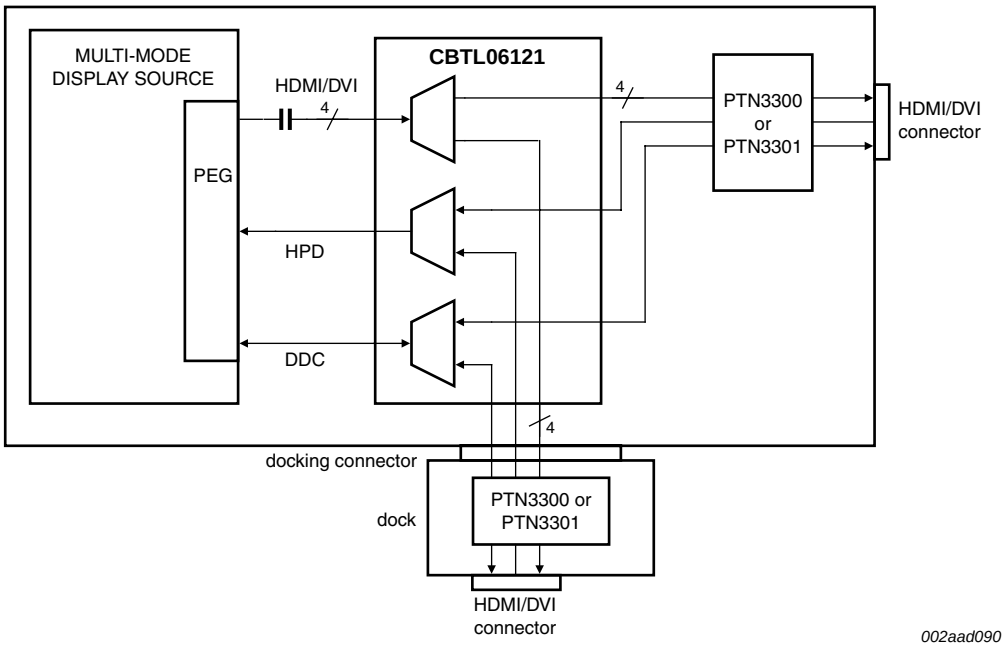


Fig 2. Intended usage 2: HDMI/DVI docking solution for mobile platform

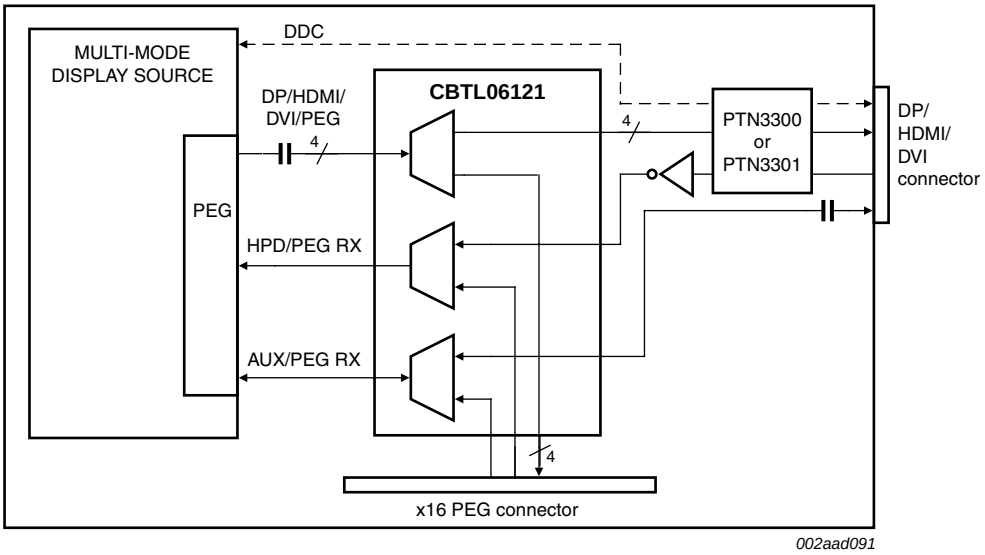


Fig 3. Intended usage 3: Digital display + external graphics solution for desktop platform

2. Features and benefits

- 1 : 2 multiplexing of DisplayPort (v1.1 - 2.7 Gbit/s) or PCI Express (v1.1 - 2.5 Gbit/s) signals
  - 4 high-speed differential channels
  - 1 channel for AUX differential signals or DDC clock and data
  - 1 channel for HPD
- High-bandwidth analog pass-gate technology
- Very low intra-pair differential skew (< 5 ps)
- Very low inter-pair skew (< 180 ps)
- All path delays matched including between RX1− to X− and RX1+ to X+
- Switch/MUX position select with latch function
- Shutdown mode CMOS input
- Shutdown mode minimizes power consumption while switching all channels off
- Very low operation current of 0.2 mA typ
- Very low shutdown current of < 10 μA
- Standby mode minimizes power consumption while switching all channels off
- Single 3.3 V power supply
- ESD 8 kV HBM, 1 kV CDM
- Two pinouts (A and B) available as separate ordering part numbers
- Available in 11 mm × 5 mm HWQFN56R package

3. Applications

- Motherboard applications requiring DisplayPort and PCI Express switching/multiplexing
- Docking stations
- Notebook computers
- Chip sets requiring flexible allocation of PCI Express or DisplayPort I/O pins to board connectors

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBTL06121AHF[1][2]	HWQFN56R	plastic thermal enhanced very very thin quad flat package; no leads; 56 terminals; resin based; body 11 × 5 × 0.7 mm[3]	SOT1033-1
CBTL06121BHF[1][2]			

[1] The A and B suffix in the part number correspond to the A and B pinouts, respectively (see Figure 5 and Figure 6).

[2] HF is the package designator for the HWQFN package.

[3] Total height after printed circuit board mounting = 0.8 mm (max.).

5. Functional diagram

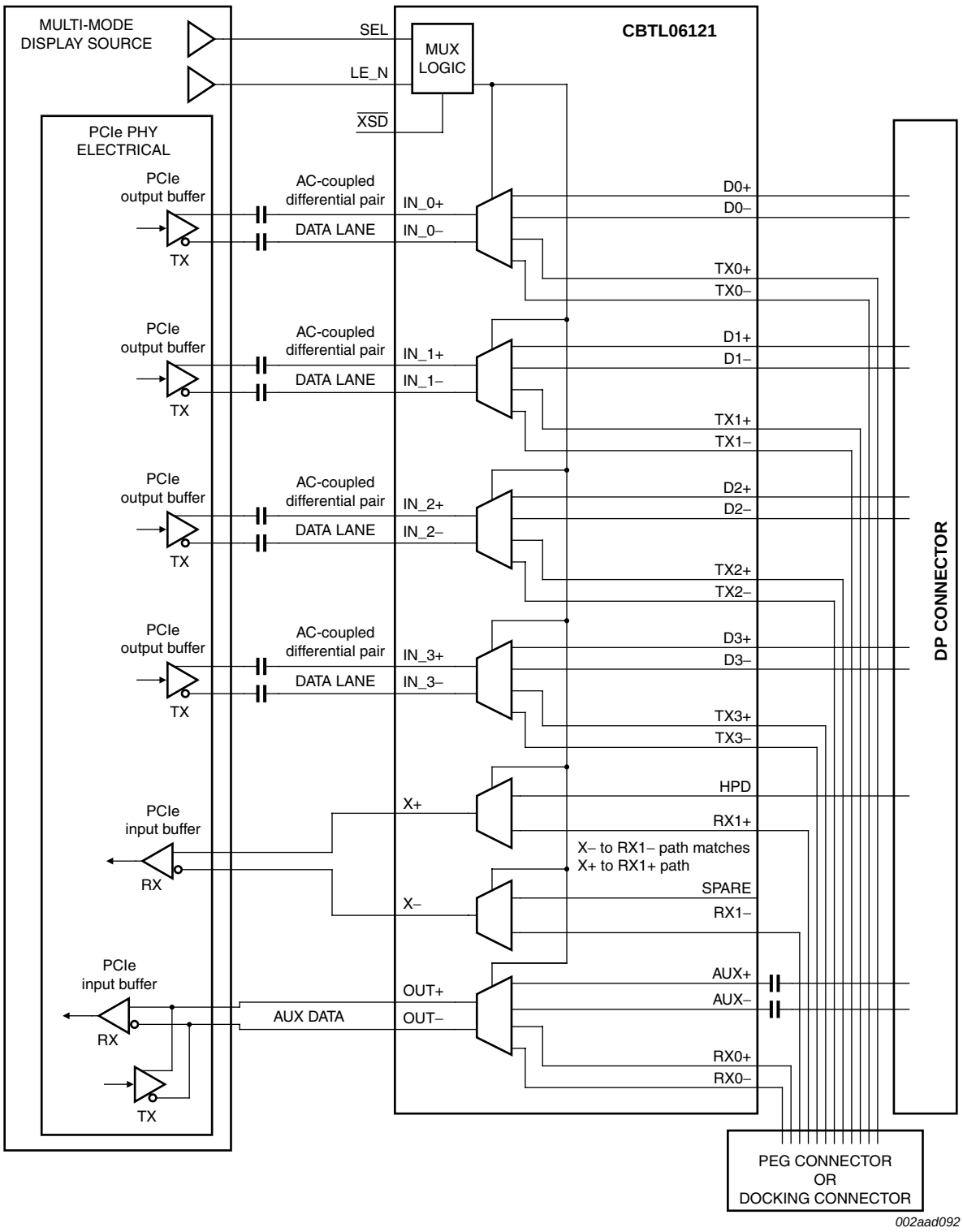


Fig 4. Functional diagram

6. Pinning information

6.1 Pinning

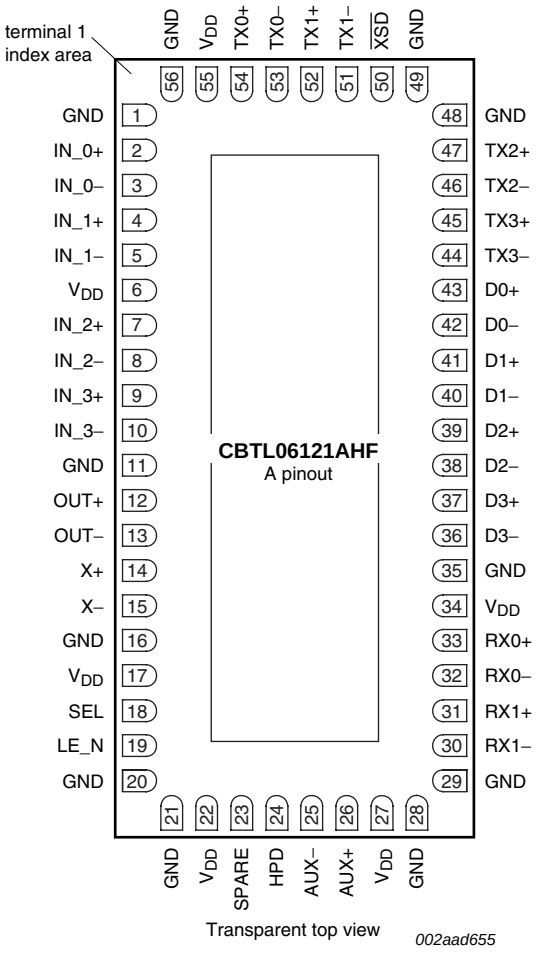


Fig 5. Pin configuration for HWQFN56R, A pinout

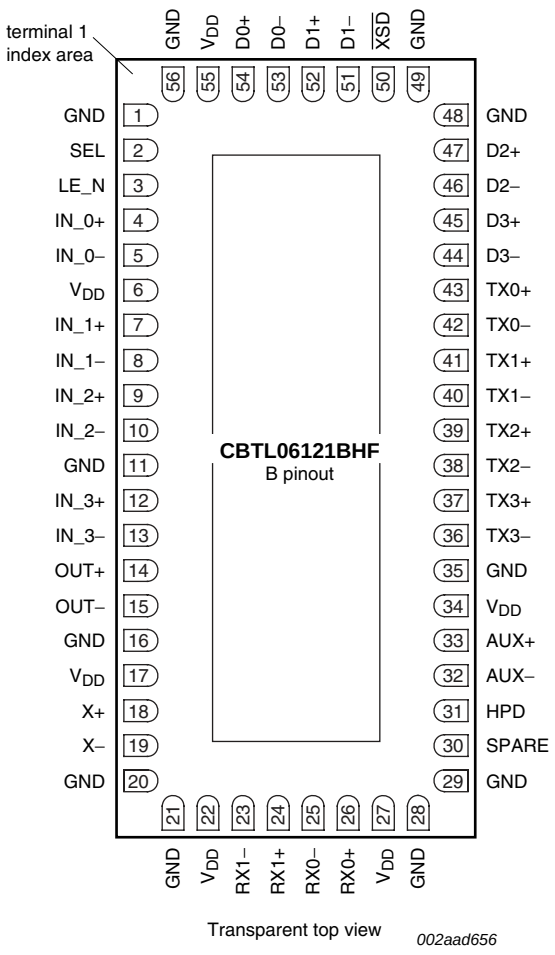


Fig 6. Pin configuration for HWQFN56R, B pinout

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	Pinout A	Pinout B		
SEL	18	2	3.3 V low-voltage CMOS single-ended input	SEL controls the MUX through a flow-through latch.
LE_N	19	3	3.3 V low-voltage CMOS single-ended input	The latch gate is controlled by LE_N.
$\overline{XSD}$	50	50	3.3 V low-voltage CMOS single-ended input	Optional shutdown pin. Should be driven HIGH or connected to V_{DD} for normal operation. When LOW, all paths are switched off (non-conducting) and supply current consumption is minimized.
RX0+	33	26	differential input	Differential input from PCIe connector or device. RX0+ makes a differential pair with RX0−. RX0+ is passed through to the OUT+ pin when SEL = 0.
RX0−	32	25	differential input	Differential input from PCIe connector or device. RX0− makes a differential pair with RX0+. RX0− is passed through to the OUT− pin when SEL = 0.
RX1+	31	24	differential input	Differential input from PCIe connector or device. RX1+ makes a differential pair with RX1−. RX1+ is passed through to the X+ pin when SEL = 0.
RX1−	30	23	differential input	Differential input from PCIe connector or device. RX1− makes a differential pair with RX1+. RX1− is passed through to the X− pin on a path that matches the RX1+ to X+ path.
IN_0+	2	4	differential input	Differential input from display source PCIe outputs. IN_0+ makes a differential pair with IN_0−.
IN_0−	3	5	differential input	Differential input from display source PCIe outputs. IN_0− makes a differential pair with IN_0+.
IN_1+	4	7	differential input	Differential input from display source PCIe outputs. IN_1+ makes a differential pair with IN_1−.
IN_1−	5	8	differential input	Differential input from display source PCIe outputs. IN_1− makes a differential pair with IN_1+.
IN_2+	7	9	differential input	Differential input from display source PCIe outputs. IN_2+ makes a differential pair with IN_2−.
IN_2−	8	10	differential input	Differential input from display source PCIe outputs. IN_2− makes a differential pair with IN_2+.
IN_3+	9	12	differential input	Differential input from display source PCIe outputs. IN_3+ makes a differential pair with IN_3−.
IN_3−	10	13	differential input	Differential input from display source PCIe outputs. IN_3− makes a differential pair with IN_3+.
HPD	24	31	high-voltage single-ended input	Low frequency, 0 V to 5 V/3.3 V (nominal) input signal. This signal comes from the HDMI/DP connector. Voltage HIGH indicates a ‘plugged’ state; voltage LOW indicates ‘unplugged’.
X+	14	18	(SEL = HIGH); HPD: high-voltage single-ended input	Low frequency, 0 V to 5 V/3.3 V (nominal) input signal. This signal comes from the HDMI/DP connector.
			(SEL = LOW); X+: pass-through output	Analog ‘pass-through’ output corresponding to RX1+.

Table 2. Pin description *...continued*

Symbol	Pin		Type	Description
	Pinout A	Pinout B		
X–	15	19	pass-through output from RX1– input	X– is an analog 'pass-through' output corresponding to the RX1– input. The path from RX1– to X– is matched with the path from RX1+ to X+. X+ and X– form a differential pair when the pass-through MUX mode is selected.
D0+	43	54	pass-through output 1, option 1	Analog 'pass-through' output 1 corresponding to IN_0+ and IN_0–, when SEL = 1.
D0–	42	53		
D1+	41	52	pass-through output 2, option 1	Analog 'pass-through' output 1 corresponding to IN_1+ and IN_1–, when SEL = 1.
D1–	40	51		
D2+	39	47	pass-through output 3, option 1	Analog 'pass-through' output 1 corresponding to IN_2+ and IN_2–, when SEL = 1.
D2–	38	46		
D3+	37	45	pass-through output 4, option 1	Analog 'pass-through' output 1 corresponding to IN_3+ and IN_3–, when SEL = 1.
D3–	36	44		
TX0+	54	43	pass-through output 1, option 2	Analog 'pass-through' output 2 corresponding to IN_0+ and IN_0–, when SEL = 0.
TX0–	53	42		
TX1+	52	41	pass-through output 2, option 2	Analog 'pass-through' output 2 corresponding to IN_1+ and IN_1–, when SEL = 0.
TX1–	51	40		
TX2+	47	39	pass-through output 3, option 2	Analog 'pass-through' output 2 corresponding to IN_2+ and IN_2–, when SEL = 0.
TX2–	46	38		
TX3+	45	37	pass-through output 4, option 2	Analog 'pass-through' output 2 corresponding to IN_3+ and IN_3–, when SEL = 0.
TX3–	44	36		
V_{DD}	6, 17, 22, 27, 34, 55	6, 17, 22, 27, 34, 55	3.3 V supply	Supply voltage (3.3 V ± 10 %).
AUX+	26	33	differential input	High-speed differential pair for AUX signals.
AUX–	25	32	differential input	
OUT+	12	14	differential input	High-speed differential pair for PCIe RX0+ signal.
OUT–	13	15	differential input	High-speed differential pair for PCIe RX0– signal.
GND[1]	1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	supply ground	Ground.
SPARE	23	30	single-ended input	Spare channel for general-purpose switch use. Connected to pin X– when SEL = 1.

[1] HWQFN56R package die supply ground is connected to both GND pins and exposed center pad. GND pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 4 “Functional diagram”.

The CBTL06121 uses 3.3 V power supply. All signal paths are implemented using high-bandwidth pass-gate technology, are bidirectional and no clock or reset signal is needed for the multiplexer to function.

The switch position is selected using the select signal (SEL), which can be latched using the latch enable pin (LE_N). The detailed operation is described in Section 7.1.

7.1 MUX select (SEL) function

The internal multiplexer switch position is controlled by two logic inputs SEL and LE_N as described below.

Table 3. MUX select control

SEL	Dx	TXx; RXx
0	high-impedance	active; follows IN_x
1	active; follows IN_x	high-impedance

The switch position select input signal SEL controls the MUX through a flow-through latch, which is gated by the latch enable input signal LE_N (active LOW). The latch is open when LE_N is LOW; in this state the internal switch position will respond to the state of the SEL input signal. The latch is closed when LE_N is HIGH, and the switch position will not respond to input state changes on the SEL input.

Table 4. MUX select latch control

LE_N	Internal MUX select
0	responds to changes on SEL
1	latched

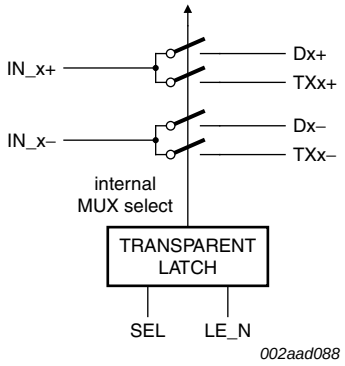


Fig 7. MUX select function

7.2 Shutdown function

The CBTL06121 provides a shutdown function to minimize power consumption when the application is not active but power to the CBTL06121 is provided. Pin $\overline{XSD}$ (active LOW) puts all channels in off mode (non-conducting) while reducing current consumption to near-zero.

Table 5. Shutdown function

$\overline{XSD}$	State
0	shutdown
1	active

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.3	+5	V
T_{case}	case temperature	for operation within specification		−40	+85	°C
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	8000	V
		CDM	[2]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	input voltage		-	-	3.6	V
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

10. Characteristics

10.1 General characteristics

Table 8. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	operating mode ($\overline{XSD}$ = HIGH); V_{DD} = 3.3 V	-	0.2	1	mA
		shutdown mode ($\overline{XSD}$ = LOW); V_{DD} = 3.3 V	-	-	10	μA
P_{tot}	total power consumption	operating mode ($\overline{XSD}$ = HIGH); V_{DD} = 3.3 V	-	-	5	mW
$t_{startup}$	start-up time	supply voltage valid or $\overline{XSD}$ going HIGH to channel specified operating characteristics	-	-	1	ms
t_{rcfg}	reconfiguration time	SEL state change to channel specified operating characteristics	-	-	1	ms

10.2 DisplayPort channel characteristics

Table 9. DisplayPort channel characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		−0.3	-	+2.6	V
V_{IC}	common-mode input voltage		0	-	2.0	V
V_{ID}	differential input voltage		−1.2	-	+1.2	V
DDIL	differential insertion loss	channel is on; 0 Hz ≤ f ≤ 1.0 GHz	−2.5	−1.6	-	dB
		channel is on; f = 2.5 GHz	−4.5	-	-	dB
		channel is off; 0 Hz ≤ f ≤ 3.0 GHz	-	-	−20	dB
DDRL	differential return loss	channel is on; 0 Hz ≤ f ≤ 1.0 GHz	-	-	−10	dB
DDNEXT	differential near-end crosstalk	adjacent channels are on; 0 Hz ≤ f ≤ 1.0 GHz	-	-	−30	dB
B	bandwidth	−3.0 dB intercept	-	2.5	-	GHz
t_{PD}	propagation delay	from left-side port to right-side port or vice versa	-	180	-	ps
$t_{sk(dif)}$	differential skew time	intra-pair	-	-	5	ps
t_{sk}	skew time	inter-pair	-	-	180	ps

10.3 AUX and DDC ports

Table 10. AUX and DDC port characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage	DDC or AUX		−0.3	-	+2.6	V
V_{IC}	common-mode input voltage	DDC or AUX		0	-	2.0	V
V_{ID}	differential input voltage			−1.2	-	+1.2	V
t_{PD}	propagation delay	from left-side port to right-side port or vice versa	[1]	-	180	-	ps

[1] Time from DDC/AUX input changing state to AUX output changing state. Includes DDC/AUX rise/fall time.

10.4 HPD input, HPD output

Table 11. HPD input and output characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_I	input voltage		[1]	−0.3	-	3.6	V
t_{PD}	propagation delay	from HPD_SINK to HPD_SOURCE	[2]	-	180	-	ps

[1] Low-speed input changes state on cable plug/unplug.

[2] Time from HPD_IN changing state to HPD changing state. Includes HPD rise/fall time.

10.5 MUX select and latch input

Table 12. SEL, LE_N input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	3.6	V
V_{IL}	LOW-level input voltage		0	-	0.8	V
I_{LI}	input leakage current	measured with input at $V_{IH(max)}$ and $V_{IL(min)}$	-	-	10	μA

11. Test information

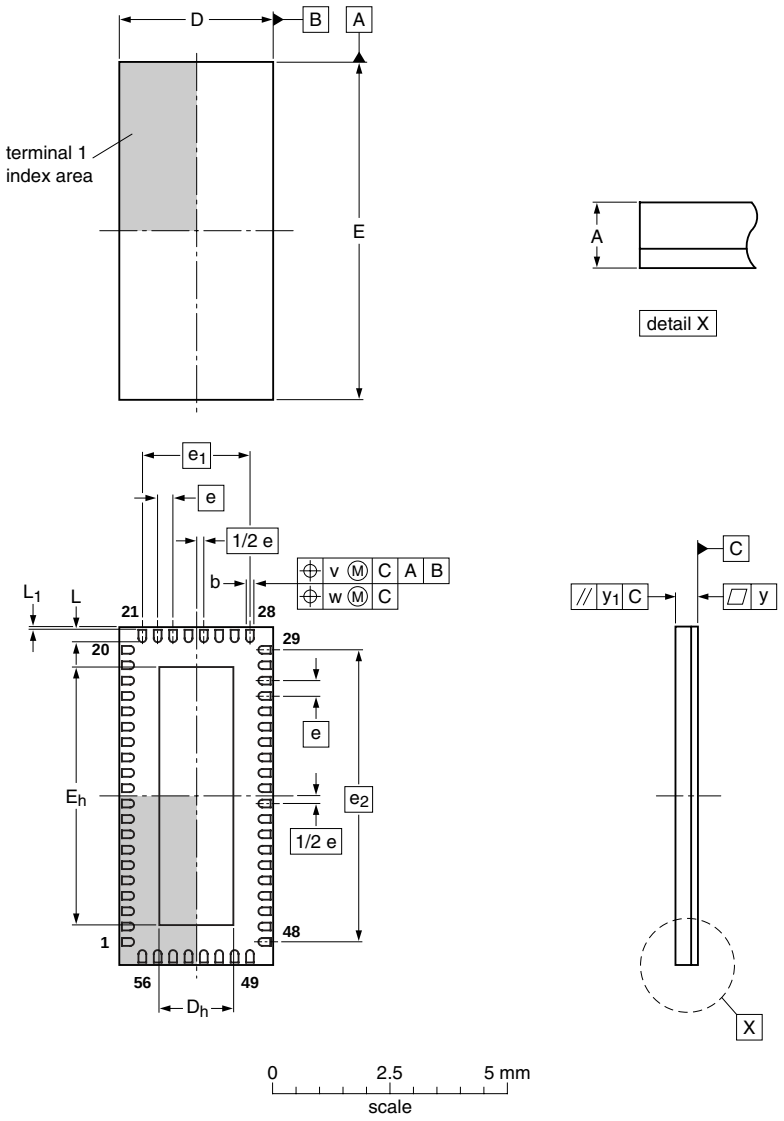
11.1 Switch test fixture requirements

The test fixture for switch S-parameter measurement shall be designed and built to specific requirements, as described below, to ensure good measurement quality and consistency.

- The test fixture shall be a FR4-based PCB of the microstrip structure; the dielectric thickness or stack-up shall be about 4 mils.
- The total thickness of the test fixture PCB shall be 1.57 mm (0.62 in).
- The measurement signals shall be launched into the switch from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the DUT and measurement ports (SMA or microprobe) should be uncoupled from each other, as much as possible. Therefore, the traces should be routed in such a way that traces will diverge from each other exiting from the switch pin field.
- The trace lengths between the DUT and measurement port shall be minimized. The maximum trace length shall not exceed 1000 mils. The trace lengths between the DUT and measurement port shall be equal.
- All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ω with a tolerance of ±7 %.
- SMA connector is recommended for ease of use. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60 ps rise time should be within 50 Ω ± 7 Ω.

12. Package outline

HWQFN56R: plastic thermal enhanced very very thin quad flat package; no leads; 56 terminals; resin based; body 11 x 5 x 0.7 mm **SOT1033-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	b	D	D_h	E	E_h	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	0.8	0.27 0.23	5.1 4.9	2.5 2.3	11.1 10.9	8.5 8.3	0.5	3.5	9.5	0.42 0.38	0.1 0.0	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1033-1	- - -	- - -	- - -			~~07-09-19~~ 07-12-01

Fig 8. Package outline HWQFN56R (SOT1033-1)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020C)

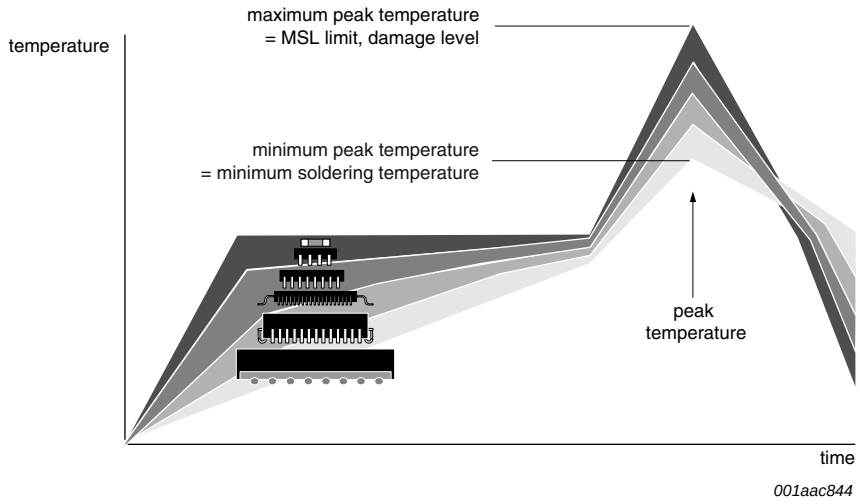
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
AUX	Auxiliary channel in DisplayPort definition
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DDC	Direct Display Control
DP	DisplayPort
DUT	Device Under Test
DVI	Digital Video Interface
ESD	ElectroStatic Discharge
HBM	Human Body Model
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I/O	Input/Output
MUX	Multiplexer
PCB	Printed-Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PEG	PCI Express Graphics
SMA	SubMiniature, version A (connector)
TDR	Time-Domain Reflectometry

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL06121 v.2	20101026	Product data sheet	-	CBTL06121 v.1
Modifications:	• Table 9 row B (bandwidth): typical value corrected from 25 to 2.5			
CBTL06121 v.1	20080523	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

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Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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Date of release: 26 October 2010
Document identifier: CBTL06121