4-pin active bridge daughter card

Line rectifier module featuring 600 V CoolMOS™ S7

Order code: KIT_ACT_BRD_S7_4PIN

About this document

Scope and purpose

This document describes the design and operation of a complete Infineon Technologies AG system solution for active line rectification based on a 600 V CoolMOS™ S7, aiming to replace the diode bridge in standard power factor correction (PFC) converters.

Use of the 600 V CoolMOS™ S7 active bridge daughter card boosts the PFC efficiency more than 1 percent at low-line levels (115 V AC) and up to 0.7 percent at high-line (230 V AC) without any impact on system design.

The active bridge daughter cards are available in the following variants:

- KIT_ACT_BRD_S7_4PIN, mounting 22 mΩ CoolMOS™ S7 with four pins only
- KIT_ACT_BRD_60R022S7, mounting 22 mΩ CoolMOS™ S7 with five pins **[1]**
- KIT_ACT_BRD_60R040S7, mounting 40 mΩ CoolMOS™ S7 with five pins **[2]**
- KIT_ACT_BRD_60R065S7, mounting 65 mΩ CoolMOS™ S7 with five pins **[3]**

The main Infineon components used in the **KIT_ACT_BRD_S7_4PIN** are described in the following:

Kit components:

- **600 V CoolMOS™ S7 superjunction MOSFET** (IPT60R022S7)

Kit specifications:

- Input voltage: from 85 to 265 V AC
- CoolMOS™ S7 $R_{DS(on)}$: 22 mΩ
- No need for supply voltage

Intended audience

This document is intended for power supply design engineers.

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1 Introduction

In recent years, the trend for SMPS has been toward increasing both efficiency and power density with optimized cost.

A variety of efficiency requirements, such as 80 PLUS or EuP, are defined for various SMPS. In the platinum class the PSU must have a peak efficiency above 94 percent at high-line and 92 percent at low-line, while for a titanium design these values increase to 96 percent and 94 percent, respectively. In addition, some customers may define stricter efficiency requirements based on system operating conditions.

It is obvious that the overall efficiency of the PSU depends on both efficiency levels of the PFC and of the DC-DC stages. For a fixed efficiency target of the PSU, if we are able to increase PFC performance then we can relax the requirements of the DC-DC converter, and vice-versa. Of course, this will impact the overall cost of the system. The question for every PSU manufacturer would be: what is the optimum balance between the two stages?

An easy and effective way of improving the PFC efficiency performance across the whole load and voltage range, without affecting the design, complexity and PFC cost too much, is to simply replace the classic diode bridge with an active bridge made with the 600 V CoolMOS™ S7.

Figure 1 shows a comparison between the active bridge daughter card and a standard diode bridge. In terms of form factor the two solutions are comparable, while the active bridge needs one extra pin connection for the bias supply. More details about the board will be discussed in the next chapter.

In **Figure 2** the efficiency benefit of the **KIT_ACT_BRD_S7_4PIN** employed in a standard continuous conduction mode (CCM) PFC is presented both at low-line (115 V AC) and high-line (230 V AC) in terms of delta efficiency comparison with the diode bridge solution. The measurement is done by plugging the 22 mΩ daughter card into the Infineon active bridge PFC demo board **EVAL_2K4W_ACT_BRD_S7** [4]. The maximum output power is around 1200 W at low-line and 2400 W at high-line. An efficiency delta improvement of 1.3 percent and 0.7 percent can be seen at low-line and at high-line respectively under light-load conditions. The delta efficiency is halved at 50 percent of the output power.

The 22 mΩ active bridge gives an improvement above 0.4 percent at both low-line and high-line when the output power is below 2000 W, as shown by the green shaded zone of **Figure 2**.

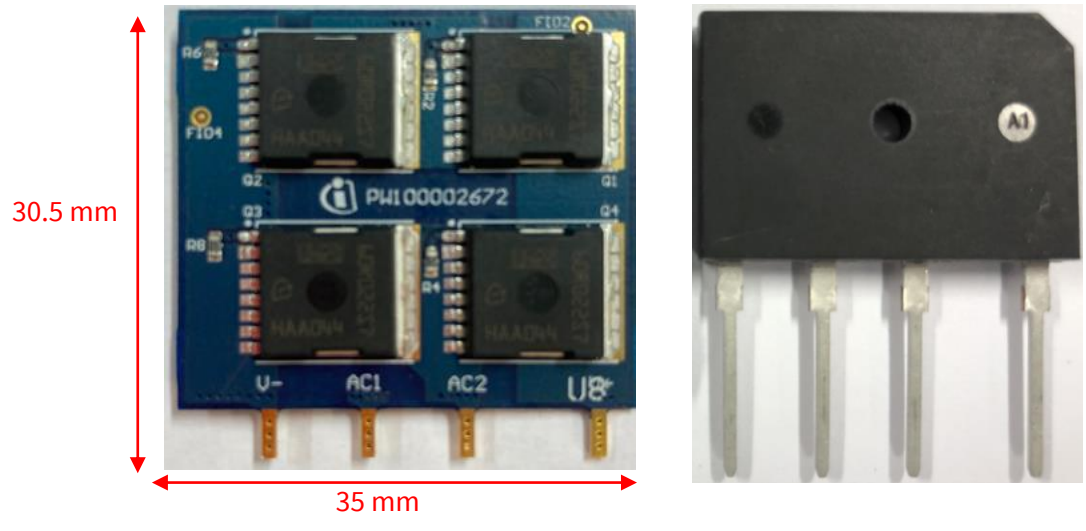


Figure 1 Active bridge daughter card (left) compared with a standard diode bridge (right)

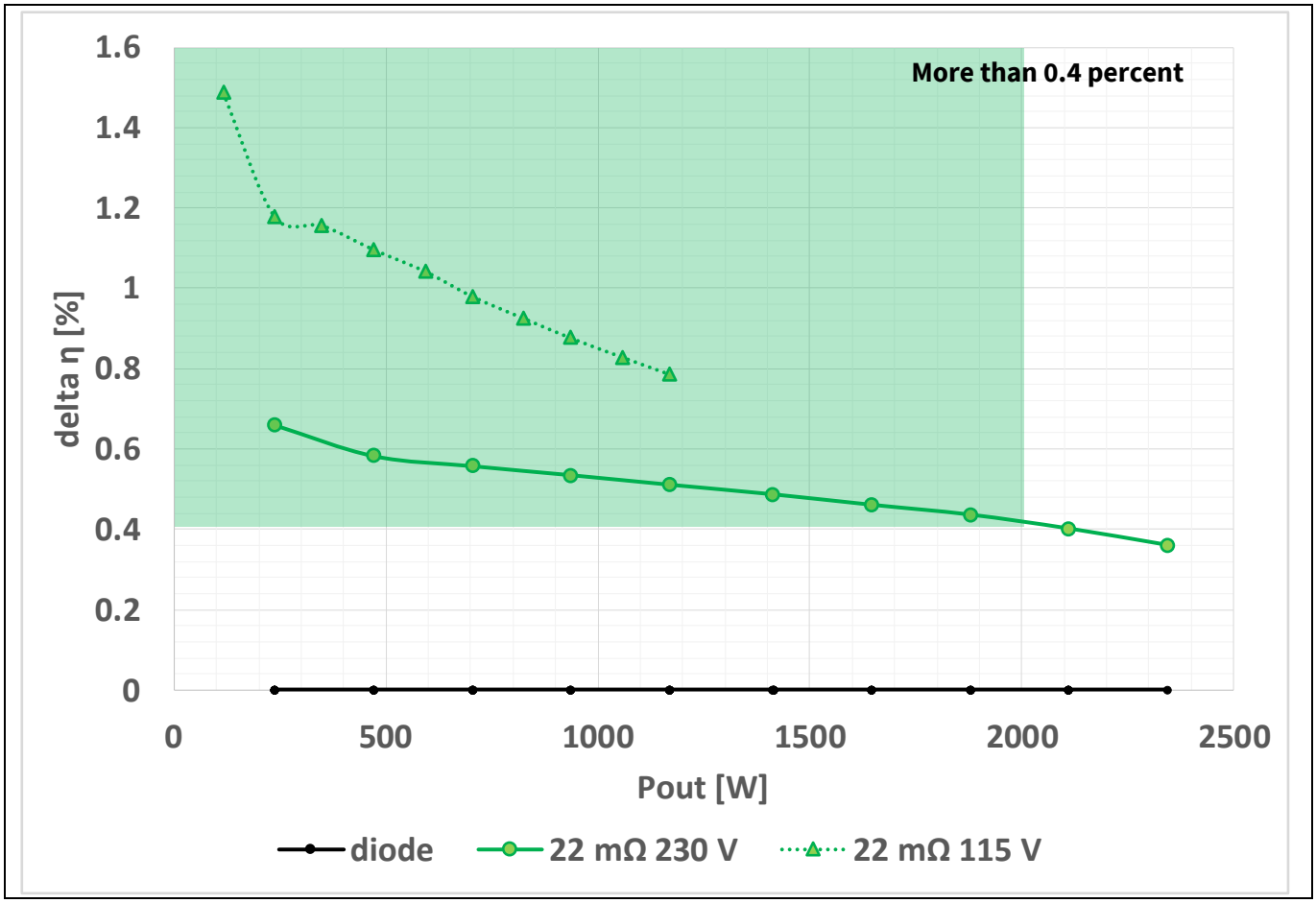


Figure 2 Efficiency improvement in CCM PFC with KIT_ACT_BRD_S7_4PIN

2 Kit overview

2.1 Hardware description

The active bridge daughter board is shown in **Figure 3**. The board is 35 mm long, with a width of 5 mm and a height of 30.5 mm, comparable to the size of a standard diode bridge rectifier (20 mm x 30 mm x 4.6 mm).

The daughter board has only four pins:

- Line (AC1) and neutral (AC2) alternate inputs
- Positive (V+) and negative (V-) rectified outputs

The bias supply voltage of 12 V is provided by the internal bias cell of the integrated controller/driver, so there is no need of an extra pin for it as implemented in the previous daughter cards **[1]** to **[3]**.

The daughter card integrates both power devices and control/driving components, thus enabling a high power density design. The power devices in TO-leadless (TOLL) packages are placed on the bottom side together with the gate resistors, as shown in **Figure 3b**. On the top side, the unique IC takes care of the control and driving of the high-side and low-side MOSFETs, as shown in **Figure 3a**. Additional components are: bootstrap R-C networks for high-side MOSFET driving, and a capacitor for the self-bias cell. More details about the control of the active bridge are discussed in the next section.

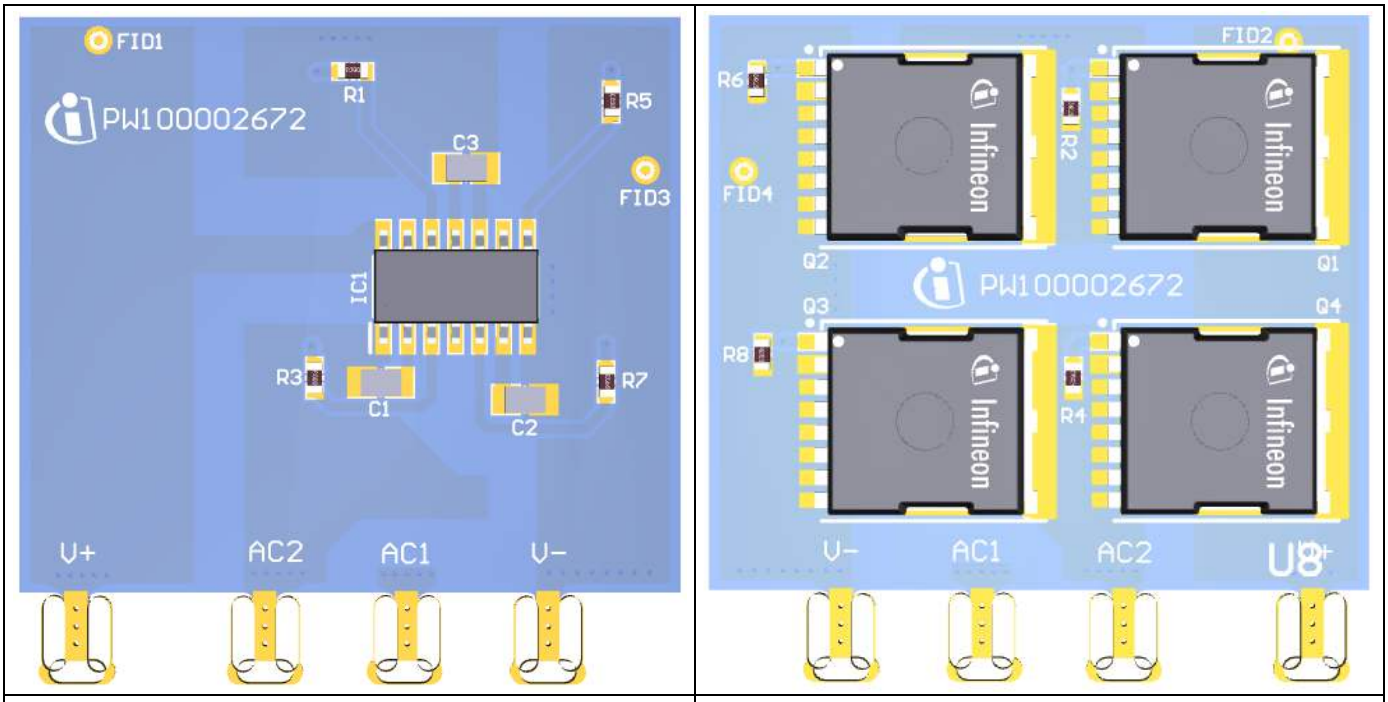


Figure 3 Placement of the different components in the active bridge daughter card with Infineon 600 V CoolMOS™ S7 MOSFET: a) top view and b) bottom view

2.2 Active bridge control method

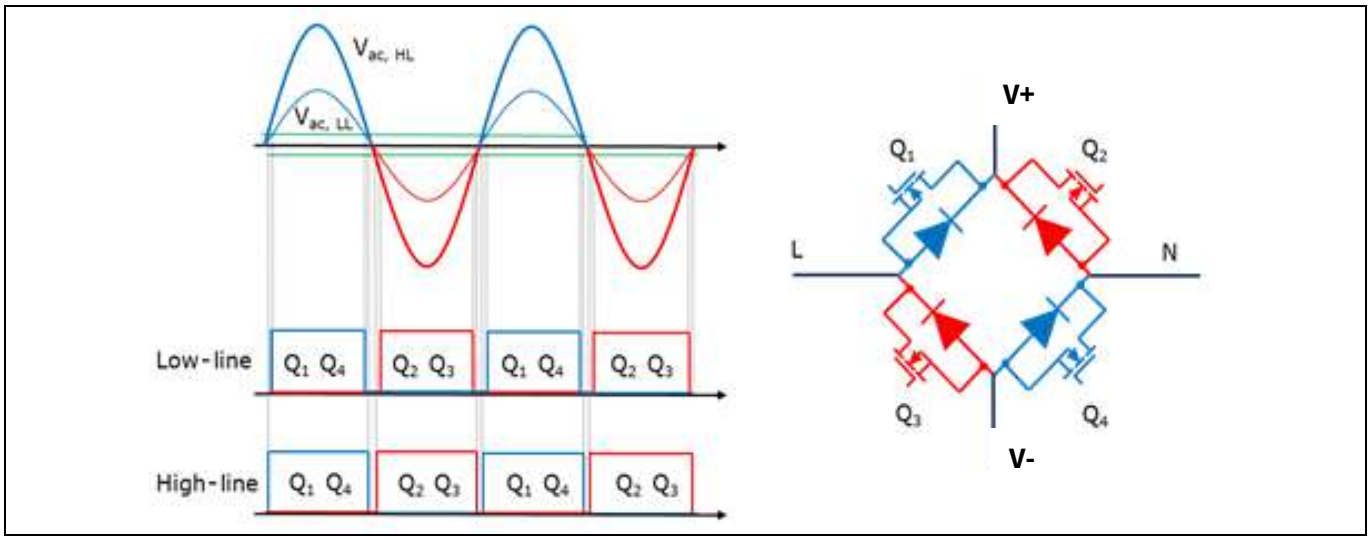


Figure 4 Control concept of the active bridge line rectification

Control of an active bridge for line rectification is intuitive. As shown in **Figure 4**, during the positive half-cycle of the mains, Q1 and Q4 are supposed to be switched on, while the others are kept off. Intead, during the negative half-cycle of the AC-grid, Q3 and Q2 are supposed to conduct, while the others are off.

It is important to highlight that all the MOSFETs are always conducting in the so-called "reverse mode" or "diode mode", with a positive current flowing from the source to the drain. In fact, the active bridge's purpose is to take over the conduction of the diode in order to achieve better efficiency, since MOSFET conduction losses are lower than those from diodes.

There are two possible ways of controlling the active bridge switches:

1. By measuring the input voltage V AC
2. By sensing the voltage drop across the MOSFET V_{DS}

In the *first method*, the control signal for each MOSFET of the active bridge is obtained by comparing the instantaneous input voltage (properly scaled down through a resistive divider) with a fixed reference voltage threshold. The voltage divider resistance should be high enough to minimize the quiescent loss, especially at high-line input. With this method, the on-time of the control signal at each cycle strongly depends on the input voltage level. This means that a shorter on-time is obtained at low-line input, and vice versa.

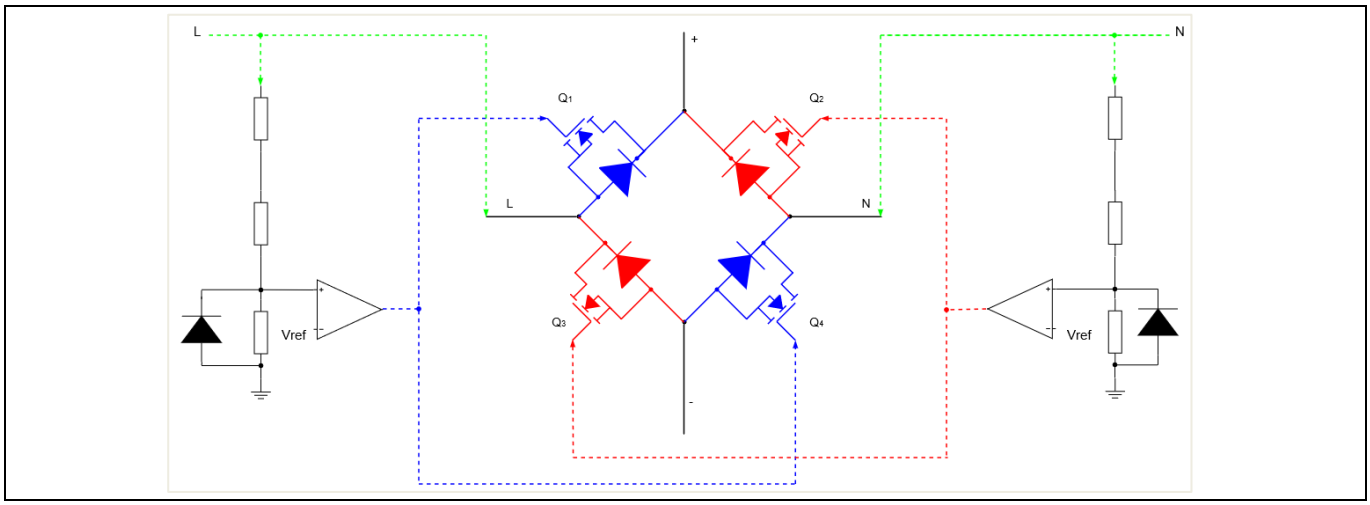


Figure 5 First control method based on measuring the input voltage

The first control method is implemented in the integrated controller of KIT_ACT_BRD_S7_4PIN.

The second approach exploits the information of the current flowing through each low-side MOSFET by sensing the V_{DS} across the MOSFETs. This method is commonly used in the secondary-side SR controllers. Such a solution is already available in the market and is widely used in high-efficiency step-down DC-DC converters, for example for driving the SR of an LLC resonant converter.

This *second method* is the one employed in the previous daughter cards **[1]** to **[3]**, using Infineon controller IR11688S.

The IR11688S is a dual smart secondary-side controller IC optimized to drive two N-channel power MOSFETs configured for synchronous rectification in resonant converter applications, with drain voltage sensing capability up to 200 V. Small-signal transistors T1 and T2 are added to further extend the voltage capability of the controller, matching the high-line PFC application.

The drain-to-source voltage of the low-voltage side MOSFET (Q3, Q4) of the active bridge is sensed through the VD1 and VD2 pins to determine the source-to-drain current and consequently turn on/off each gate rapidly at the start/end of each conduction cycle. The drain-to-source voltages are compared to different thresholds to precisely control the gates.

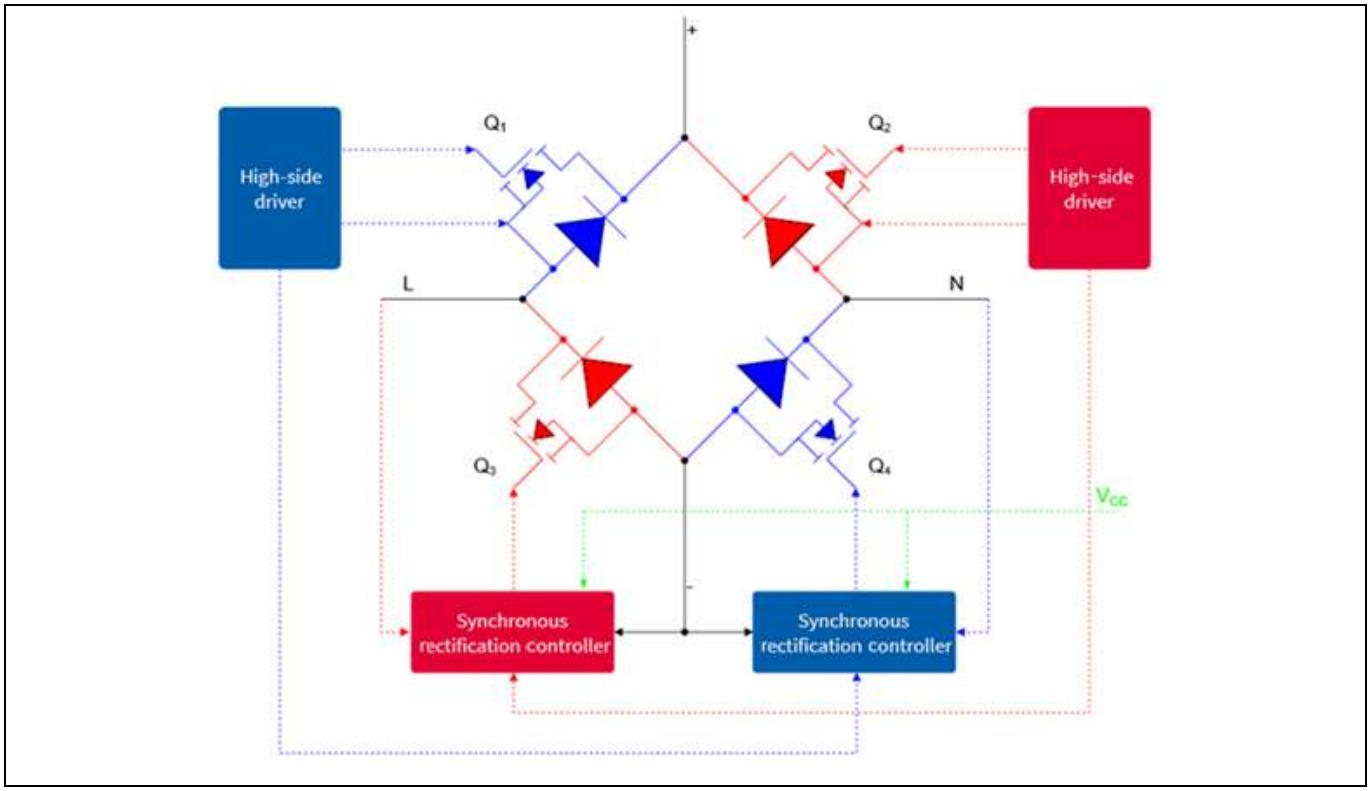


Figure 6 Second approach based on the SR controller

2.3 Board specification

Table 1 presents the specification of the active bridge board developed using the 600 V CoolMOS™ S7 in a TOLL package.

Table 1 Summary of specifications and test conditions for the active bridge daughter card

Parameter	Specification
Input voltage range	85 to 265 V_{RMS}
Nominal input voltage at low-line	115 V_{RMS}
Nominal input voltage at high-line	230 V_{RMS}
AC-line frequency range	45 to 65 Hz
Maximum ambient temperature	40°C
Maximum output power	2400 W (referenced to PFC board)
Self-bias voltage	12 V

3 Experimental results

3.1 Steady-state waveforms

Steady-state behavior of the active bridge daughter card is first tested in a standalone setup with the AC generator directly connected to the board pins AC1 and AC2 of **Figure 3**, and a resistive load of around 160 Ω attached to the output pins V+ and V-.

Figure 7 shows the steady-state waveforms of active bridge low-side complementary driving signals during PFC operation at high-line.

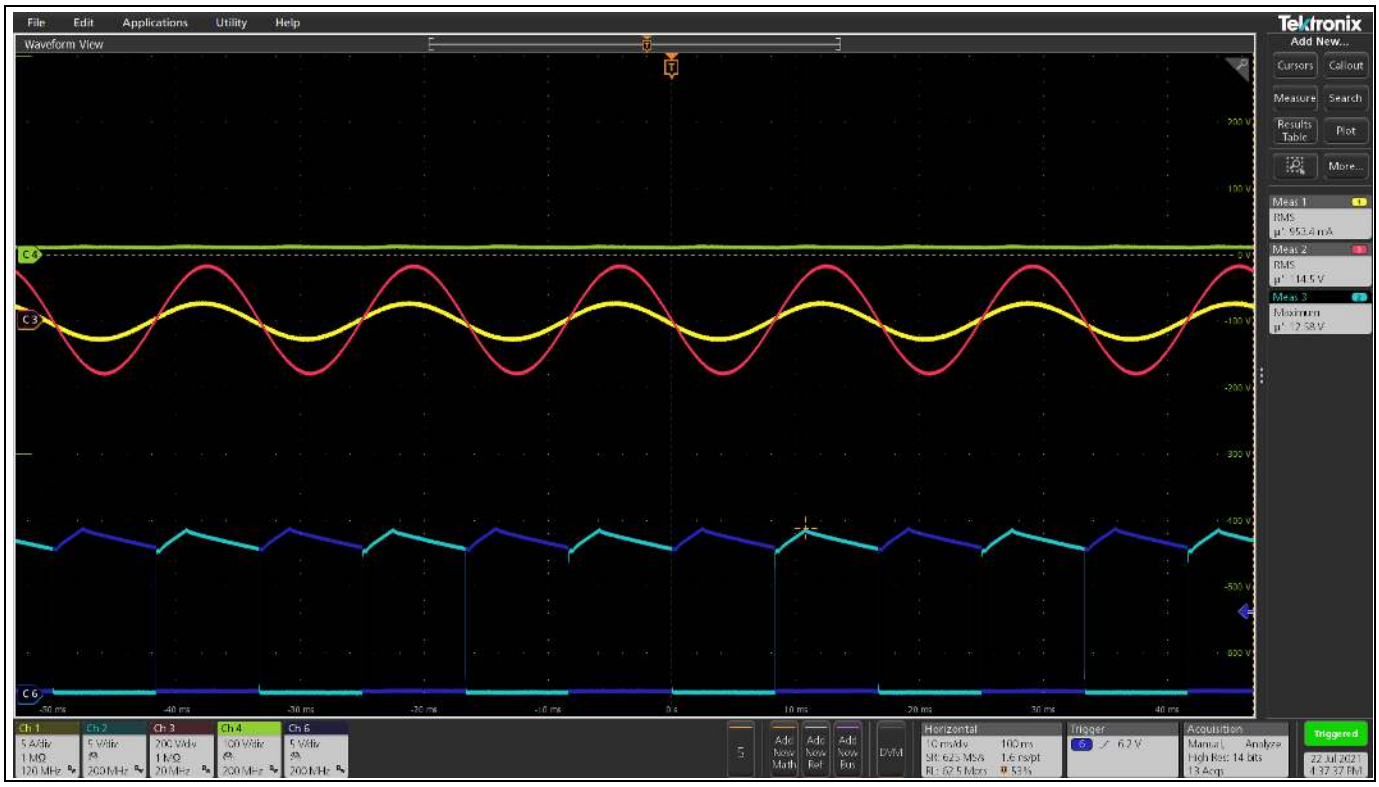


Figure 7 Steady-state waveforms of active bridge low-side complementary driving signals (dark blue and light blue lines), input current and voltage (magenta and yellow lines) and PFC output voltgage (green line) at 115 V AC

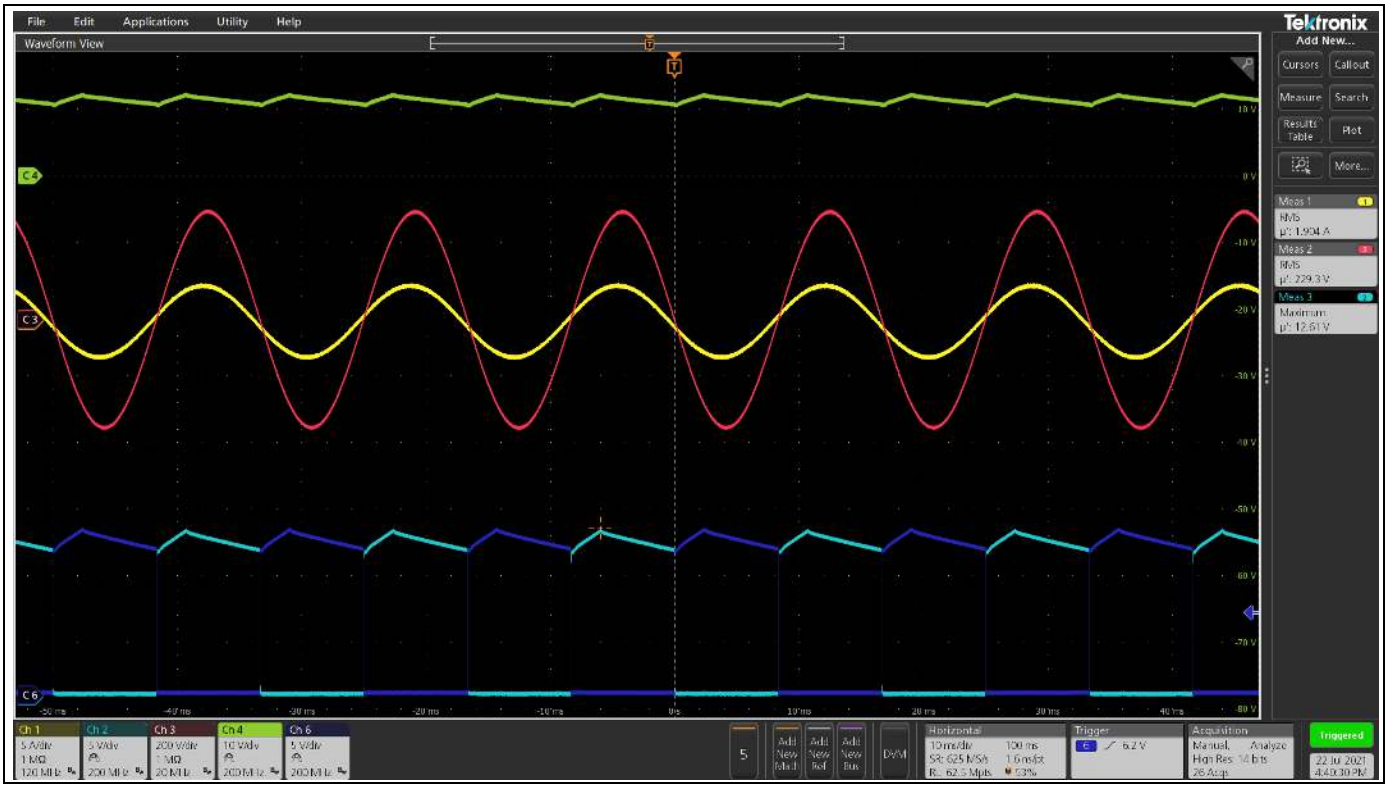


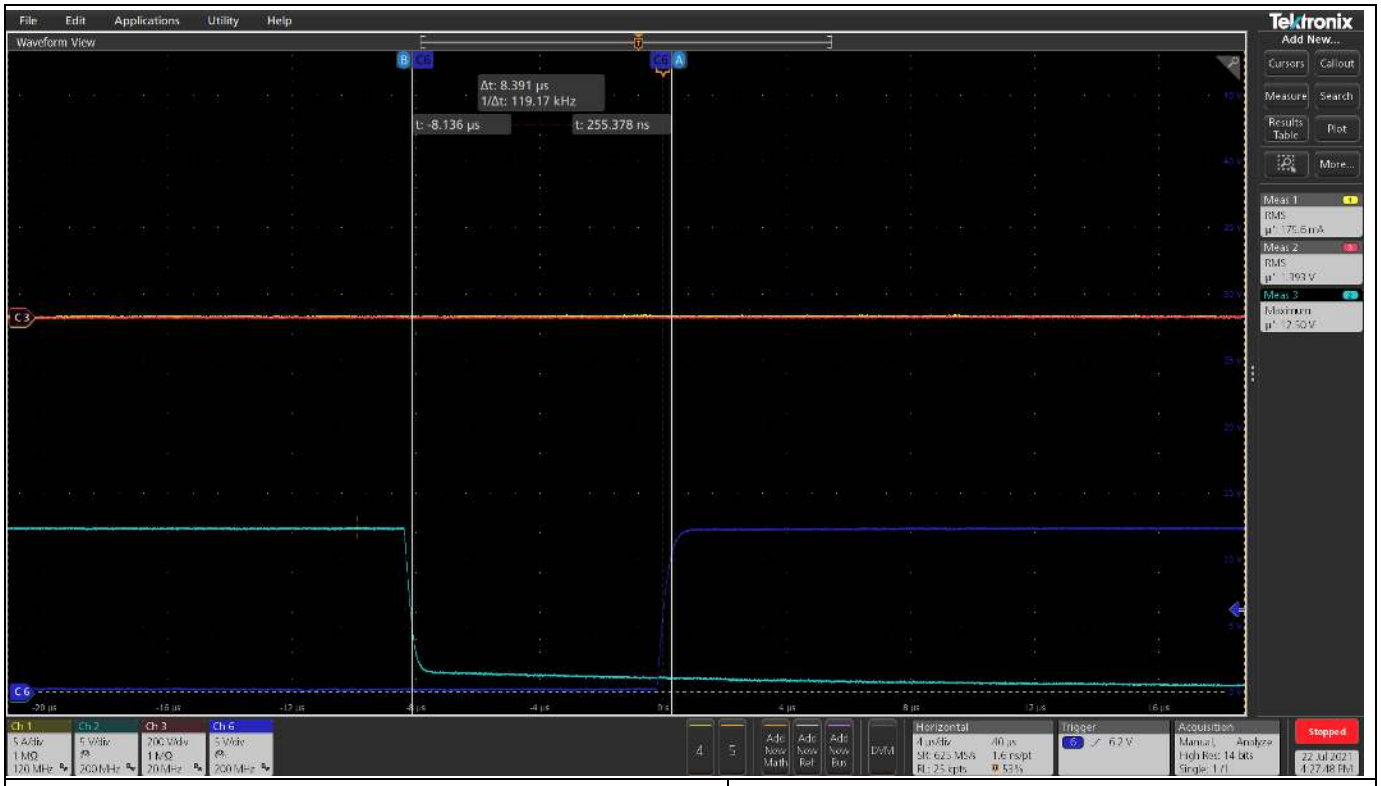
Figure 8 Steady-state waveforms of active bridge low-side complementary driving signals (dark blue and light blue lines), input current and voltage (magenta and yellow lines) and PFC output voltage (green line) at 230 V AC

3.2 Zero crossing

In the experiments of **Figure 9** and **Figure 10**, the zero crossing of the bridge is analyzed at both high- and low-line input voltage.

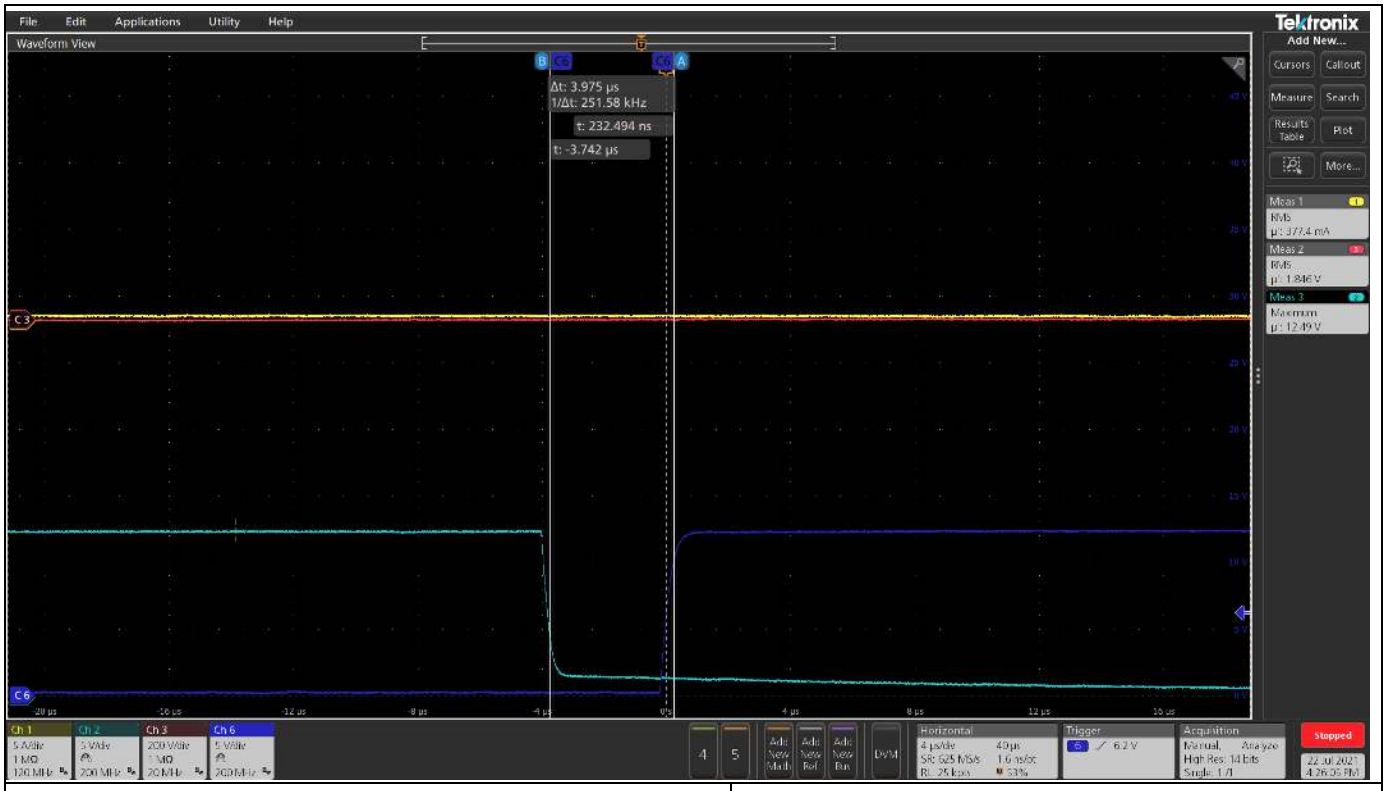
At 115 V_{RMS} the dead time between the high- and low-side gate signals is around 8 µs, as shown in **Figure 9**.

At 230 V_{RMS} the dead time between the high- and low-side gate signals is around 4 µs, as shown in **Figure 10**.



a) Vs = 36 mV	b) Vs = 44mV

Figure 9 Zero crossing at 115 V_{RMS}



a) Vs = 36 mV	b) Vs = 44 mV

Figure 10 Zero crossing at 230 V_{RMS}

3.3 Start-up waveforms

Active bridge behavior during PFC start-up is checked by mounting the **KIT_ACT_BRD_S7_4PIN** on the 2400 W CCM PFC demo board **EVAL_2K4W_ACT_BRD_S7**. The test is perfomed at light load. As shown in **Figure 11** the active bridge is activated only when the PFC starts boosting the current in order to reach the target output voltage. After that, because the load is very low, the active bridge is not triggered.

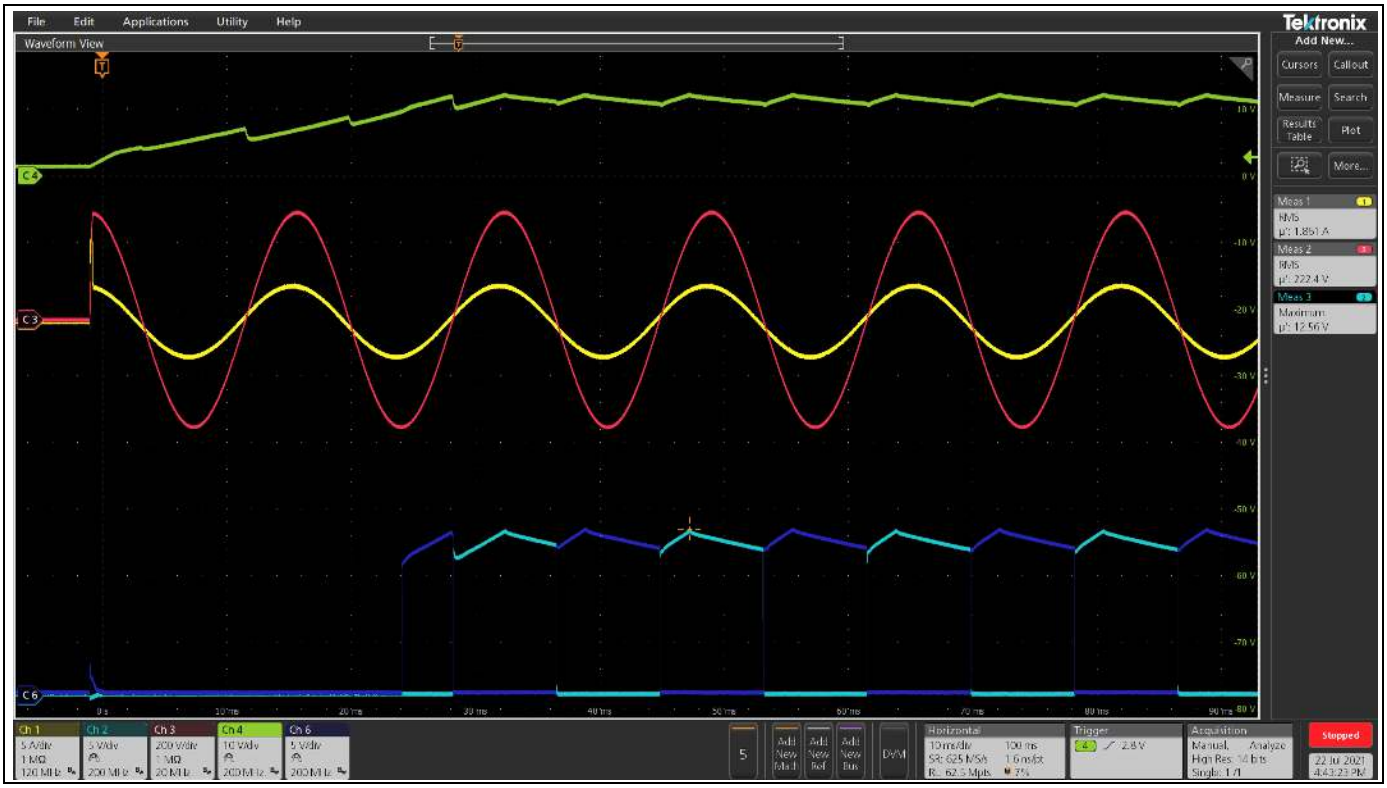


Figure 11 **PFC start-up waveforms of active bridge low-side complementary driving signals (dark blue and light blue lines), input current and voltage (magenta and yellow lines) and self-bias cell voltage (yellow line) at 230 V AC and V_{out} = 390 V**

3.4 Efficiency measurements

The efficiency measurements are performed by mounting the **KIT_ACT_BRD_S7_4PIN** on the 2400 W CCM PFC demo board **EVAL_2K4W_ACT_BRD_S7**. Load is changed through a DC electronic load and the output voltage is kept constant by the PFC at around 390 V DC.

Results at nominal low-line (115 V AC) and high-line (230 V AC) are shown in **Figure 12** and **Figure 13**, making a comparison with the standard diode bridge case. The fan consumption is included in the efficiency calculation.

A peak efficiency of 97.3 percent is reached with the 22 mΩ active bridge at around 50 percent of the output power at 115 V_{RMS} as shown in **Figure 12**.

A peak efficiency of 98.6 percent is reached with the 22 Ω active bridge at around 50 percent of the output power at 230 V_{RMS} as shown in **Figure 13**.

From **Figure 13** it is also evident that the PFC efficiency with the **KIT_ACT_BRD_S7_4PIN** is above 98 percent in almost all the load conditions, keeping a constant delta compared to the diode solution in the range of 0.4 to 0.5 percent.

The 22 mΩ active bridge is the most powerful active line rectification currently available on the market for this power range. Please note that in the **EVAL_2K4W_ACT_BRD_S7** the diode bridge is always present for surge protection purposes.

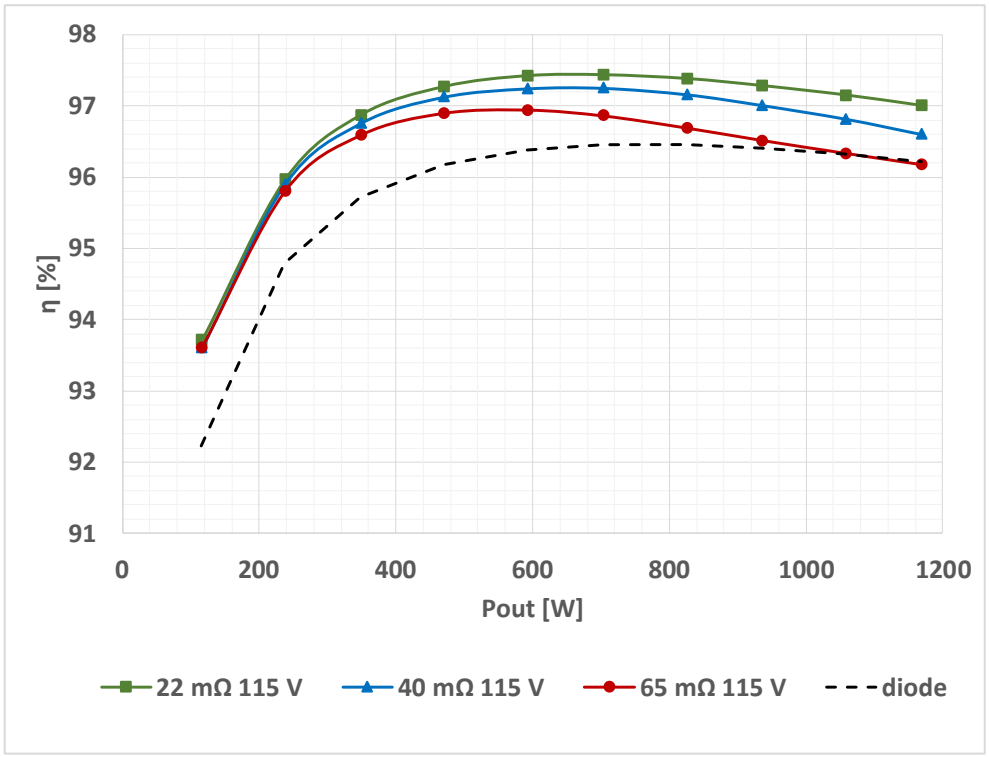


Figure 12 **Efficiency test result of EVAL_2K4W_ACT_BRD_S7 with and without KIT_ACT_BRD_S7_4PIN at both low-line (115 V AC) and high-line (230 V AC)**

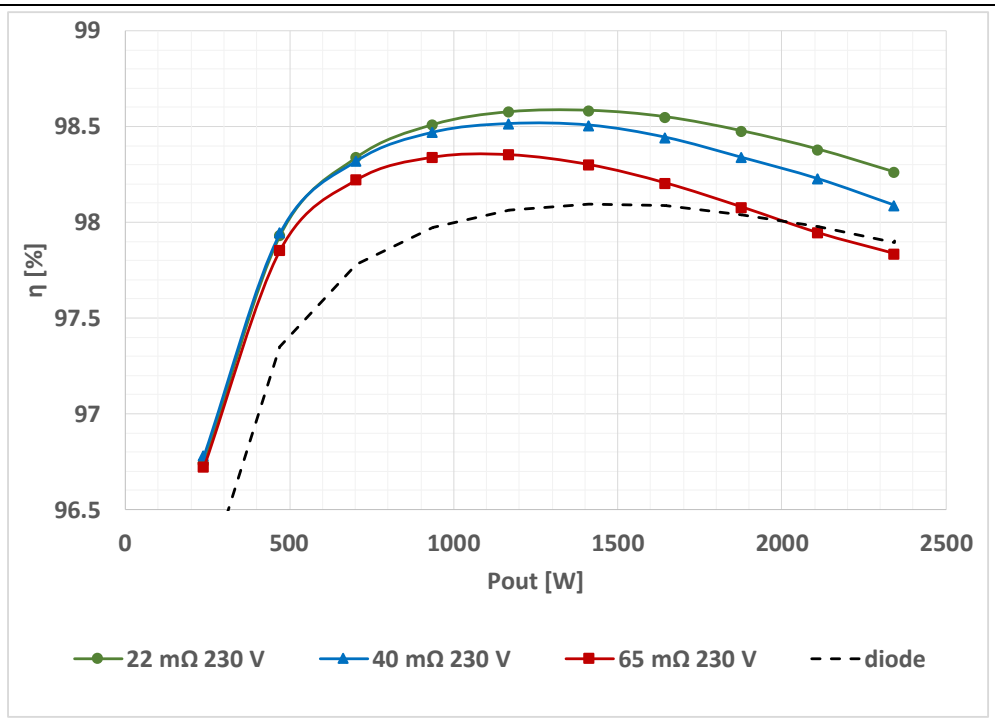


Figure 13 **Bridge temperature result of EVAL_2K4W_ACT_BRD_S7 with and without KIT_ACT_BRD_S7_4PIN at both low-line (115 V AC) and high-line (230 V AC)**

4 Summary

Active bridge line rectification is a circuit which can improve efficiency within entire power ranges for high efficiency and high power density in SMPS. It demonstrates a flexible design with different daughter board MOSFET $R_{DS(on)}$ for various efficiency requirements of different applications without any other circuit modification.

Steady-state waveforms are documented, as well as an indication of how to tune some control parameters depending on the application.

Start-up waveforms and efficiency improvement results with active bridge line rectification are demonstrated in a 2400 W PFC.

A schematic of a reference circuit is provided in this application note, so that readers can design and manufacture an active bridge line rectification board following the concept.

5 Schematics

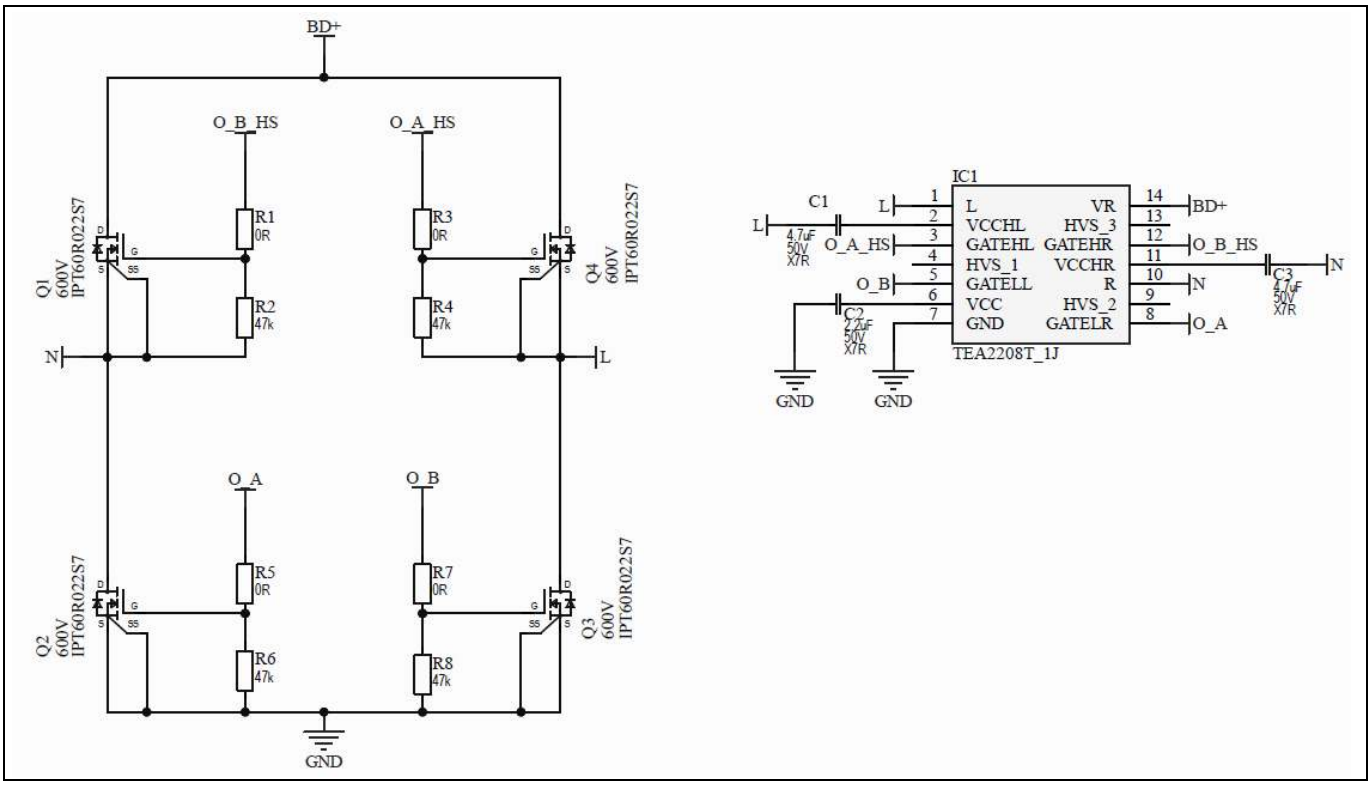
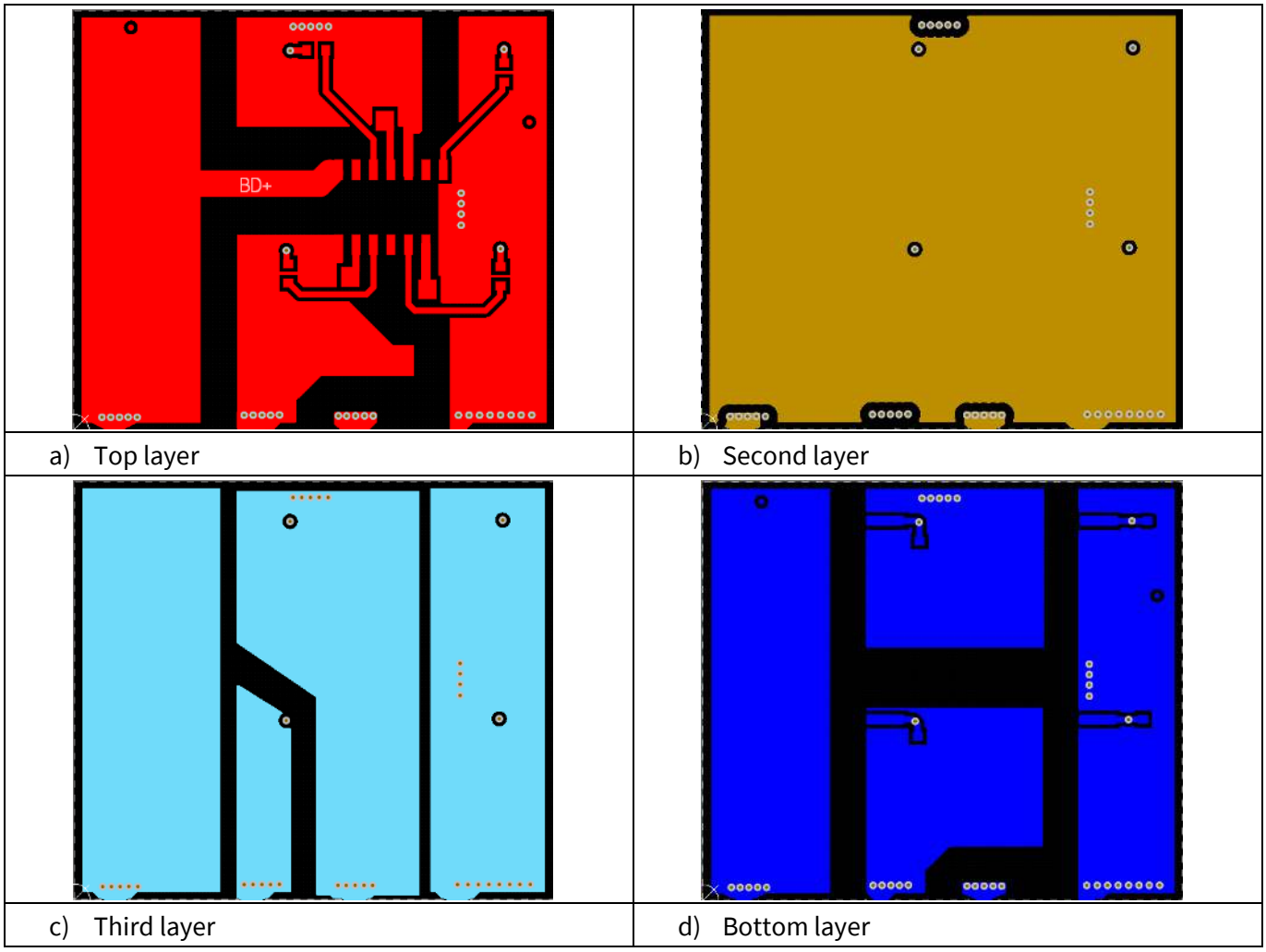


Figure 14 Active bridge daughter card schematic

6 PCB layout



a) Top layer

b) Second layer

c) Third layer

d) Bottom layer

Figure 15 Active bridge daughter card PCB layout: a) top, b) second, c) third and d) bottom layers

7 Bill of materials

Table 2 Active bridge daughter card components

Designator	Comment	Value	Voltage	Description
Q1, Q2, Q3, Q4	**SMD**	**IPT60R022S7**	**600 V**	**Power MOSFET**
C1, C3	SMD	4.7 µF	50 V	Ceramic capacitor
C2	SMD	2.2 µF	50 V	Ceramic capacitor
IC1	SMD	TEA2208T_1J		Integrated circuit
R1, R3, R5, R7	SMD	0R		Resistor
R2, R4, R6, R8	SMD	47k		Resistor

8 References

[1] “**22 mΩ active bridge daughter card: line rectifier module featuring 600 V CoolMOS™ S7, integrated IR11688S controller and 2EDF7275F driver in an ultra compact design**”, AN_1912_PL52_2002_094315.

[2] “**40 mΩ active bridge daughter card: line rectifier module featuring 600 V CoolMOS™ S7, integrated IR11688S controller and 2EDF7275F driver in an ultra compact design**”, AN_1912_PL52_2002_ 102254.

[3] “**65 mΩ active bridge daughter card: line rectifier module featuring 600 V CoolMOS™ S7, integrated IR11688S controller and 2EDF7275F driver in an ultra compact design**”, AN_1912_PL52_2002_ 160440.

[4] “**CCM PFC demo board with CoolMOS™ S7 for active line rectification and inrush current control**”, AN_1912_PL52_2002_103313.

Revision history

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V 1.0	2022-03-21	First release

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