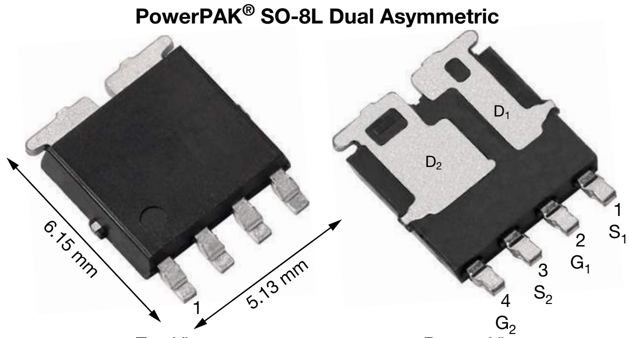
Automotive Dual N-Channel 100 V (D-S) 175 °C MOSFETs

PowerPAK® SO-8L Dual Asymmetric



Top View   Bottom View

FEATURESS

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Optimized for synchronous buck applications
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

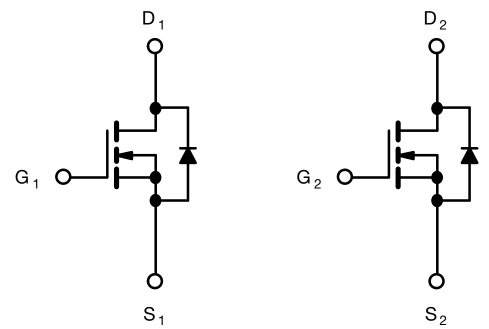
AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE

PRODUCT SUMMARY		
	N-CHANNEL 1	N-CHANNEL 2
V_{DS} (V)	100	100
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0400	0.0190
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.0505	0.0235
I_D (A)	17	34
Configuration	Dual N	
Package	PowerPAK SO-8L Dual Asymmetric	



N-Channel 1 MOSFET   N-Channel 2 MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Drain-Source Voltage		V_{DS}	100	100	V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current	T_C = 25 °C	I_D	17	34	A
	T_C = 125 °C		10	19	
Continuous Source Current (Diode conduction)		I_S	20 [a]	44	
Pulsed Drain Current [b]		I_{DM}	40	80	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	17	28	
Single Pulse Avalanche Energy		E_{AS}	14.4	39.2	mJ
Maximum Power Dissipation [b]	T_C = 25 °C	P_D	27	48	W
	T_C = 125 °C		9	16	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175		°C
Soldering Recommendations (Peak temperature) [d, e]			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Junction-to-Ambient	PCB mount [c]	R_{thJA}	85	85	°C/W
Junction-to-Case (Drain)		R_{thJC}	5.5	3.1	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR4 material).
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Static								
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		N-Ch 1	100	-	-	V
		V_{GS} = 0 V, I_D = 250 µA		N-Ch 2	100	-	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		N-Ch 1	1.5	2.0	2.5	
		V_{DS} = V_{GS}, I_D = 250 µA		N-Ch 2	1.5	2.0	2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		N-Ch 1	-	-	± 100	nA
				N-Ch 2	-	-	± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 100 V	N-Ch 1	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 100 V	N-Ch 2	-	-	1	
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 125 °C	N-Ch 1	-	-	50	
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 125 °C	N-Ch 2	-	-	50	
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 175 °C	N-Ch 1	-	-	250	
		V_{GS} = 0 V	V_{DS} = 100 V, T_J = 175 °C	N-Ch 2	-	-	250	
On-State Drain Current [a]	$I_{D(on)}$	V_{GS} = 10 V	$V_{DS} \geq$ 5 V	N-Ch 1	10	-	-	A
		V_{GS} = 10 V	$V_{DS} \geq$ 5 V	N-Ch 2	20	-	-	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 6 A	N-Ch 1	-	0.0325	0.0400	Ω
		V_{GS} = 10 V	I_D = 10 A	N-Ch 2	-	0.0154	0.0190	
		V_{GS} = 10 V	I_D = 6 A, T_J = 125 °C	N-Ch 1	-	-	0.0694	
		V_{GS} = 10 V	I_D = 10 A, T_J = 125 °C	N-Ch 2	-	-	0.0326	
		V_{GS} = 10 V	I_D = 6 A, T_J = 175 °C	N-Ch 1	-	-	0.0877	
		V_{GS} = 10 V	I_D = 10 A, T_J = 175 °C	N-Ch 2	-	-	0.0412	
		V_{GS} = 4.5 V	I_D = 4 A	N-Ch 1	-	0.0412	0.0505	
		V_{GS} = 4.5 V	I_D = 8 A	N-Ch 2	-	0.0191	0.0235	
Forward Transconductance [b]	g_{fs}	V_{DS} = 10 V, I_D = 6 A		N-Ch 1	-	17	-	S
		V_{DS} = 10 V, I_D = 10 A		N-Ch 2	-	34	-	
Dynamic [b]								
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch 1	-	475	650	pF
		V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch 2	-	1065	1390	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch 1	-	280	375	
		V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch 2	-	560	750	
Reverse Transfer Capacitance	C_{rss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch 1	-	18	25	
		V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	N-Ch 2	-	37	50	
Total Gate Charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 50 V, I_D = 1 A	N-Ch 1	-	10	15	nC
		V_{GS} = 10 V	V_{DS} = 50 V, I_D = 1 A	N-Ch 2	-	20	30	
Gate-Source Charge [c]	Q_{gs}	V_{GS} = 10 V	V_{DS} = 50 V, I_D = 1 A	N-Ch 1	-	2	-	
		V_{GS} = 10 V	V_{DS} = 50 V, I_D = 1 A	N-Ch 2	-	3	-	
Gate-Drain Charge [c]	Q_{gd}	V_{GS} = 10 V	V_{DS} = 50 V, I_D = 1 A	N-Ch 1	-	3	-	
		V_{GS} = 10 V	V_{DS} = 50 V, I_D = 60 A	N-Ch 2	-	5	-	
Gate Resistance	R_g	f = 1 MHz		N-Ch 1	1.2	2.5	3.8	Ω
				N-Ch 2	0.6	1.4	2.2	

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Dynamic [b]							
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 1	-	8	15	ns
		V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 2	-	12	20	
Rise Time [c]	t_r	V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 1	-	3	5	
		V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 2	-	3	5	
Turn-Off Delay Time [c]	$t_{d(off)}$	V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 1	-	22	35	
		V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 2	-	28	45	
Fall Time [c]	t_f	V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 1	-	21	35	
		V_{DD} = 50 V, R_L = 5 Ω, $I_D \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	N-Ch 2	-	22	35	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed Current [a]	I_{SM}		N-Ch 1	-	-	40	A
			N-Ch 2	-	-	80	
Forward Voltage	V_{SD}	I_F = 6 A, V_{GS} = 0 V	N-Ch 1	-	0.87	1.2	V
		I_F = 10 A, V_{GS} = 0 V	N-Ch 2	-	0.84	1.2	

Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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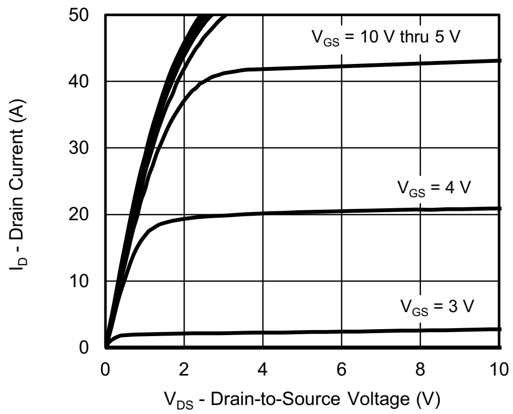
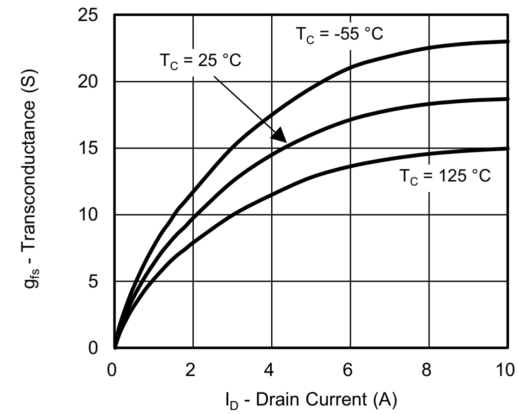
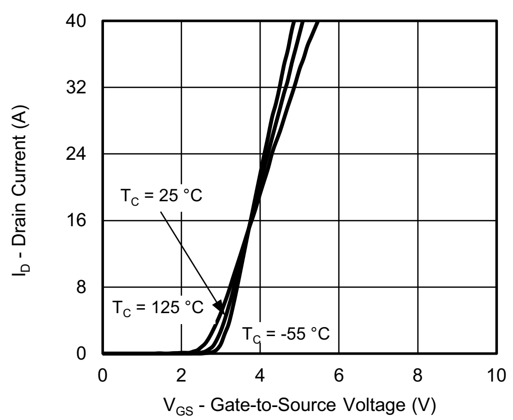
N-CHANNEL 1 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



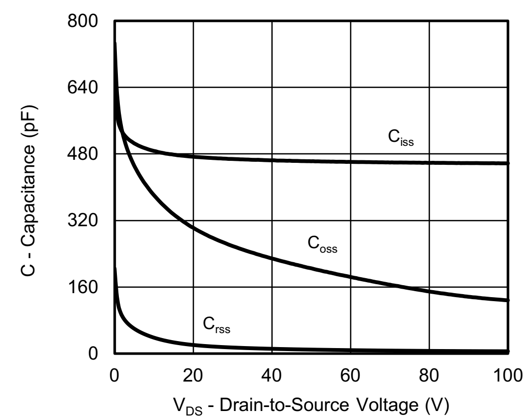
Output Characteristics



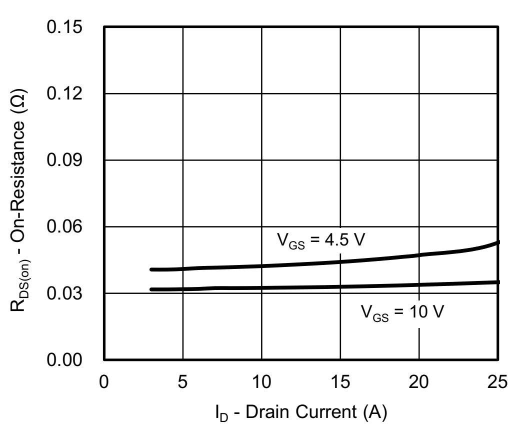
Transconductance



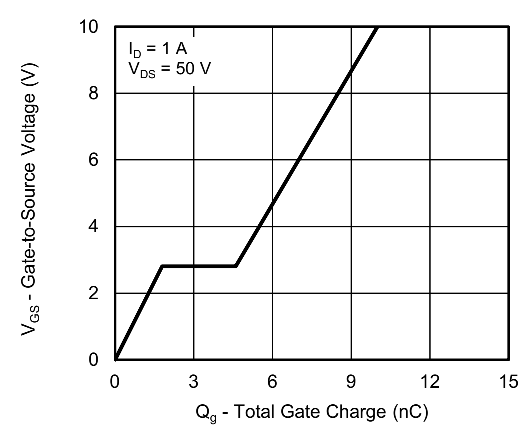
Transfer Characteristics



Capacitance



On-Resistance vs. Drain Current



Gate Charge

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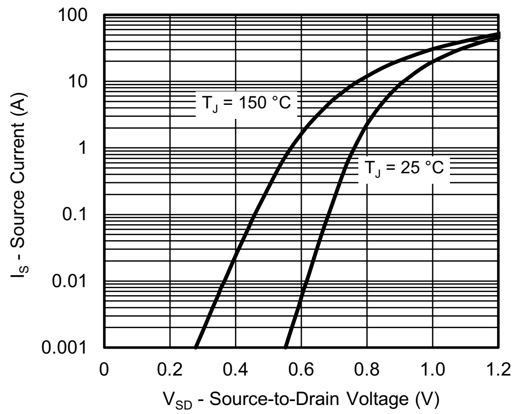
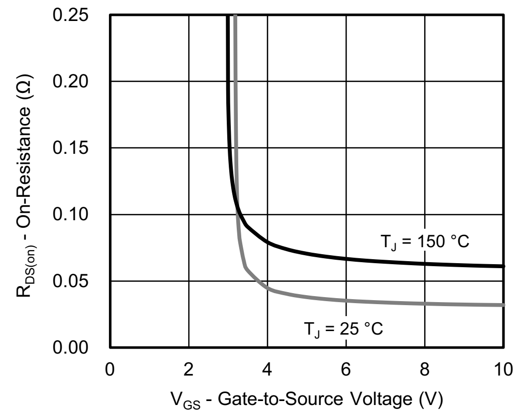
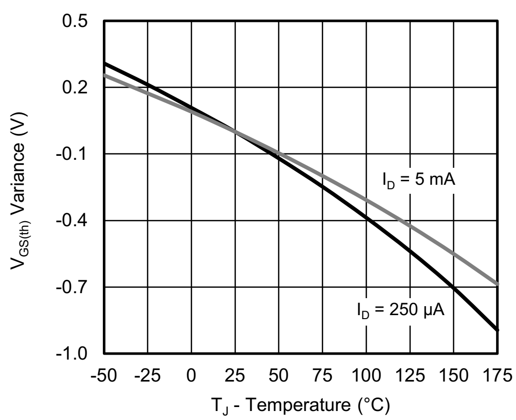


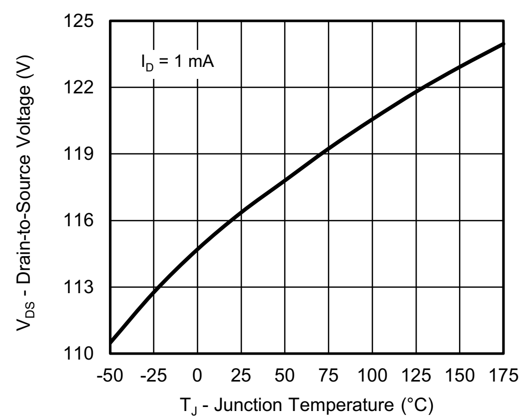
Source Drain Diode Forward Voltage



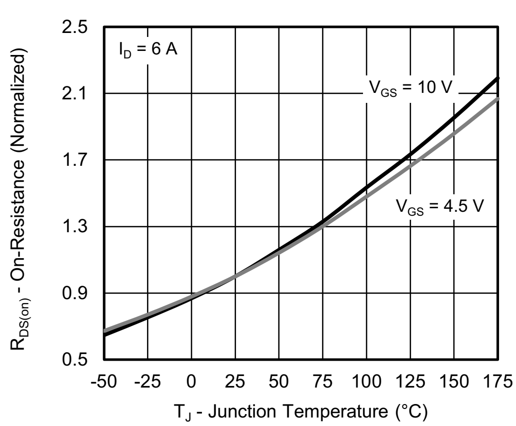
On-Resistance vs. Gate-to-Source Voltage



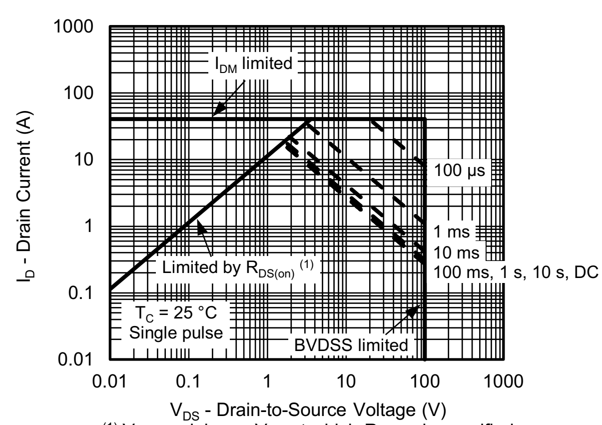
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Junction Temperature



(1) V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

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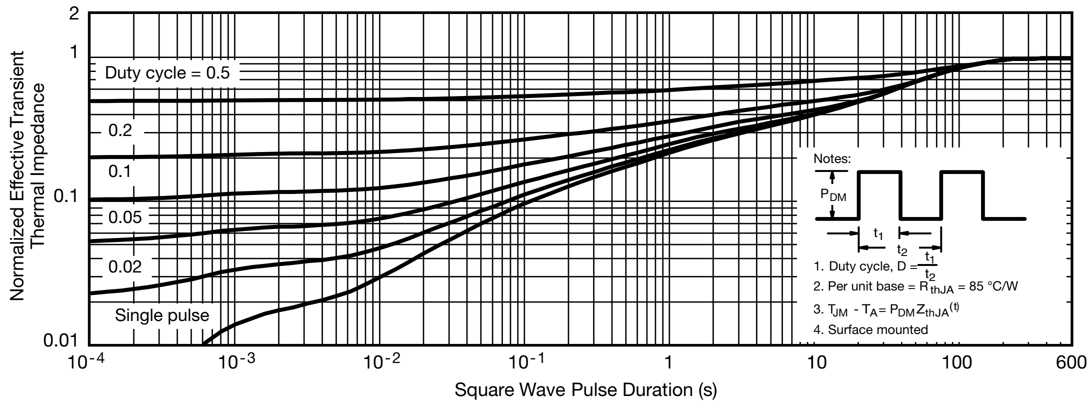
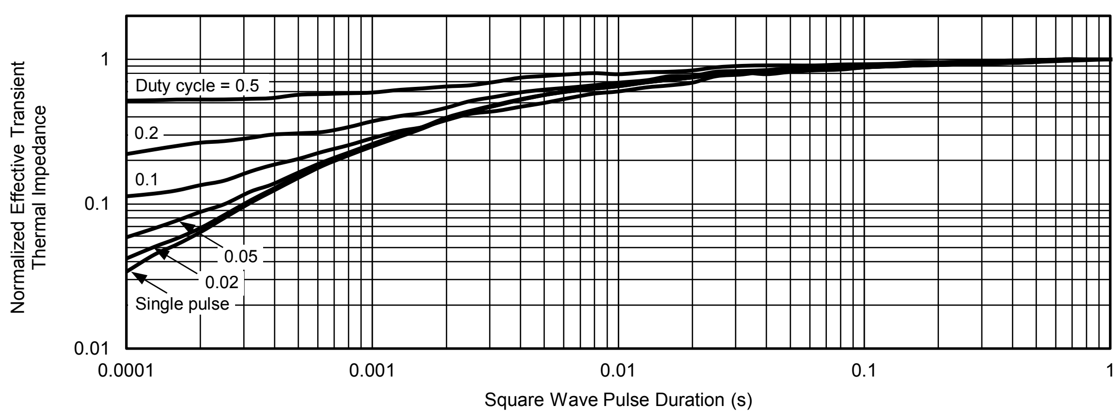


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the graph:
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

  is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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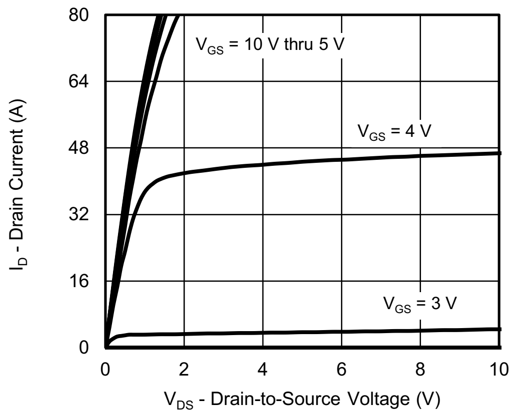
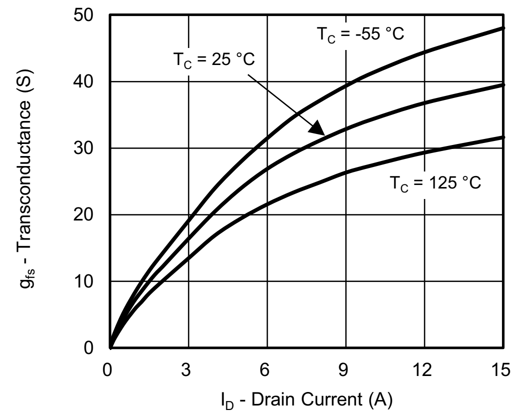
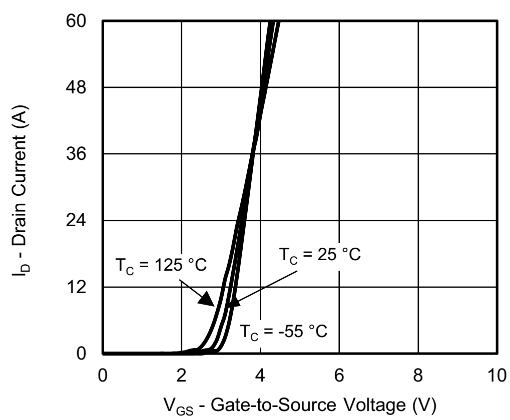
N-CHANNEL 2 TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



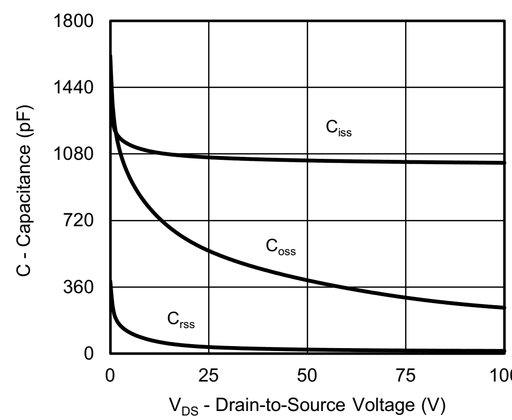
Output Characteristics



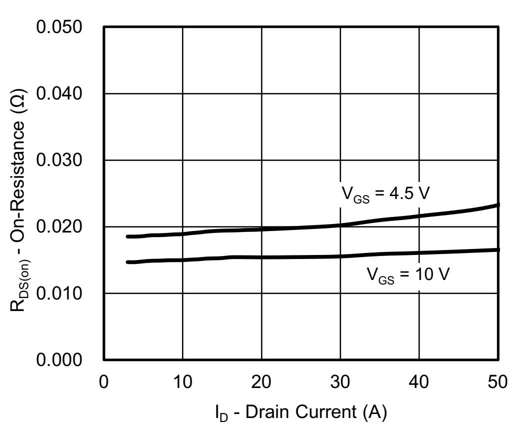
Transconductance



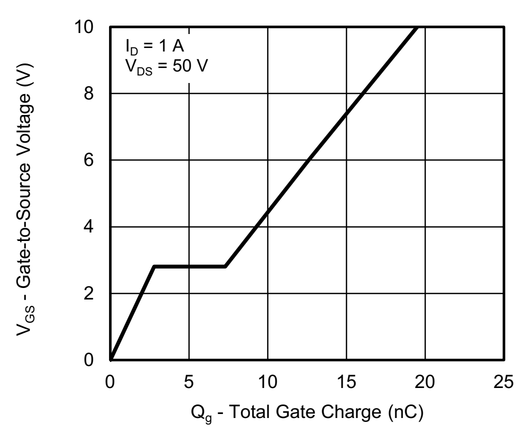
Transfer Characteristics



Capacitance



On-Resistance vs. Drain Current



Gate Charge

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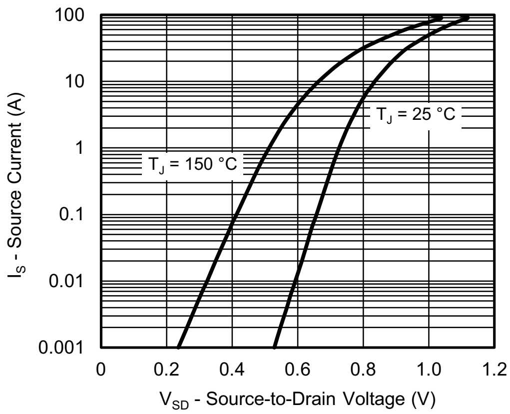
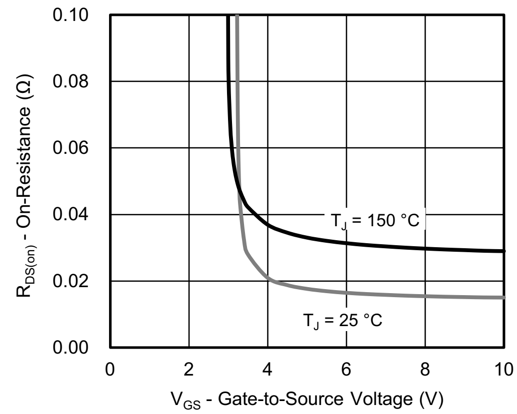
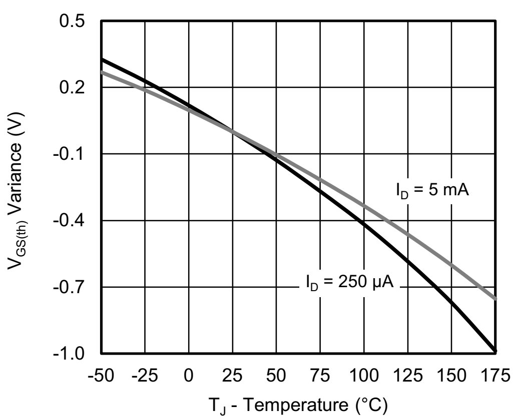


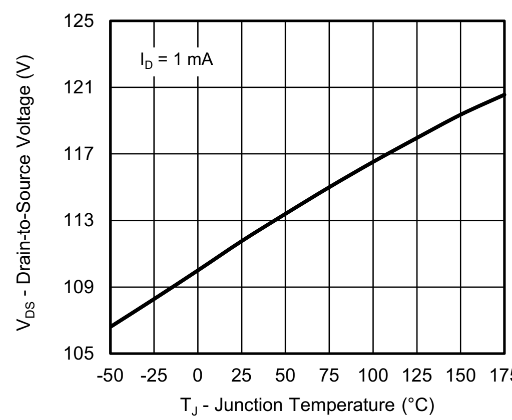
Source Drain Diode Forward Voltage



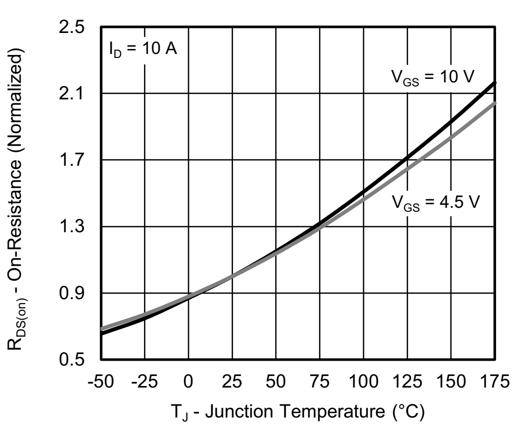
On-Resistance vs. Gate-to-Source Voltage



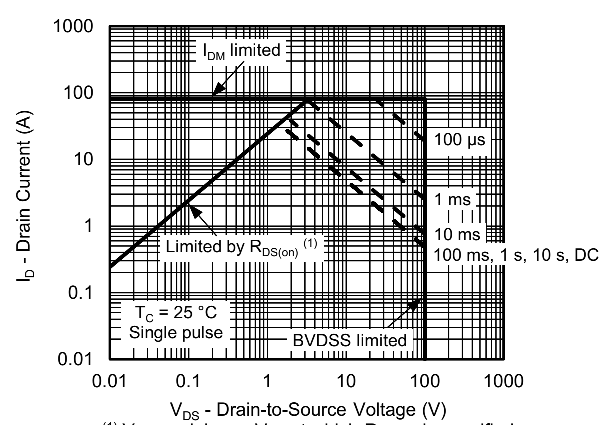
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Junction Temperature



(1) V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

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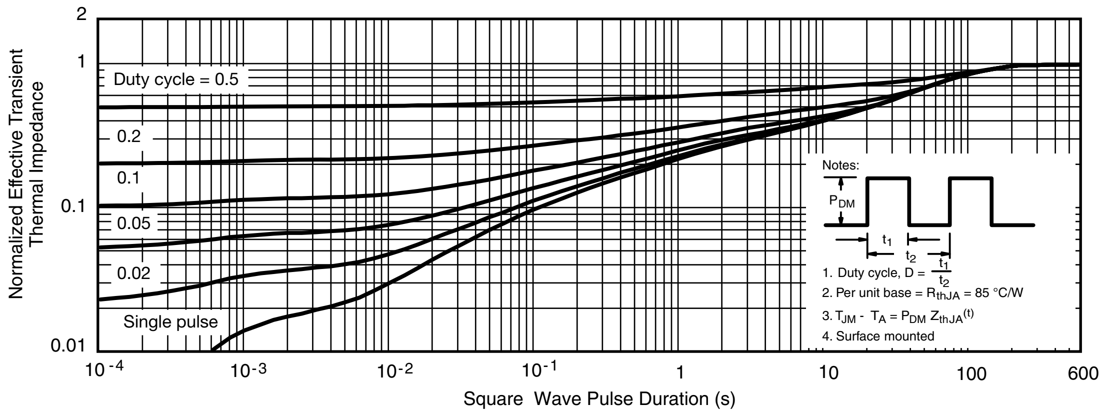
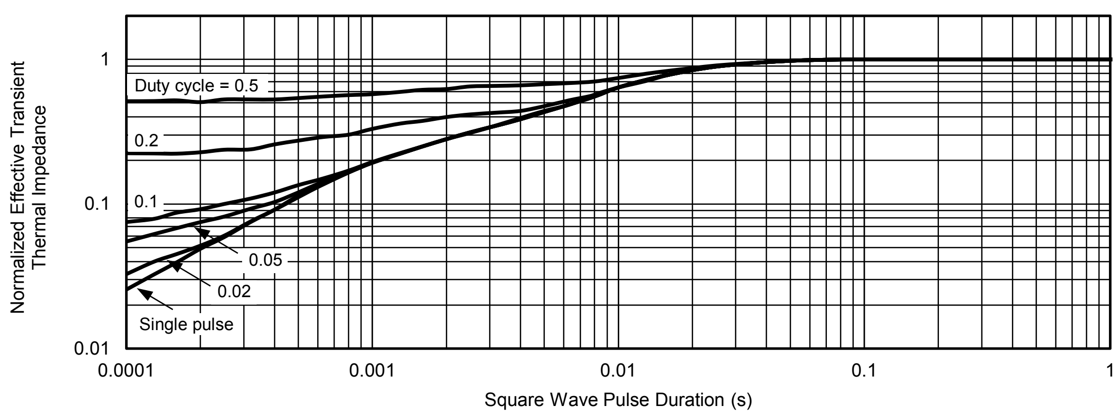


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the graph:
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
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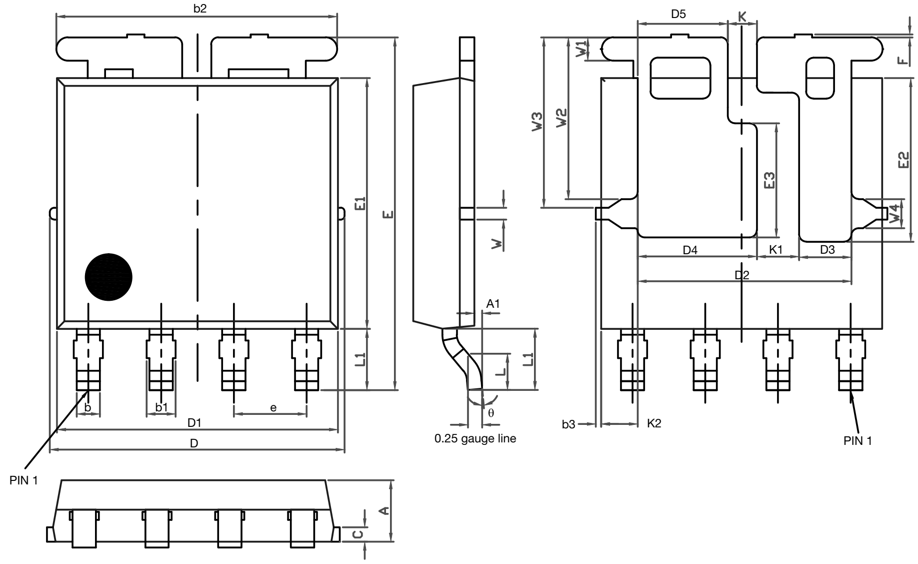
PowerPAK® SO-8L Assymetric Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	0.06	0.13	0.000	0.003	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.04	0.12	0.20	0.002	0.005	0.008
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.63	3.73	3.83	0.143	0.147	0.151
D3	0.81	0.91	1.01	0.032	0.036	0.040
D4	1.98	2.08	2.18	0.078	0.082	0.086
D5	1.47	1.57	1.67	0.058	0.062	0.066
e	1.20	1.27	1.34	0.047	0.050	0.053
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	1.89	1.99	2.09	0.074	0.078	0.082
F	0.05	0.12	0.19	0.002	0.005	0.007
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.41	0.51	0.61	0.016	0.020	0.024
K1	0.64	0.74	0.84	0.025	0.029	0.033
K2	0.54	0.64	0.74	0.021	0.025	0.029
W	0.13	0.23	0.33	0.005	0.009	0.013
W1	0.31	0.41	0.51	0.012	0.016	0.020
W2	2.72	2.82	2.92	0.107	0.111	0.115
W3	2.86	2.96	3.06	0.113	0.117	0.120
W4	0.41	0.51	0.61	0.016	0.020	0.024
θ	5°	10°	12°	5°	10°	12°

DWG: 6009

Note

- Millimeters will govern

For technical questions, contact: pmostechsupport@vishay.com
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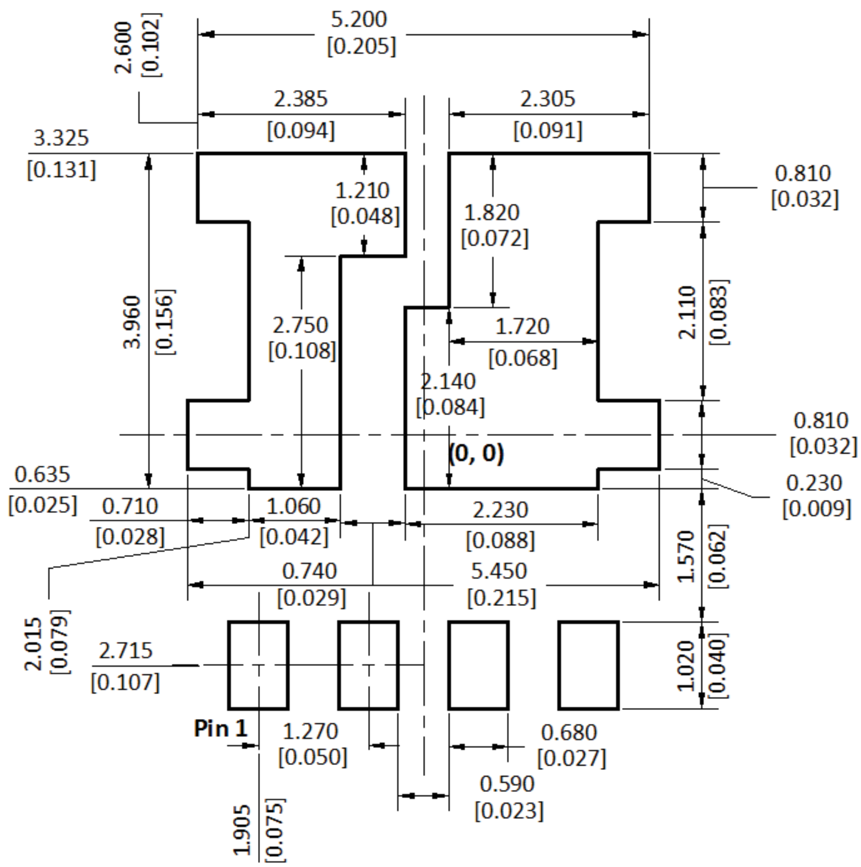
RECOMMENDED MINIMUM PADs FOR PowerPAK® SO-8L DUAL ASYMMETRIC



Recommended Minimum Pads
Dimensions in mm [inches]

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