HARRIS

HM-6617/883

June 1989

2K x 8 CMOS PROM

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby and Operating Power
  - ICCSB 100μA
  - ICCOP .... 20mA at 1MHz
- Fast Access Time.. 90/120ns
- Industry Standard Pinout
- Single 5.0 Volt Supply
- CMOS/TTL Compatible Inputs
- High Output Drive .... 12 LSTTL Loads
- Synchronous Operation
- On-Chip Address Latches
- Separate Output Enable
- Operating Temperature Range .... -55°C to +125°C

Description

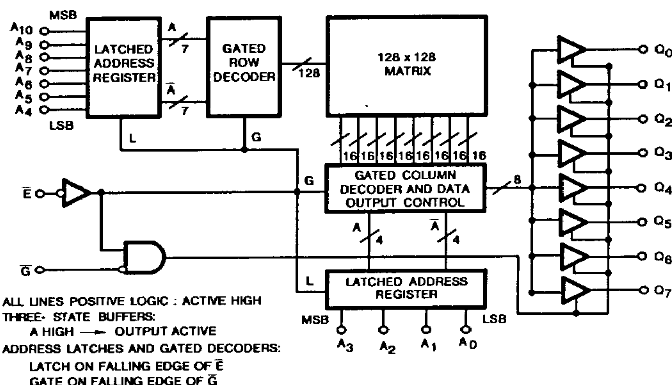
The HM-6617/883 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8 bit/word format with "Three-State" outputs. This PROM is available in the standard 0.600 inch wide 24 pin Ceramic DIP, the 0.300 inch wide slimline Ceramic DIP, and the JEDEC standard 32 pad Ceramic LCC.

The HM-6617/883 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Harris NiCr fuse link technology is utilized on this and other Harris CMOS PROMs. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature voltage ranges. NiCr fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard bipolar PROMs or NMOS EPROMs.

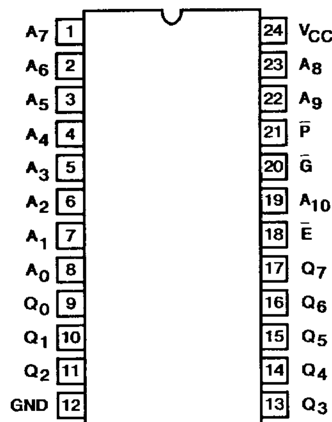
All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Functional Diagram

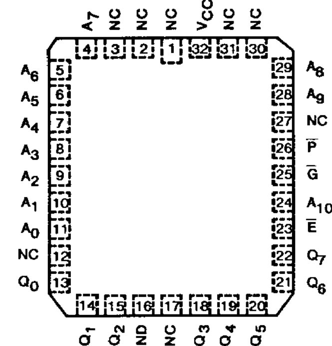


Pinouts

HM1-6617/883 (CERAMIC DIP)
TOP VIEW



HM4-6617/883 (CERAMIC LCC)
TOP VIEW



PIN	DESCRIPTION
NC	No Connect
A_0 - A_{10}	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Input
VCC	Power (+5V)
$\overline{G}$	Output Enable
$\overline{P}$*	Program Enable

* $\overline{P}$ Should be Hardwired to V_{CC} Except During Programming

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Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND)..... +7.0V
Input or Output Voltage Applied for all Grades .... GND-0.3V to V_{CC}+0.3V
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec).................. +300°C
Junction Temperature .... +175°C
ESD Classification .... Class 1
Typical Derating Factor .... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	9°C/W
Ceramic LCC Package	58°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.86W
Gate Count .... 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (V_{CC}) .... 4.5V to 5.5V
Operating Temperature (T_A) .... -55°C to +125°C
Input Low Voltage (V_{IL}) .... -0.3V to +0.8V
Input High Voltage (V_{IH}) .... +2.4V to V_{CC} +0.3V

TABLE 1. HM-6617/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH1	V_{CC} = 4.5V, IO = -2.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	V_{CC} = 4.5V, IO = +4.8mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	V_{CC} = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or V_{CC}	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	μA
Input Leakage Current	II	V_{CC} = 5.5V, VI = GND or V_{CC}, $\overline{P}$ Not Tested	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	μA
Standby Supply Current	ICCSB	VI = V_{CC} or GND, V_{CC} = 5.5V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	μA
Operating Supply Current	ICCOP	V_{CC} = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = V_{CC} or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	20	mA
Functional Test	FT	V_{CC} = 4.5V (Note 12)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	

TABLE 2. HM-6617/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Access Time	TAVQV	V_{CC} = 4.5V and 5.5V (Note 5)	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	140	ns
Output Enable Access Time	TGLQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	50	ns
Chip Enable Access Time	TELQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	120	ns
Address Setup Time	TAVEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	20	-	ns
Address Hold Time	TELAX	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	25	-	ns
Chip Enable Low Width	TELEH	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	ns
Chip Enable High Width	TEHEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	ns
Read Cycle Time	TELEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	160	-	ns

NOTES:
1. All voltages referenced to Device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≈ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with $\overline{P}$ hardwired to V_{CC}.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-6617/883 A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	10	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	12	pF
			6, 11	+25°C	-	10	pF
I/O Capacitance	$C_{I/O}$	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	12	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	14	pF
			6, 11	+25°C	-	12	pF
Chip Enable Time	TELQX	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable Time	TGLQX	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Disable Time	TEHQZ	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output Disable Time	TGHQZ	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Output High Voltage	V_{OH2}	V_{CC} = 4.5V, IO = 100μA	6	$-55^oC \leq T_A \leq +125^oC$	V_{CC}- 1V	-	V

NOTES:
6. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.
7. Tested as follows: f = 2MHz, V_{IH} = 2.4V, V_{IL} = 0.4V, I_{OH} = -4.0mA, $V_{OH} \geq 1.5V$, and $V_{OL} \leq 1.5V$.
8. This is a "typical" value and not a "maximum" value.
9. Applies to .600 inch Ceramic Dual-In-Line (DIP) device types only.
10. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
11. Applies to Ceramic Leadless Chip Carrier (LCC) device types only.
12. Tested as follows: f = 1MHz, V_{IH} = 2.4V, V_{IL} = 0.8V, I_{OH} = -1mA, I_{OL} = +1mA, $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND)..... +7.0V
Input or Output Voltage Applied for all Grades .... GND-0.3V to V_{CC}+0.3V
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10 sec).................. +300°C
Junction Temperature .... +175°C
ESD Classification .... Class 1
Typical Derating Factor .... 5mA/MHz Increase in ICCOP

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	9°C/W
Ceramic LCC Package	58°C/W	19°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.86W
Gate Count .... 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (V_{CC}).................... 4.5V to 5.5V
Operating Temperature (T_A).................. -55°C to +125°C
Input Low Voltage (V_{IL}) .... -0.3V to +0.8V
Input High Voltage (V_{IH}) .... +2.4V to V_{CC} +0.3V

TABLE 1. HM-6617B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

D.C. PARAMETERS	SYMBOL	(NOTES 1, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	V_{OH1}	V_{CC} = 4.5V, IO = -2.0mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.5V, IO = +4.8mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	V_{CC} = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or V_{CC}	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-1.0	1.0	µA
Input Leakage Current	II	V_{CC} = 5.5V, VI = GND or V_{CC}, $\overline{P}$ Not Tested	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-1.0	1.0	µA
Standby Supply Current	ICCSB	VI = V_{CC} or GND, V_{CC} = 5.5V, IO = 0mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	100	µA
Operating Supply Current	ICCOP	V_{CC} = 5.5V, $\overline{G}$ = GND, (Note 3), f = 1MHz, IO = 0mA, VI = V_{CC} or GND	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	20	mA
Functional Test	FT	V_{CC} = 4.5V (Note 12)	7, 8A, 8B	$-55^oC \leq T_A \leq +125^oC$	-	-	

TABLE 2. HM-6617B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 4) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Access Time	TAVQV	V_{CC} = 4.5V and 5.5V (Note 5)	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	105	ns
Output Enable Access Time	TGLQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Chip Enable Access Time	TELQV	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	90	ns
Address Setup Time	TAVEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	15	-	ns
Address Hold Time	TELAX	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	20	-	ns
Chip Enable Low Width	TELEH	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	95	-	ns
Chip Enable High Width	TEHEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Read Cycle Time	TELEL	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	136	-	ns

NOTES:
1. All voltages referenced to Device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL $\simeq$ 50pF.
3. Typical derating = 5mA/MHz increase in ICCOP.
4. All tests performed with $\overline{P}$ hardwired to V_{CC}.
5. TAVQV = TELQV + TAVEL

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-6617B/883 A.C. AND D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 4) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	10	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	12	pF
			6, 11	+25°C	-	10	pF
I/O Capacitance	$C_{I/O}$	V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 9	+25°C	-	12	pF
		V_{CC} = Open, f = 1MHz, All Measurements Referenced to Device GND	6, 10	+25°C	-	14	pF
			6, 11	+25°C	-	12	pF
Chip Enable Time	TELQX	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Output Enable Time	TGLQX	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	5	-	ns
Chip Disable Time	TEHQZ	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	45	ns
Output Disable Time	TGHQZ	V_{CC} = 4.5V and 5.5V	6	$-55^oC \leq T_A \leq +125^oC$	-	40	ns
Output High Voltage	V_{OH2}	V_{CC} = 4.5V, IO = 100μA	6	$-55^oC \leq T_A \leq +125^oC$	V_{CC}- 1V	-	V

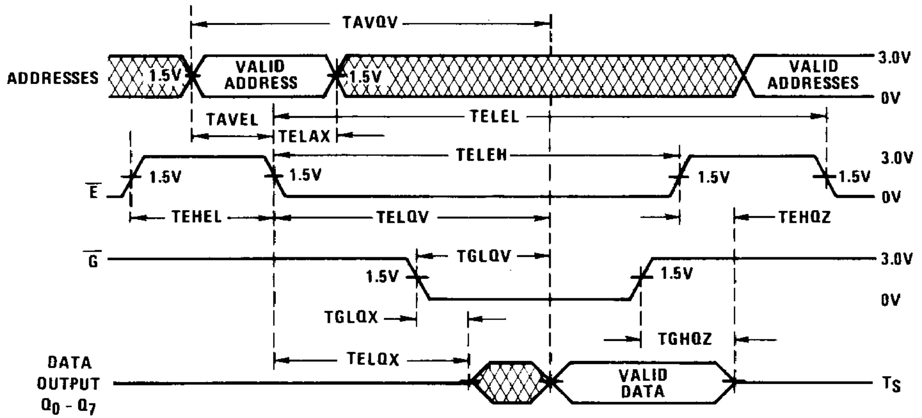
NOTES:
6. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.
7. Tested as follows: f = 2MHz, V_{IH} = 2.4V, V_{IL} = 0.4V, I_{OH} = -4.0mA, $V_{OH} \geq$ 1.5V, and $V_{OL} \leq$ 1.5V.
8. This is a typical" value and not a maximum" value.
9. Applies to .600 inch Ceramic Dual-In-Line (DIP) device types only.
10. Applies to .300 inch Ceramic Dual-In-Line (DIP) device types only.
11. Applies to Ceramic Leadless Chip Carrier (LCC) device types only.
12. Tested as follows: f = 1MHz, V_{IH} = 2.4V, V_{IL} = 0.8V, I_{OH} = -1mA, I_{OL} = +1mA, $V_{OH} \geq$ 1.5V, $V_{OL} \leq$ 1.5V.

TABLE 4. APPLICABLE SUBGROUPS

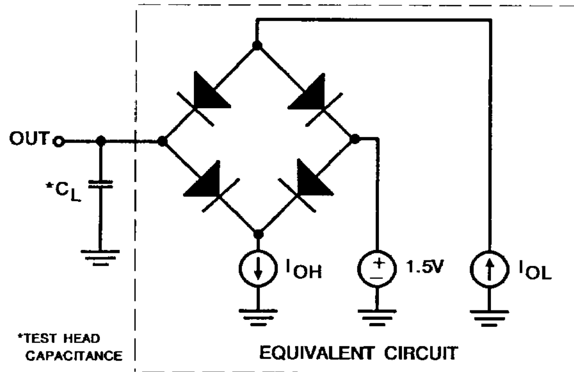
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Switching Waveforms

READ CYCLE

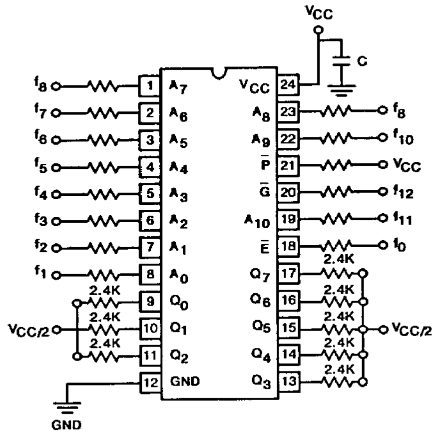


Test Circuit

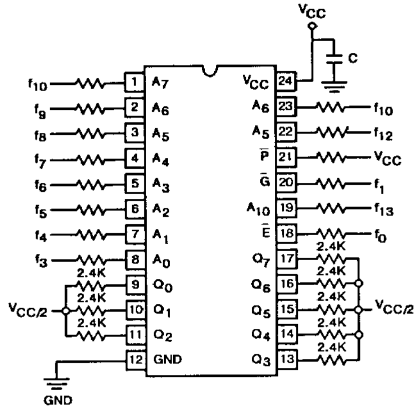


Burn-In Circuits

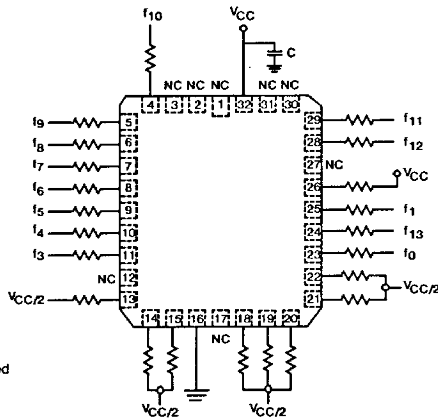
HM-6617/883 (.300 INCH) CERAMIC DIP



HM-6617/883 (.600) CERAMIC DIP



HM-6617/883 CERAMIC LCC



NOTES:

f_0 = 100kHz ± 10%
All resistors = 47kΩ Unless Otherwise Noted
V_{CC} = 5.5V ± 0.05V
C = 0.01μF min

Metallization Topology

DIE DIMENSIONS:

140 x 232 x 19 ± 1mils

METALLIZATION:

Type: Si - Al

Thickness: 11kÅ - 15kÅ

GLASSIVATION:

Type: SiO_2

Thickness: 7kÅ - 9kÅ

DIE ATTACH:

Material: Si - Au Eutectic

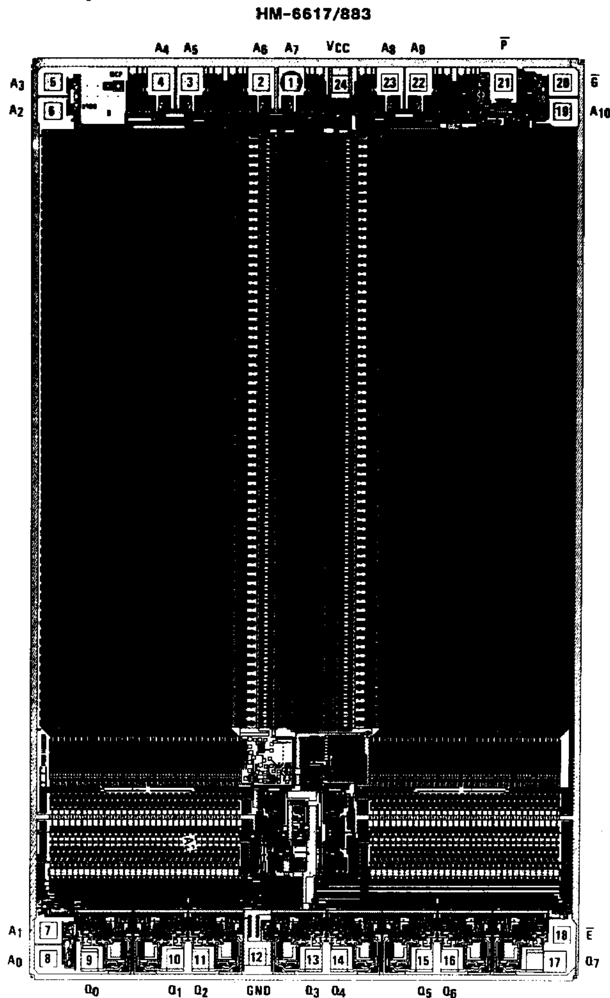
Temperature: Ceramic DIP — 460°C (Max)

Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:

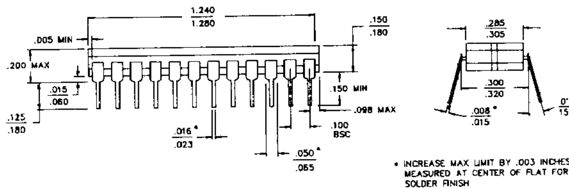
1.7×10^5 A/cm^2

Metallization Mask Layout



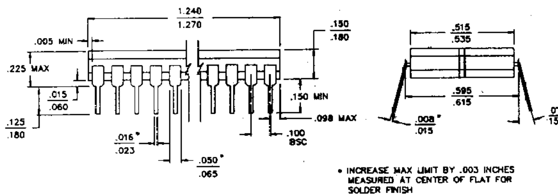
Packaging †

24 PIN (.300) CERAMIC DIP



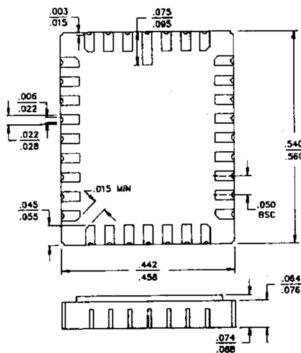
LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-9

24 PIN (.600) CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Ceramic Al_2O_3 90%
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze
INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HM-6617

DESIGN INFORMATION

2K x 8 CMOS PROM

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Background Information HM-6617 Programming

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IL}	Input "0"	0.0	0.2	0.8	V	
V_{IH}	Voltage "1"	V_{CC}-2	V_{CC}	V_{CC}+0.3	V	6
V_{CCPROG}	Programming V_{CC}	12.0	12.0	12.5	V	2
V_{CC1}	Operating V_{CC}	4.5	5.5	5.5	V	
V_{CC2}	Special Verify V_{CC}	4.0	-	6.0	V	3
t_d	Delay Time	1.0	1.0	-	µs	
t_r	Rise Time	1.0	10.0	10.0	µs	
t_f	Fall Time	1.0	10.0	10.0	µs	
TEHEL	Chip Enable Pulse Width	50	-	-	ns	
TAVEL	Address Valid to Chip Enable Low Time	20	-	-	ns	
TELQV	Chip Enable Low to Output Valid Time	-	-	120	ns	
t_{pw}	Programming Pulse Width	90	100	110	µs	4
t_{IP}	Input Leakage at V_{CC} = V_{CCPROG}	-10	+1.0	10	µA	
I_{OP}	Data Output Current at V_{CC} = V_{CCPROG}	-	-5.0	-10	mA	
R_n	Output Pull-Up Resistor	5	10	15	kΩ	5
T_A	Ambient Temperature	-	25	-	°C	

NOTES:

1. All inputs must track V_{CC} (pin 24) within these limits.
2. V_{CCPROG} must be capable of supplying 500mA.
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to V_{CC} through a resistor of value R_n.
6. Except during programming (See Programming Cycle Waveforms).

DESIGN INFORMATION (Continued)

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Background Information Programming Algorithm

The HM-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or any of the approved commercial programmers can be used.

PROGRAMMING SEQUENCE OF EVENTS

1) Apply a voltage of V_{CC1} to V_{CC} of the PROM.
2) Read all fuse locations to verify that the PROM is blank (output low).
3) Place the PROM in the initial state for programming: $\overline{E} = V_{IH}$, $\overline{P} = V_{IH}$, $\overline{G} = V_{IL}$.
4) Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5) After a delay of t_d, apply voltage of V_{IL} to $\overline{E}$ (pin 18) to access the addressed word.
6) The address may be held through the cycle, but must be held valid at least for a time equal to t_d after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7) After a delay of t_d, disable the outputs by applying a voltage of V_{IH} to $\overline{G}$ (pin 20).
8) After a delay of t_d, apply voltage of V_{IL} to $\overline{P}$ (pin 21).
9) After delay of t_d, raise V_{CC} (pin 24) to V_{CCPROG} with a rise time of t_r. All outputs at V_{IH} should track V_{CC} with V_{CC}-2.0V to V_{CC}+0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value R_n.
10) After a delay of t_d, pull the output which corresponds to the bit to be programmed to V_{IL}. Only one bit should be programmed at a time.
11) After a delay of t_{pw}, allow the output to be pulled to V_{IH} through pull-up resistor R_n.
12) After a delay of t_d, reduce V_{CC} (pin 24) to V_{CC1} with a fall time of t_f. All outputs at V_{IH} should track V_{CC} with V_{CC}-2.0V to V_{CC}+0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value R_n.
13) Apply a voltage of V_{IH} to $\overline{P}$ (pin 21).
14) After a delay of t_d, apply a voltage of V_{IL} to $\overline{G}$ (pin 20).
15) After a delay of t_d, examine the outputs for correct data. If any location verifies incorrectly, repeat steps 4 through 14 (attempting to program only those bits in the word which verified incorrectly) up to a maximum of eight attempts for a given word. If a word does not program within eight attempts, it should be considered a programming reject.
16) Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

POST-PROGRAMMING VERIFICATION

17) Place the PROM in the post-programming verification mode: $\overline{E} = V_{IH}$, $\overline{G} = V_{IL}$, $\overline{P} = V_{IH}$, V_{CC} (pin 24) = V_{CC1}.
18) Apply the correct binary address of the word to be verified to the PROM.
19) After a delay of t_d, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
20) After a delay of t_d, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21) Repeat steps 17 through 20 for all possible programming locations.

POST-PROGRAMMING READ

22) Apply a voltage of V_{CC2} = 4.0V to V_{CC} (pin 24).
23) After a delay of t_d, apply a voltage of V_{IH} to $\overline{E}$ (pin 18).
24) Apply the correct binary address of the word to be read.
25) After a delay of TAVEL, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
26) After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27) Repeat steps 23 through 26 for all address locations.
28) Apply a voltage of V_{CC2} = 6.0V to V_{CC} (pin 24).
29) Repeat steps 23 through 26 for all address locations.

DESIGN INFORMATION (Continued)

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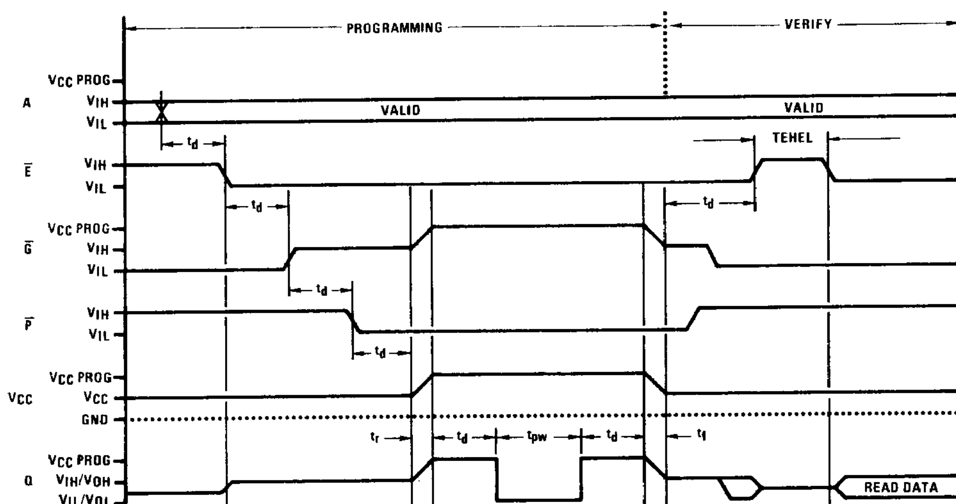
HM-6617 PROGRAMMING CYCLE



HM-6617 POST PROGRAMMING VERIFY CYCLE