

**COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET
POWERDI® 5060-8**

Product Summary

Device	V _{(BR)DSS}	R _{DS(ON)}	I _D T _A = +25°C
Q1	12V	17mΩ @ V _{GS} = 4.5V	9.5A
		25mΩ @ V _{GS} = 2.5V	7.8A
Q2	-12V	32mΩ @ V _{GS} = -4.5V	-6.9A
		53mΩ @ V _{GS} = -2.5V	-5.4A

Description and Applications

This new generation Complementary Pair Enhancement Mode MOSFET has been designed to minimize R_{DS(on)} and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Loadswitch.

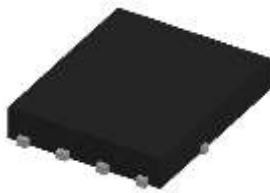
- Notebook Battery Power Management
- DC-DC Converters
- Loadswitch

Features and Benefits

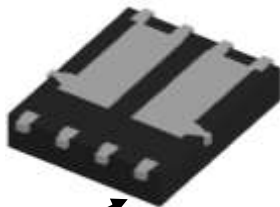
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R_{DS(ON)} – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

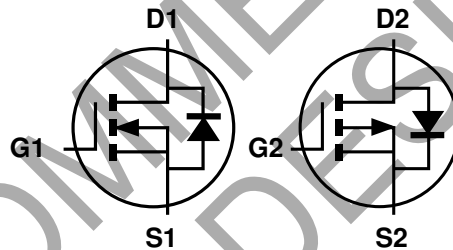
- Case: POWERDI5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Weight: 0.097 grams (approximate)



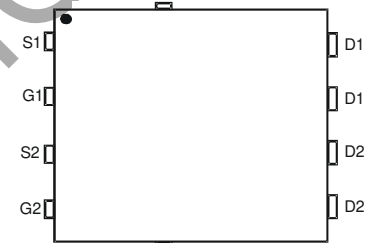
Top View



Bottom View
Pin1



Q1 N-Channel MOSFET Q2 P-Channel MOSFET



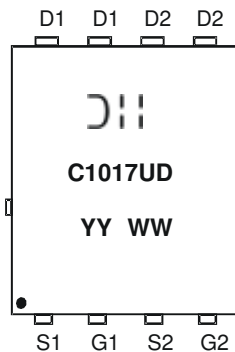
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMC1017UPD-13	POWERDI5060-8	2500 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



☺☺☺ = Manufacturer's Marking
 C1017UD = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 13 = 2013)
 WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Q1 Value	Q2 Value	Units
Drain-Source Voltage		V _{DSS}	12	-12	V
Gate-Source Voltage		V _{GSS}	±8	±8	V
Continuous Drain Current (Note 5) V _{GS} = 4.5V	Steady State	I _D	9.5 7.6	-6.9 -5.5	A
	t < 10s	I _D	13.0 10.4	-9.4 -7.5	A
Maximum Body Diode Forward Current		I _S	2	-2	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)		I _{DM}	50	-35	A
Avalanche Current (Note 6) L = 0.1mH		I _{AS}	9.7	-9.2	A
Avalanche Energy (Note 6) L = 0.1mH		E _{AS}	4.7	4.3	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P _D	T _A = +25°C	2.3
		T _A = +70°C	1.5
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	Steady state	54
		t < 10s	29
Thermal Resistance, Junction to Case (Note 5)	R _{θJC}	4.1	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	12	—	—	V	V _{GS} = 0V, I _D = 250µA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	µA	V _{DS} = 12V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	0.6	—	1.5	V	V _{DS} = V _{GS} , I _D = 250µA
Static Drain-Source On-Resistance	R _{DS(on)}	—	9.6	17	mΩ	V _{GS} = 4.5V, I _D = 11.8A
		—	11	25		V _{GS} = 2.5V, I _D = 9.8A
Diode Forward Voltage	V _{SD}	—	0.7	1.2	V	V _{GS} = 0V, I _S = 2.9A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	1787	—	pF	V _{DS} = 6V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	297	—		
Reverse Transfer Capacitance	C _{rss}	—	265	—		
Gate Resistance	R _G	—	1.6	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	18.6	—	nC	V _{DS} = 6V, I _D = 11.8A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	35.4	—		
Gate-Source Charge	Q _{gs}	—	2.7	—		
Gate-Drain Charge	Q _{gd}	—	3.8	—		
Turn-On Delay Time	t _{D(on)}	—	6.9	—	nS	V _{DD} = 6V, R _L = 6Ω V _{GS} = 4.5V, R _G = 6Ω, I _D = 1A
Turn-On Rise Time	t _r	—	10.9	—		
Turn-Off Delay Time	t _{D(off)}	—	70.3	—		
Turn-Off Fall Time	t _f	—	31.8	—		
Body Diode Reverse Recovery Time	t _{rr}	—	13.1	—	nS	I _F = 11.8A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q _{rr}	—	2.2	—	nC	I _F = 11.8A, di/dt = 100A/µs

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = 25°C.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

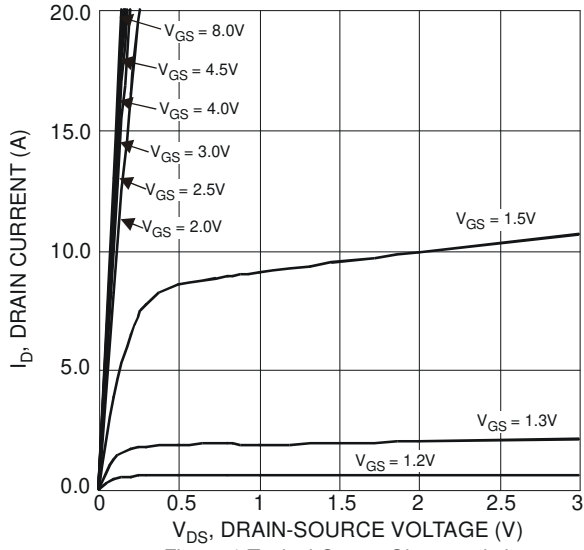


Figure 1 Typical Output Characteristics

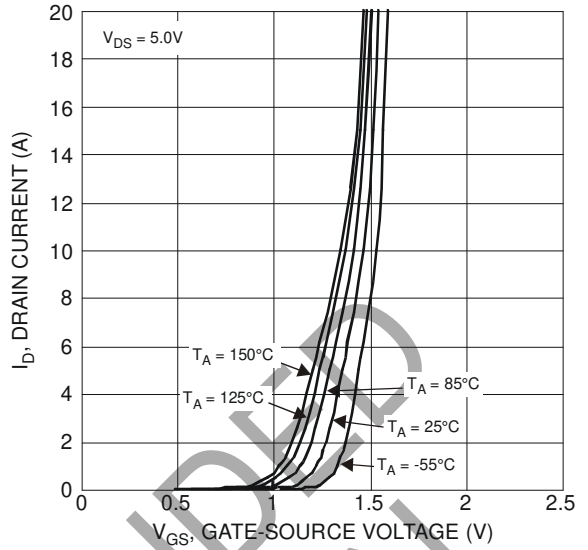


Figure 2 Typical Transfer Characteristics

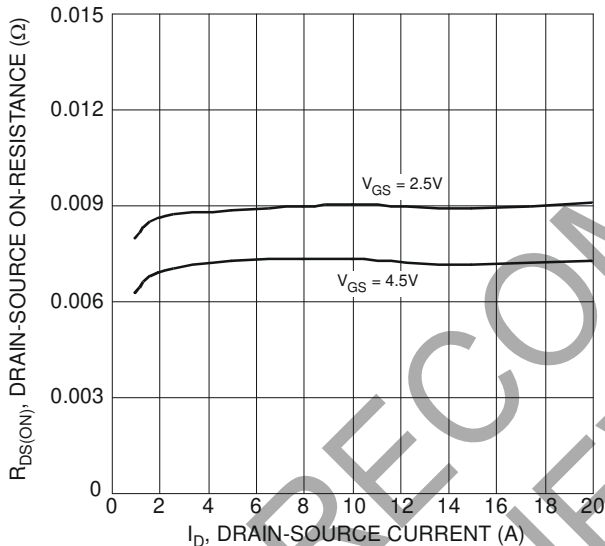


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

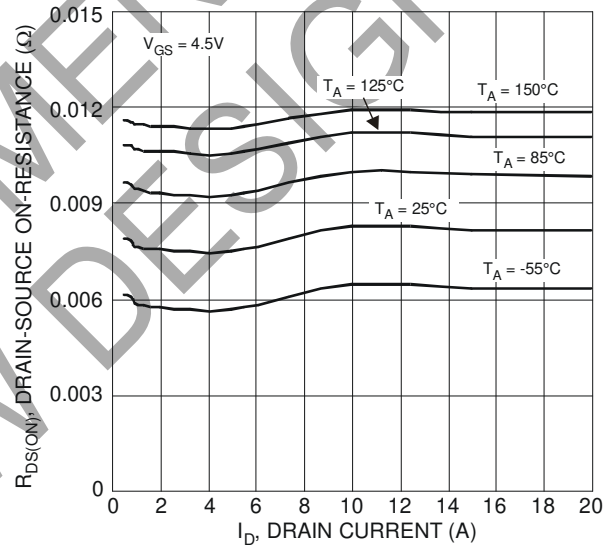


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

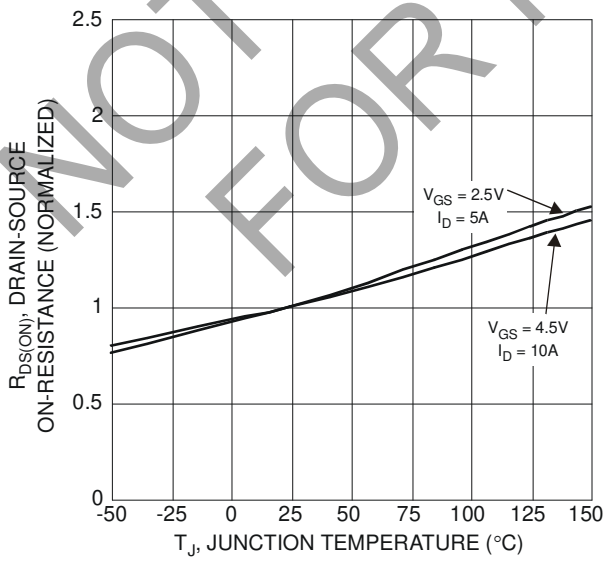


Figure 5 On-Resistance Variation with Temperature

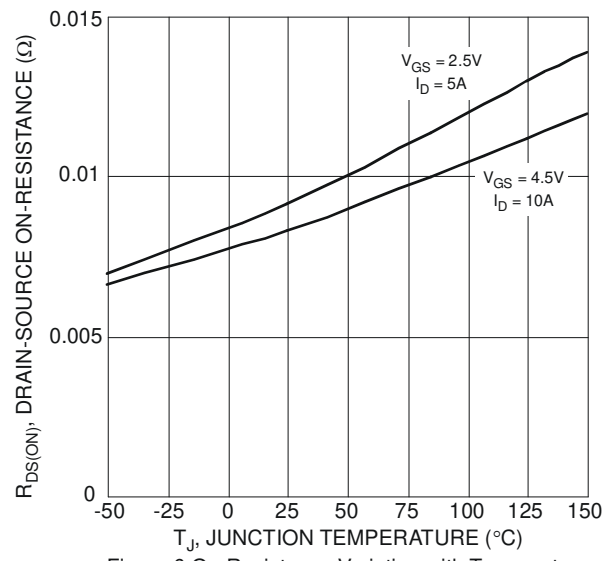


Figure 6 On-Resistance Variation with Temperature

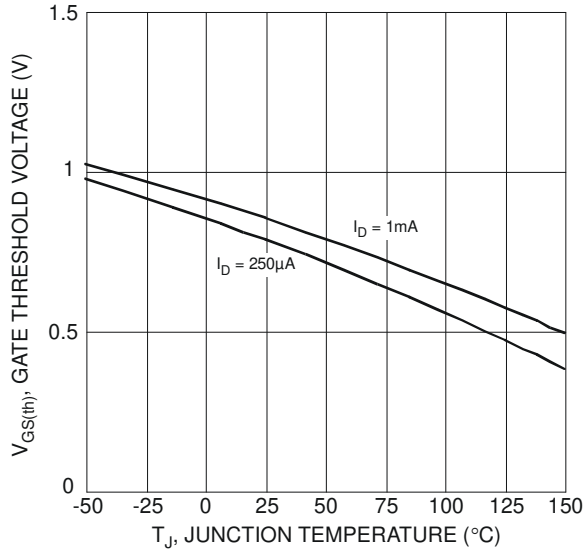


Figure 7 Gate Threshold Variation vs. Ambient Temperature

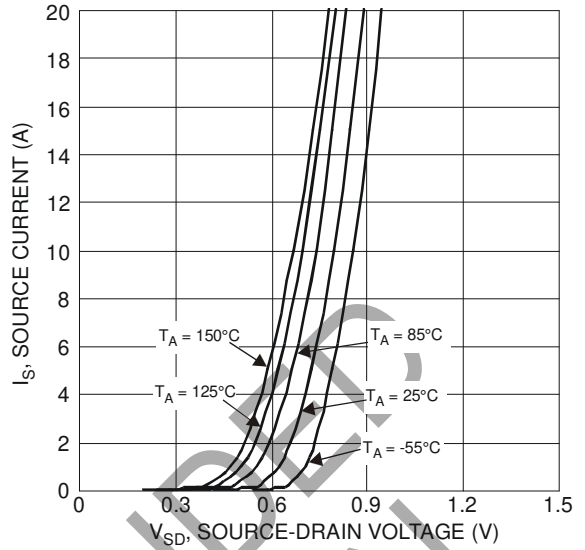


Figure 8 Diode Forward Voltage vs. Current

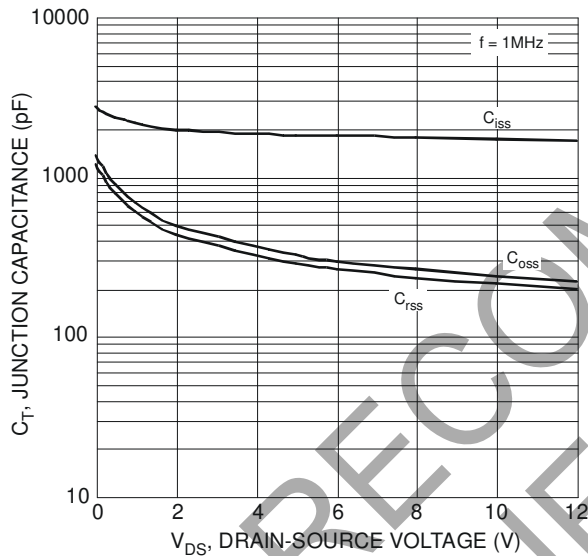


Figure 9 Typical Junction Capacitance

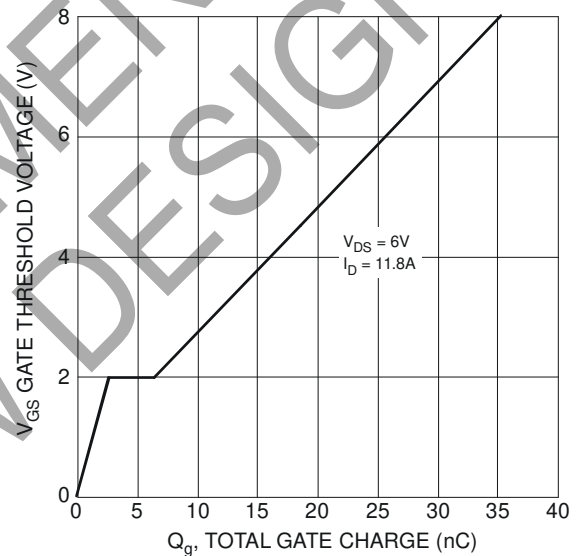


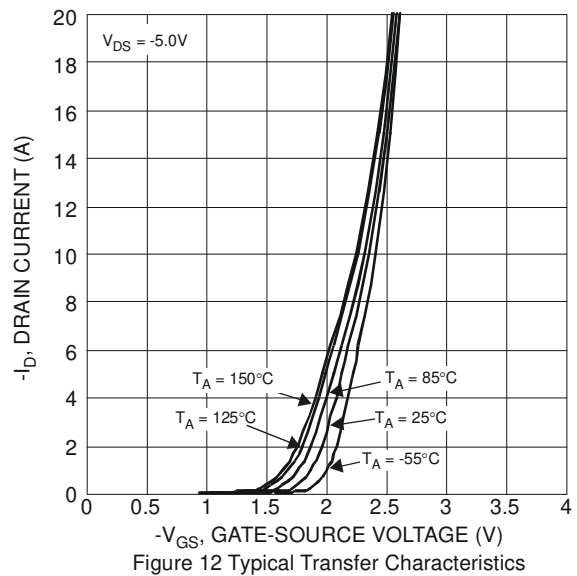
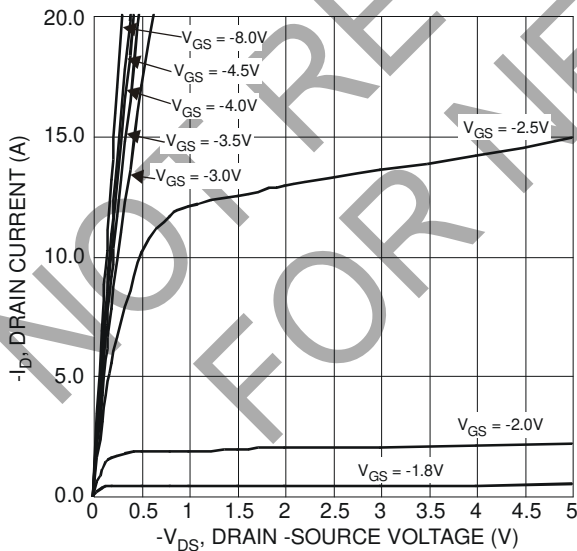
Figure 10 Gate Charge

NOT RECOMMENDED FOR NEW DESIGN

Electrical Characteristics Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV _{DSS}	-12	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1	μA	V _{DS} = -12V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	V _{GS(th)}	-0.6	—	-1.5	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	21	32	mΩ	V _{GS} = -4.5V, I _D = -8.9A
		—	41	53		V _{GS} = -2.5V, I _D = -6.9A
Diode Forward Voltage	V _{SD}	—	-0.7	-1.2	V	V _{GS} = 0V, I _S = -2.9A
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C _{iSS}	—	2100	—	pF	V _{DS} = -6V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oSS}	—	872	—		
Reverse Transfer Capacitance	C _{rSS}	—	626	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Gate Resistance	R _G	—	23.1	—		
Total Gate Charge (V _{GS} = -4.5V)	Q _g	—	23.7	—	nC	V _{DS} = -6V, I _D = -8.9A
Total Gate Charge (V _{GS} = -8V)	Q _g	—	38.8	—		
Gate-Source Charge	Q _{gs}	—	5.3	—		
Gate-Drain Charge	Q _{gd}	—	9.8	—		
Turn-On Delay Time	t _{D(on)}	—	10.6	—	nS	V _{DD} = -6V, R _L = 6Ω V _{GS} = -4.5V, R _G = 6Ω, I _D = -1A
Turn-On Rise Time	t _r	—	25.5	—		
Turn-Off Delay Time	t _{D(off)}	—	144	—		
Turn-Off Fall Time	t _f	—	129	—		
Body Diode Reverse Recovery Time	t _{rr}	—	48.9	—	nS	I _F = -8.9A, di/dt = -100A/μs
Body Diode Reverse Recovery Charge	Q _{rr}	—	15.3	—	nC	I _F = -8.9A, di/dt = -100A/μs

Notes: 6. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = 25°C.
7. Short duration pulse test used to minimize self-heating effect.



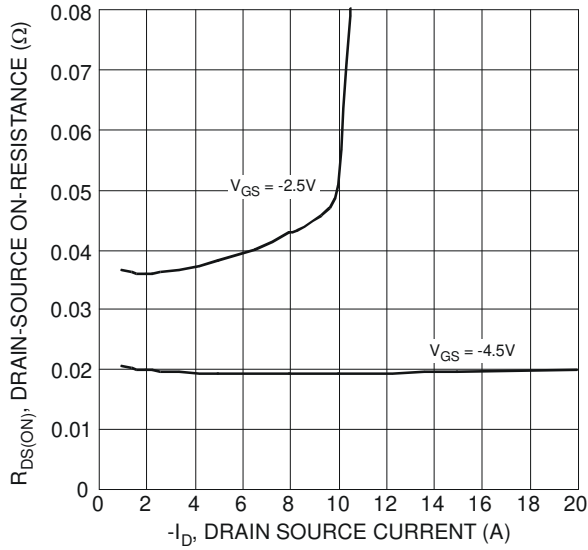


Figure 13 Typical On-Resistance vs. Drain Current and Gate Voltage

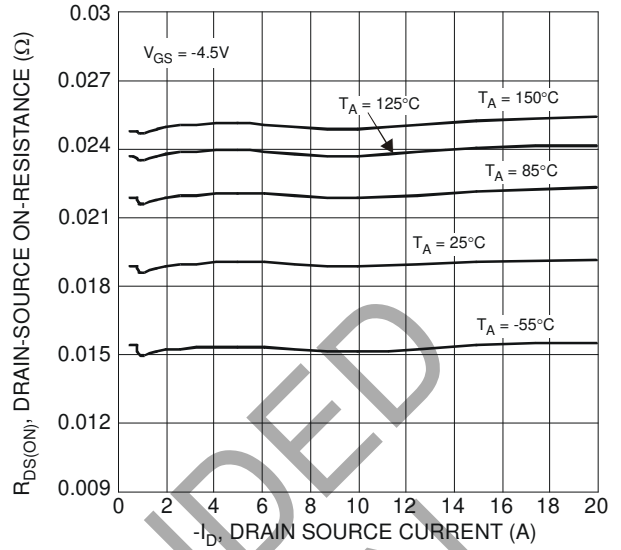


Figure 14 Typical On-Resistance vs. Drain Current and Temperature

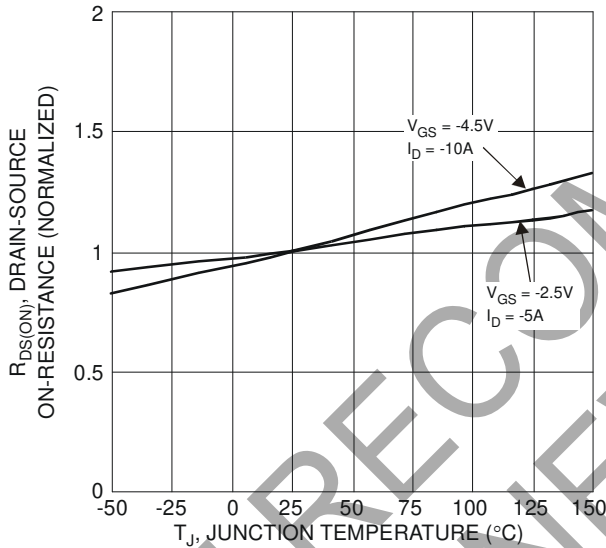


Figure 15 On-Resistance Variation with Temperature

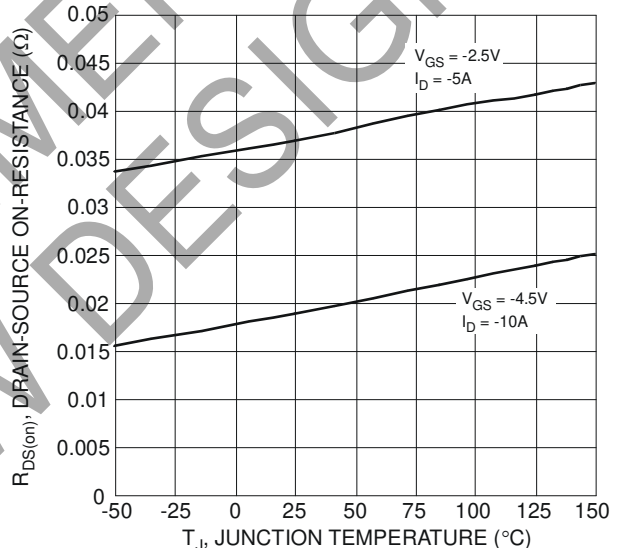


Figure 16 On-Resistance Variation with Temperature

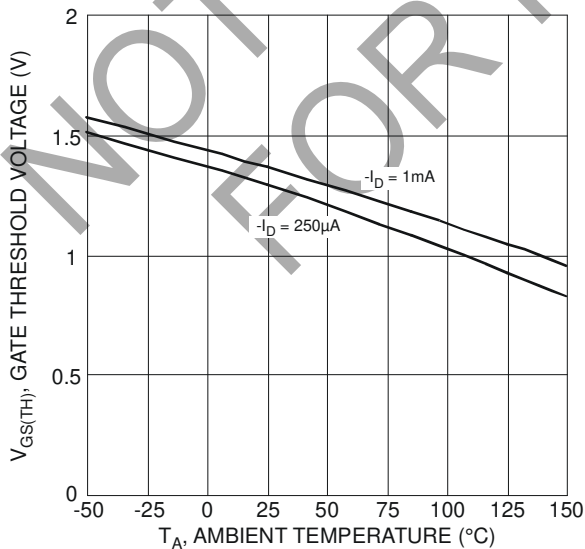


Figure 17 Gate Threshold Variation vs. Ambient Temperature

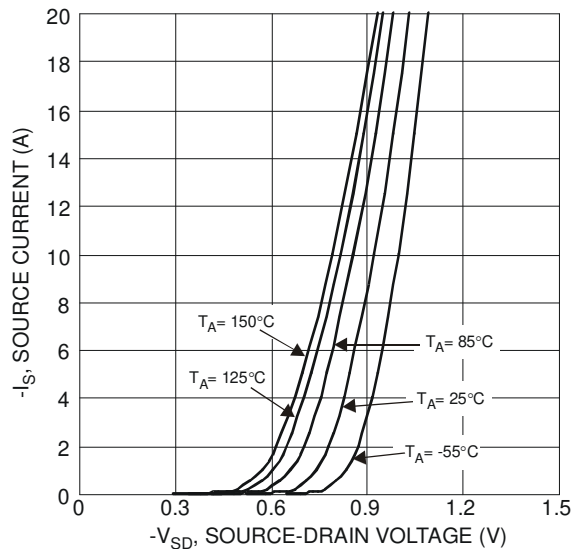


Figure 18 Diode Forward Voltage vs. Current

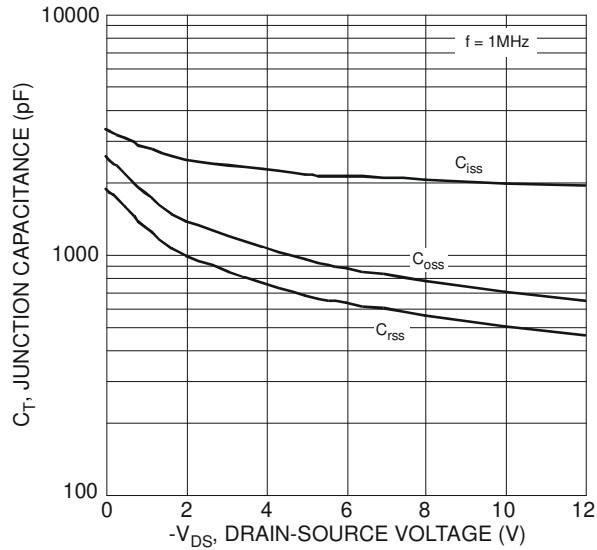


Figure 19 Typical Junction Capacitance

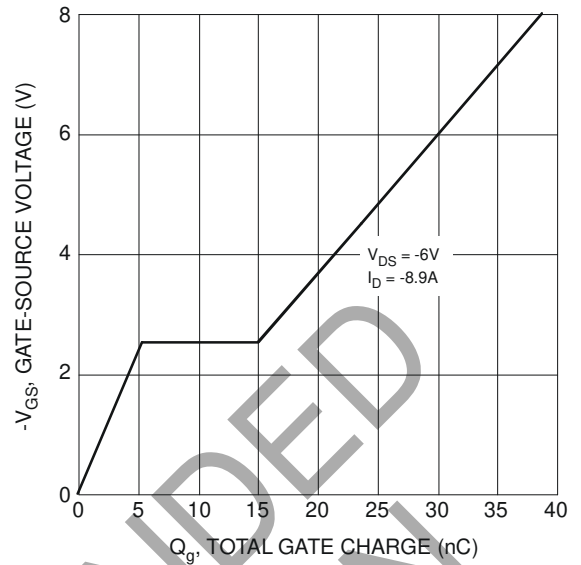


Figure 20 Gate-Charge Characteristics

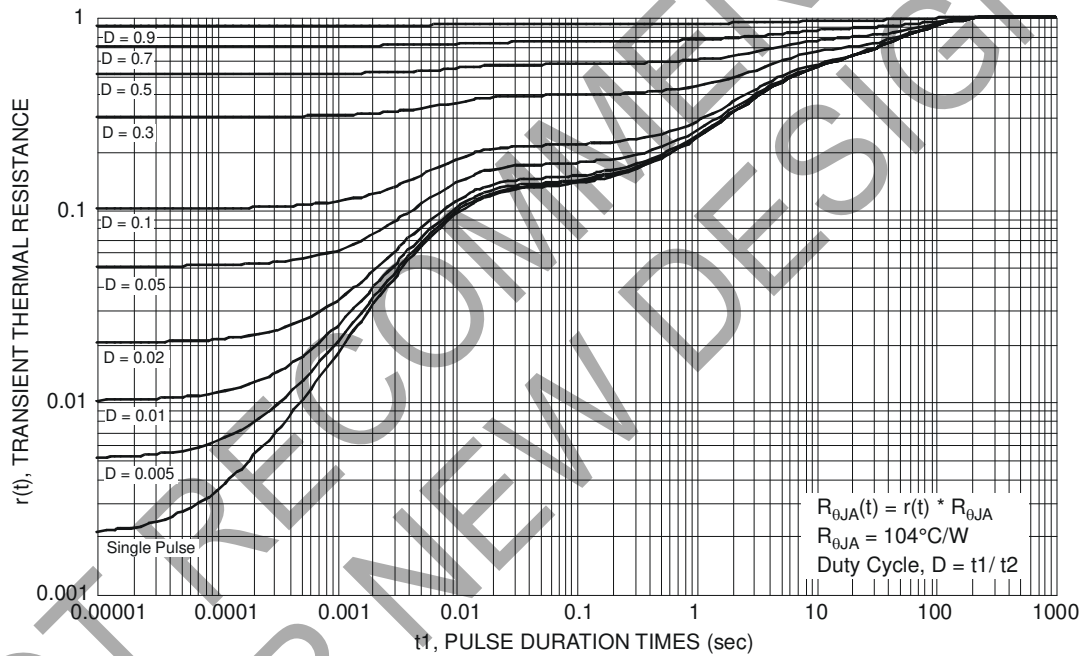


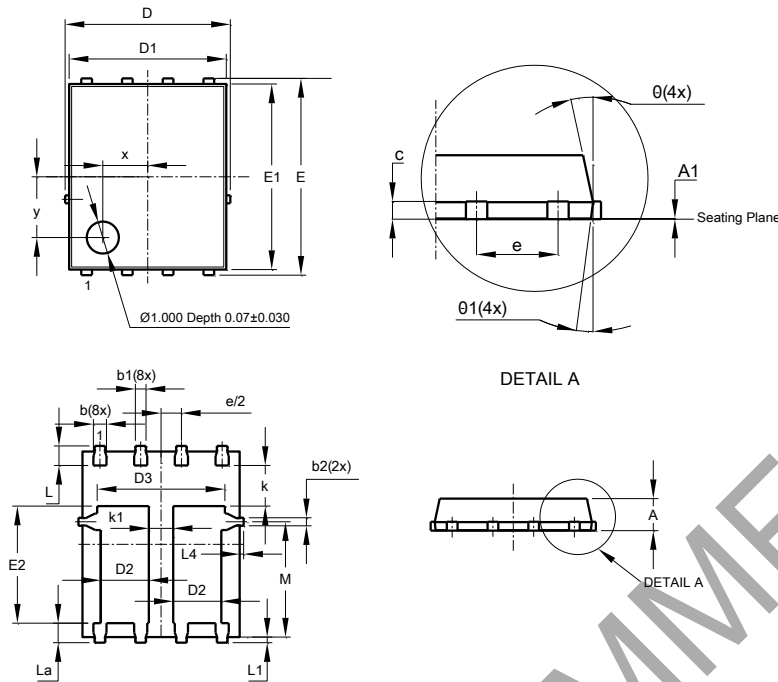
Figure 21 Transient Thermal Resistance

$R_{\theta JA}(t) = r(t) * R_{\theta JA}$
 $R_{\theta JA} = 104^{\circ}\text{C/W}$
 Duty Cycle, $D = t_1 / t_2$

NOT FOR NEW DESIGN

Package Outline Dimensions

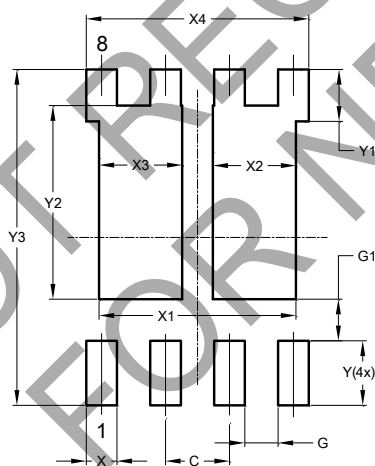
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0	0.05	0.02
b	0.33	0.51	0.41
b1	0.300	0.366	0.333
b2	0.20	0.35	0.25
c	0.23	0.33	0.277
D	5.15 BSC		
D1	4.85	4.95	4.90
D2	1.40	1.60	1.50
D3	-	-	3.98
E	6.15 BSC		
E1	5.75	5.85	5.80
E2	3.56	3.76	3.66
e	1.27 BSC		
k	-	-	1.27
k1	0.56	-	-
L	0.51	0.71	0.61
La	0.51	0.71	0.61
L1	0.05	0.20	0.175
L4	-	-	0.125
M	3.50	3.71	3.605
x	-	-	1.400
y	-	-	1.900
θ	10°	12°	11°
$\theta 1$	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for latest version.



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	1.650
X3	1.650
X4	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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