DUAL 10-A OUTPUTS, 4.75-V to 14-V INPUT, NON-ISOLATED, DIGITAL POWERTRAIN™ MODULE

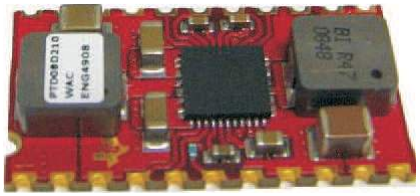
Check for Samples: PTD08D210W

FEATURES

- **Dual 10-A Outputs**
- **4.75-V to 14-V Input Voltage**
- **Programmable Wide-Output Voltage (0.7 V to 3.6 V)**
- **Efficiencies up to 96%**
- **Digital I/O**
  - **PWM signal**
  - **Fault Flag (FF)**
  - **Sychronous Rectifier Enable (SRE)**
- **Analog I/O**
  - **Temperature**
  - **Output currrent**
- **Safety Agency Approvals: (Pending)**
  - **UL/IEC/CSA-C22.2 60950-1**
- **Operating Temperature: –40°C to 85°C**

APPLICATIONS

- **Digital Power Systems using UCD9XXX Digital Controllers**



DESCRIPTION

The PTD08D210W is a high-performance dual 10-A output, non-isolated digital PowerTrain module. This module is the power conversion section of a digital power system which incorporates TI's UCD7242 MOSFET/driver IC. The PTD08D210W must be used in conjunction with a digital power controller such as the UCD9240, UCD9220 or UCD9110 family. The PTD08D210W receives control signals from the digital controller and provides parametric and status information back to the digital controller. Together, PowerTrain modules and a digital power controller form a sophisticated, robust, and easily configured power management solution.

Operating from an input voltage range of 4.75 V to 14 V, the PTD08D210W provides step-down power conversion to a wide range of output voltages from, 0.7 V to 3.6 V. The wide input voltage range makes the PTD08D210W particularly suitable for advanced computing and server applications that utilize a loosely regulated 8-V, 9.6-V or 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V or 12-V intermediate bus architectures.

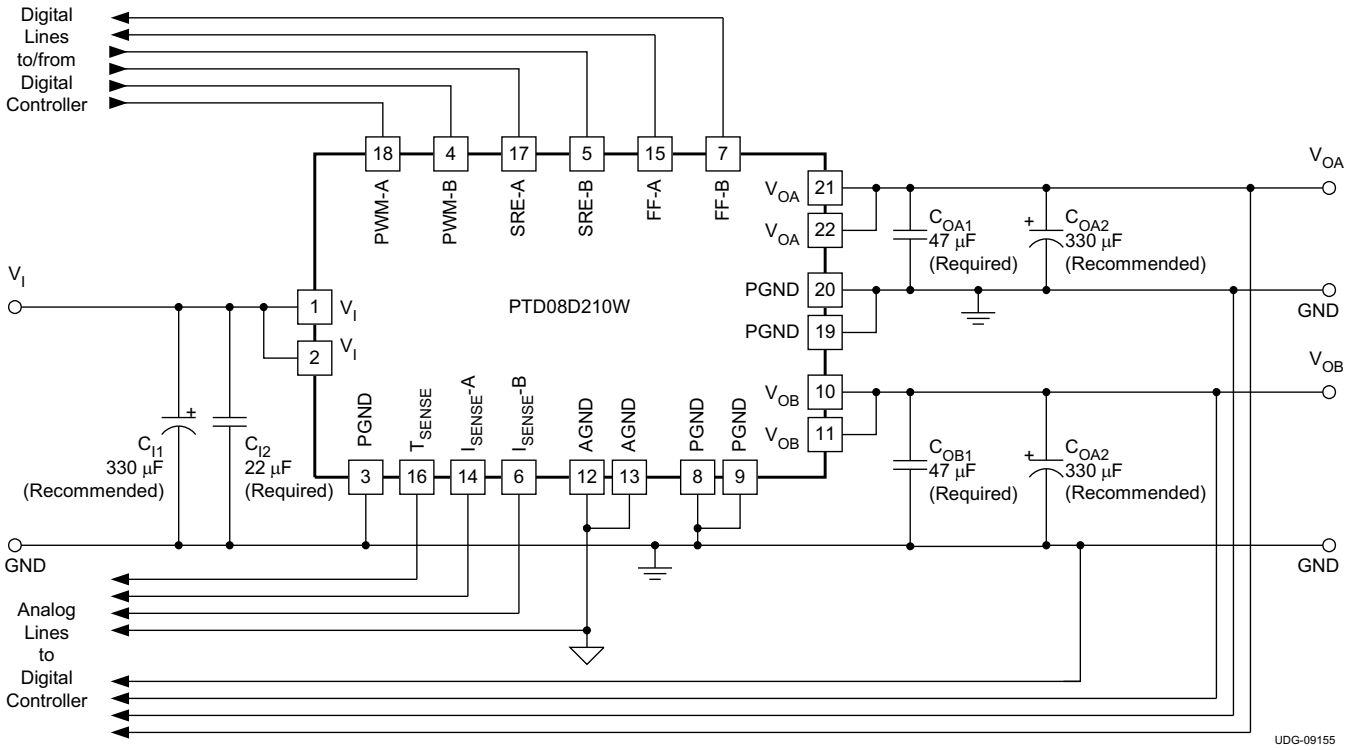
The module incorporates output over-current and temperature monitoring which protects against most load faults. Output current and module temperature signals are provided for the digital controller to permit user defined over-current and over-temperature warning and fault scerarios.

The module uses single-sided, pin-less surface mount construction to provide a low profile and compact footprint. The package is lead (Pb) - free and RoHS compatible.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Standard PTD08D210W Application



ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

DATASHEET TABLE OF CONTENTS

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

				UNIT
V_I	Input voltage		16	V
T_A	Operating temperature range	Over V_I range	–40 to 85	°C
T_{reflow}	Solder reflow temperature	Surface temperature of module body	260(1)	
T_{stg}	Storage temperature		–55 to 125(2)	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted	275	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	10	
	Weight		3.9	grams
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign	13.3	10^6 Hr
	Flammability	Meets UL94V-O		

(1) During reflow do not elevate peak temperature of the module or internal components above the stated maximum.
(2) The shipping tray or tape and reel cannot be used to bake parts at temperatures higher than 65°C.

ELECTRICAL CHARACTERISTICS

PTD08D210W

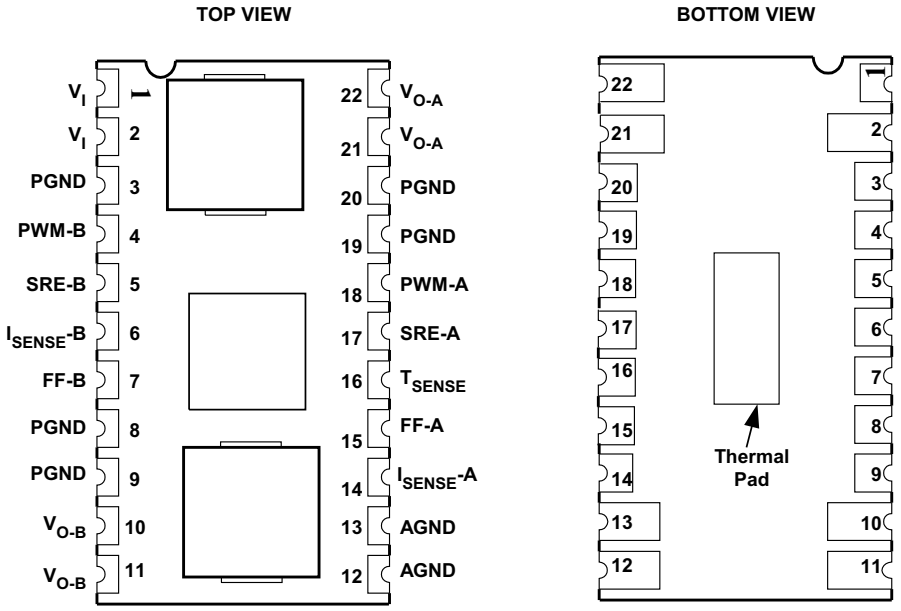
T_A= 25°C, F_{SW}= 750kHz, V_I= 12 V, V_O= 1.2 V, C_{I1}= 330 µF, C_{I2}= 22 µF ceramic, C_{O1}= 47 µF ceramic, C_{O2}= 330 µF, I_O= $I_{O(max)}$, single output (unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTD08D210W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection	0		10	A
V_I	Input voltage range	Over I_O range		4.75		14	V
V_{OADJ}	Output voltage adjust range	Over I_O range		0.7		3.6 (1)	V
η	Efficiency	I_O = 10 A, *f*s = 750 kHz	V_O = 3.3 V		92.8%		
			V_O = 2.5 V		91.4%		
			V_O = 1.8 V		89.1%		
			V_O = 1.5 V		87.7%		
			V_O = 1.2 V		85.6%		
			V_O = 1.0 V		84.0%		
V_{OPP}	V_O Ripple (peak-to-peak)	20-MHz bandwidth			11		mV_{PP}
I_B	Bias current	PWM & SRE to AGND	Standby		6		mA
V_{IH}	High-level input voltage	SRE & PWM input levels		2.0		5.5	V
V_{IL}	Low-level input voltage					0.8	
	PWM input	Frequency range		500 (1)		1000	kHz
		Pulse width limits		20			ns
	TEMP output	Range		-40		125	°C
		Accuracy, -40°C ≤ T_A ≤ 85°C		-5		5	°C
		Slope			10		mV/°C
		Offset, T_A = 25°C			720		mV
V_{OH}	FAULT output	High-level output voltage, I_{FAULT} = 4mA		2.7	3.3		V
V_{OL}		Low-level output voltage, I_{FAULT} = 4mA			0	0.6	
I_{LIM}		Overcurrent threshold; Reset, followed by auto-recovery			15 (2)		A
	IOUT output	Range		0.15		3.5	V
		Gain, 3A ≤ I_O ≤ 10A		188	200	212	mV/A
		Offset, I_O = 0A, V_O = 1.2V		0	0.3	0.76	V
		Output Impedance			10		kΩ
C_I	External input capacitance		Nonceramic		330 (3)		µF
			Ceramic	22 (3)			
C_O	External output capacitance	Capacitance Value	Nonceramic		330 (4)	5000 (5)	µF
			Ceramic	47 (4)			
		Equivalent series resistance (non-ceramic)		1 (6)			mΩ

(1) When operating at 12V input and 500kHz, V_O is limited to ≤ 2.0V.
(2) The current limit threshold is the sum of I_O and the peak inductor ripple current.
(3) A 22 µF ceramic input capacitor is required for proper operation. An additional 330 µF bulk capacitor rated for a minimum of 500mA rms of ripple current is recommended. When operating at frequencies > 500kHz the 22 µF ceramic capacitor is only recommended. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(4) A 47 µF ceramic output capacitor is required for basic operation. An additional 330 µF bulk capacitor is recommended for improved transient response. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(5) 5,000 µF is the calculated maximum output capacitance given a 1V/msec output voltage rise time. Additional capacitance or increasing the output voltage rise rate may trigger the overcurrent threshold at start-up. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(6) This is the minimum ESR for all non-ceramic output capacitance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	1, 2	The positive input voltage power node to the module, which is referenced to common GND.
PGND	3, 8, 9, 19, 20	The common ground connection for the V_I and V_O power connections.
V_{OA}	21, 22	The regulated positive power A output with respect to GND.
V_{OB}	10, 11	The regulated positive power B output with respect to GND.
I_{SENSE}-A	14	Current sense A output. The voltage level on this pin represents the average output current of the module.
I_{SENSE}-B	6	Current sense B output. The voltage level on this pin represents the average output current of the module.
PWM-A	18	This is the PWM A input pin. It is a high impedance digital input that accepts 3.3-V or 5-V logic level signals up to 1 MHz.
PWM-B	4	This is the PWM B input pin. It is a high impedance digital input that accepts 3.3-V or 5-V logic level signals up to 1 MHz.
FF-A	15	Current limit fault flag A. The Fault signal is a 3.3-V digital output which is latched high after an over-current condition. The Fault is reset after a complete PWM cycle without an over-current condition (falling edge of the PWM).
FF-B	7	Current limit fault flag A. The Fault signal is a 3.3-V digital output which is latched high after an over-current condition. The Fault is reset after a complete PWM cycle without an over-current condition (falling edge of the PWM).
SRE-A	17	Synchronous Rectifier Enable A. This pin is a high impedance digital input. A 3.3 V or 5 V logic level signals is used to enable the synchronous rectifier switch. When this signal is high, the module will source and sink output current. When this signal is low, the module will only source current.
SRE-B	5	Synchronous Rectifier Enable B. This pin is a high impedance digital input. A 3.3 V or 5 V logic level signals is used to enable the synchronous rectifier switch. When this signal is high, the module will source and sink output current. When this signal is low, the module will only source current.
AGND	12, 13	Analog ground return. It is the 0 V_{dc} reference for the control inputs.
T_{SENSE}	16	Temperature sense output. The voltage level on this pin represents the temperature of the module.
Thermal Pad		This pad is electrically connected to PGND and is the primary thermal conduction cooling path for the module. This pad should be soldered to a grounded copper pad on the host board. For optimum cooling performance, the grounded copper pad should also be tied with multiple vias to the host board internal ground plane. See the Land Pattern drawing for package EFS for recommended pad dimensions.



TYPICAL CHARACTERISTICS (V_I = 12 V)

(1)(2)

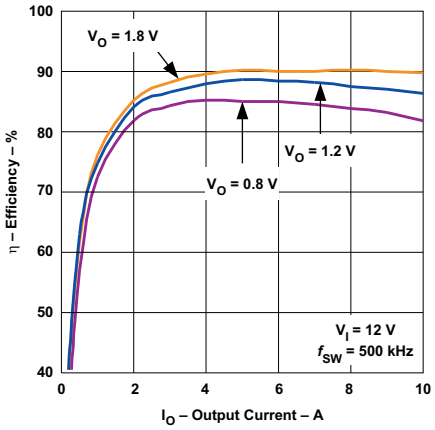


Figure 1. Efficiency

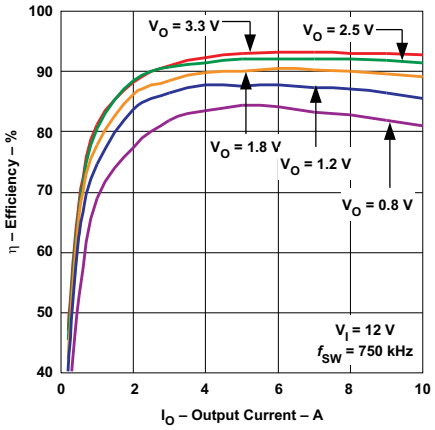


Figure 2. Efficiency

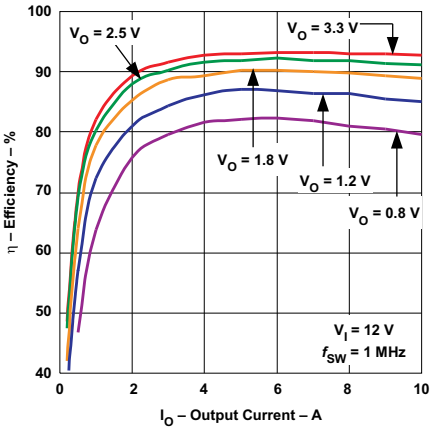


Figure 3. Efficiency

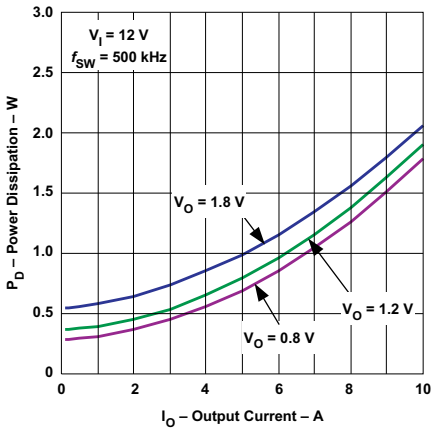


Figure 4. Power Dissipation

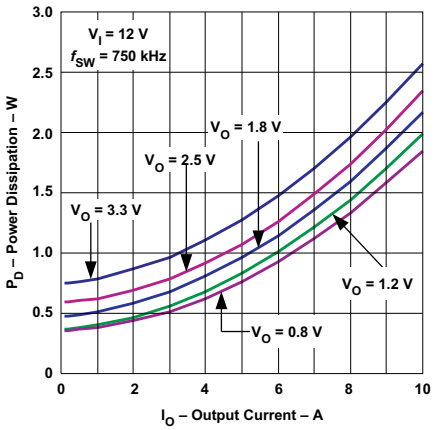


Figure 5. Power Dissipation

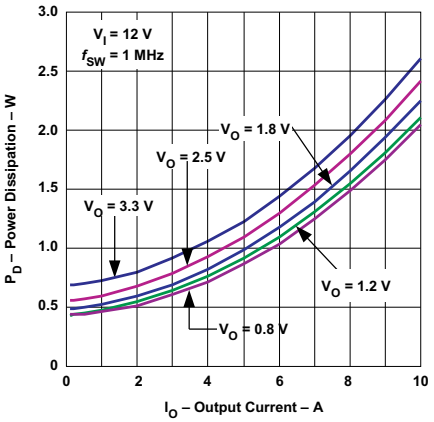


Figure 6. Power Dissipation

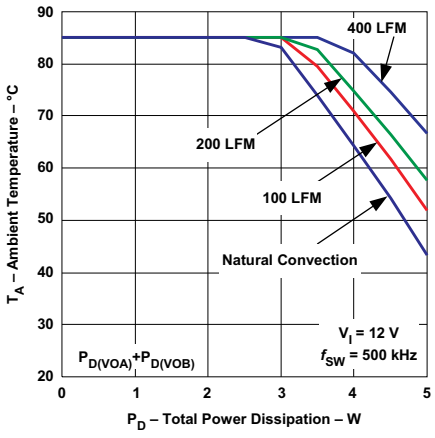


Figure 7. Safe Operating Area

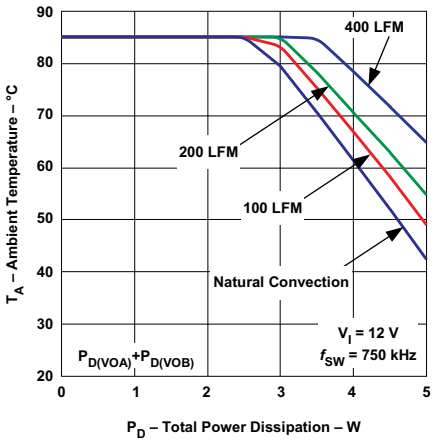


Figure 8. Safe Operating Area

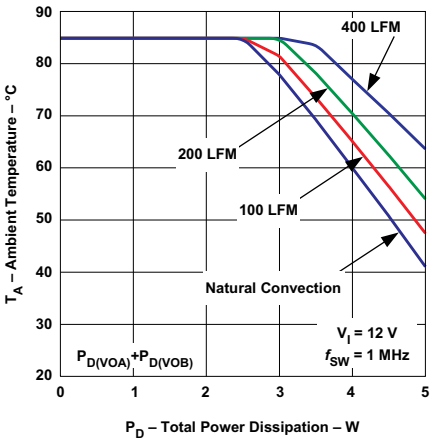


Figure 9. Safe Operating Area

(1) The electrical characteristic data (Figure 1 through Figure 6) has been developed from actual products tested at 25°C. This data is considered typical for the converter.

(2) The temperature derating curves (Figure 7 through Figure 9) represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2-oz. copper. See the Safe Operating Area application section of this datasheet.

TYPICAL CHARACTERISTICS (V_I = 5 V)

(1)(2)

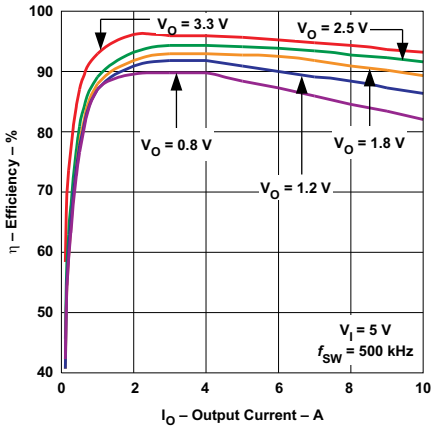


Figure 10. Efficiency

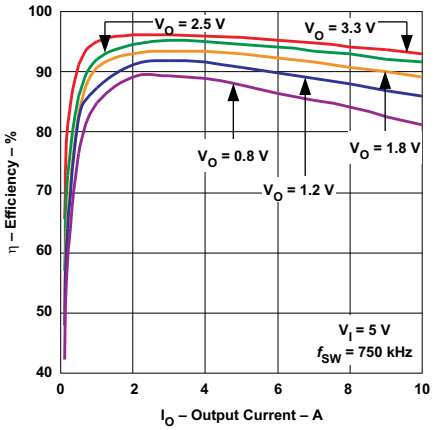


Figure 11. Efficiency

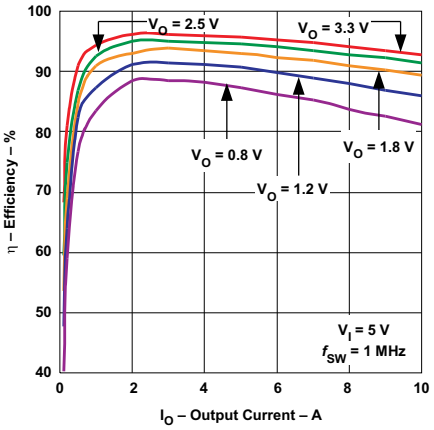


Figure 12. Efficiency

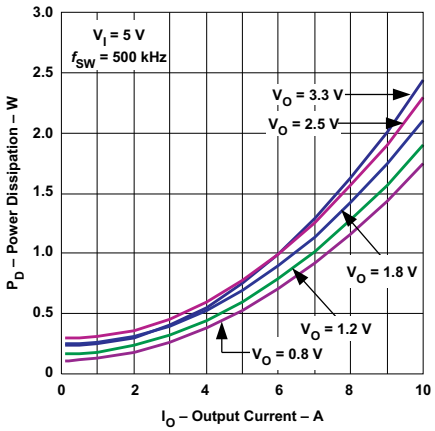


Figure 13. Power Dissipation

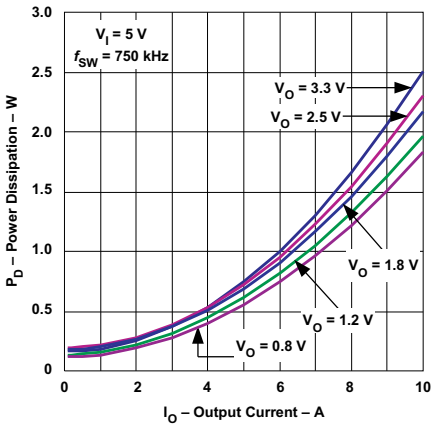


Figure 14. Power Dissipation

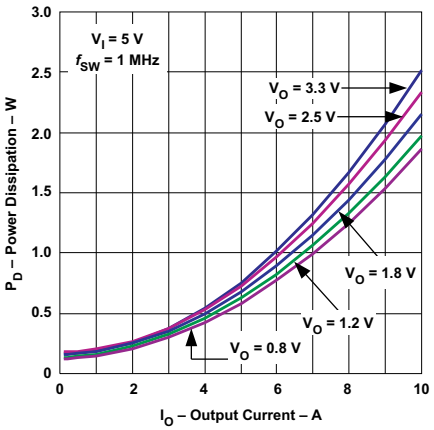


Figure 15. Power Dissipation

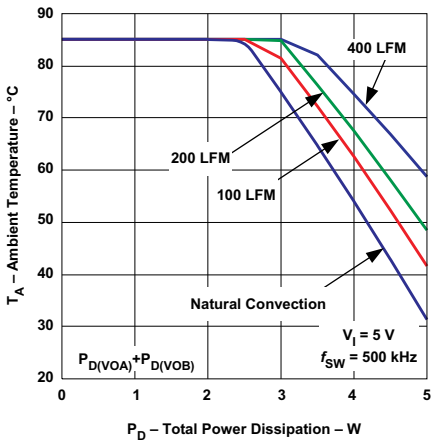


Figure 16. Safe Operating Area

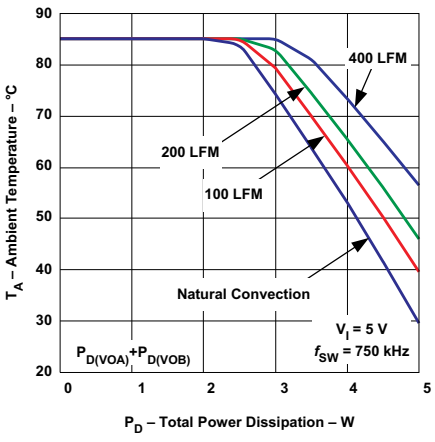


Figure 17. Safe Operating Area

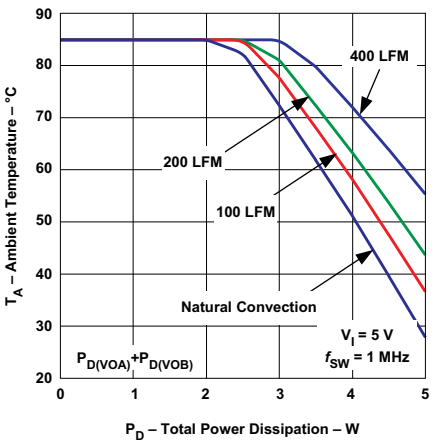


Figure 18. Safe Operating Area

(1) The electrical characteristic data (Figure 10 through Figure 15) has been developed from actual products tested at 25°C. This data is considered typical for the converter.

(2) The temperature derating curves (Figure 16 through Figure 18) represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2-oz. copper. See the Safe Operating Area application section of this datasheet.

TYPICAL CHARACTERISTICS

CURRENT SENSE OUTPUT VS OUTPUT CURRENT

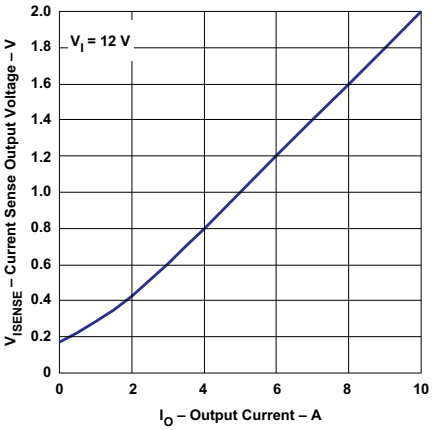


Figure 19.

CURRENT SENSE OUTPUT VS OUTPUT CURRENT

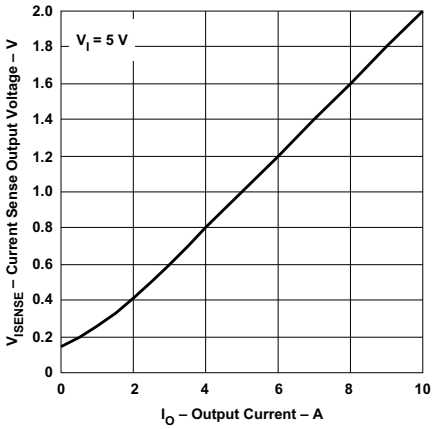


Figure 20.

TEMPERATURE SENSE VS JUNCTION TEMPERATURE

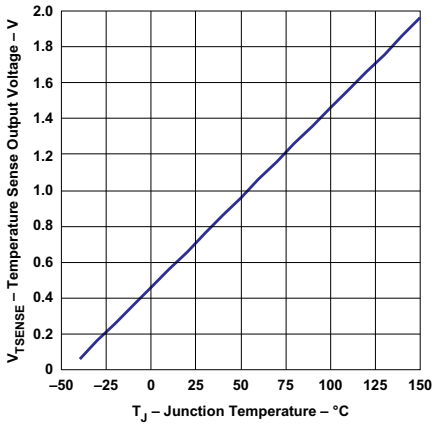
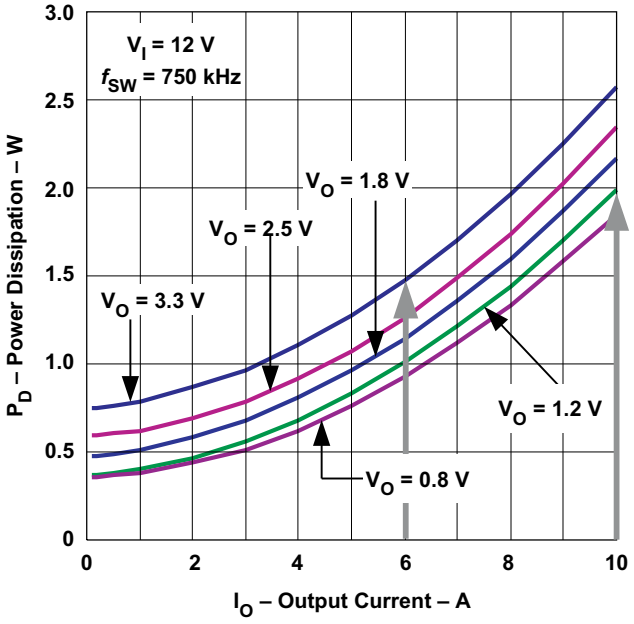
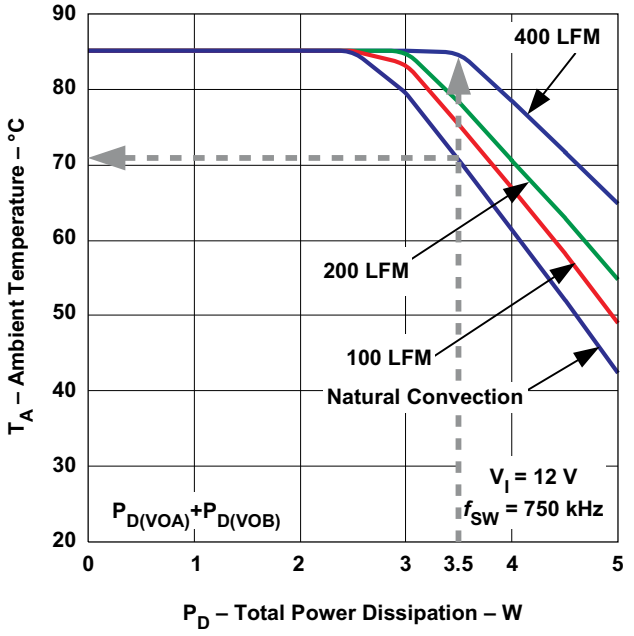


Figure 21.

APPLICATION INFORMATION

Determining the Safe Operating Area





The Safe Operating Area (SOA) curves for the PTD08D210W are determined by the total power dissipation of the module, the maximum ambient temperature, and the minimum available airflow of the application. Operation below the application airflow curve is considered a thermally safe design. For a given SOA, refer to the Power Dissipation curves for the same input voltage and switching frequency to determine each output's power dissipation. Add the power dissipation of V_{OA} and V_{OB} to get the total power dissipation. The total power dissipation can then be used to determine the safe operating area for the application.

For example, consider an application operating from a 12-V input and a 750-kHz switching frequency, requiring 1.2 V @ 10 A and 3.3 V @ 6 A outputs. In order to determine the safe operating area the power dissipation for each of the outputs must first be determined. Using the *V_I = 12 V, f_{SW} = 750 kHz Power Dissipation* graph, the power dissipation for the 1.2 V @ 10 A output is 2 W and the power dissipation for the 3.3 V @ 6 A output is 1.5 W. Adding the power dissipation for both outputs results in a total power dissipation of 3.5 W. The safe operating area can then be determined using the *V_I = 12V, f_{SW} = 750 kHz SOA* graph, the amount of airflow of the application and the 3.5-W total power dissipation. At 3.5 W and 400 LFM, the application can operate up to 85°C, but when no airflow is available the maximum ambient temperature is limited to less than 71°C.

NOTE

- Graphs above have been replicated from the *Typical Characteristics* section for this example
- The maximum output current for either output must not exceed 10 A.

Digital Power

Figure 22 shows the UCD9220 power supply controller working with a single PTD08D210W, dual-output module regulating two independent power supplies. The loop for each power supply is created by the respective voltage outputs feeding into the Error ADC differential inputs, and completed by DPWM outputs feeding the PTD08D210W module.

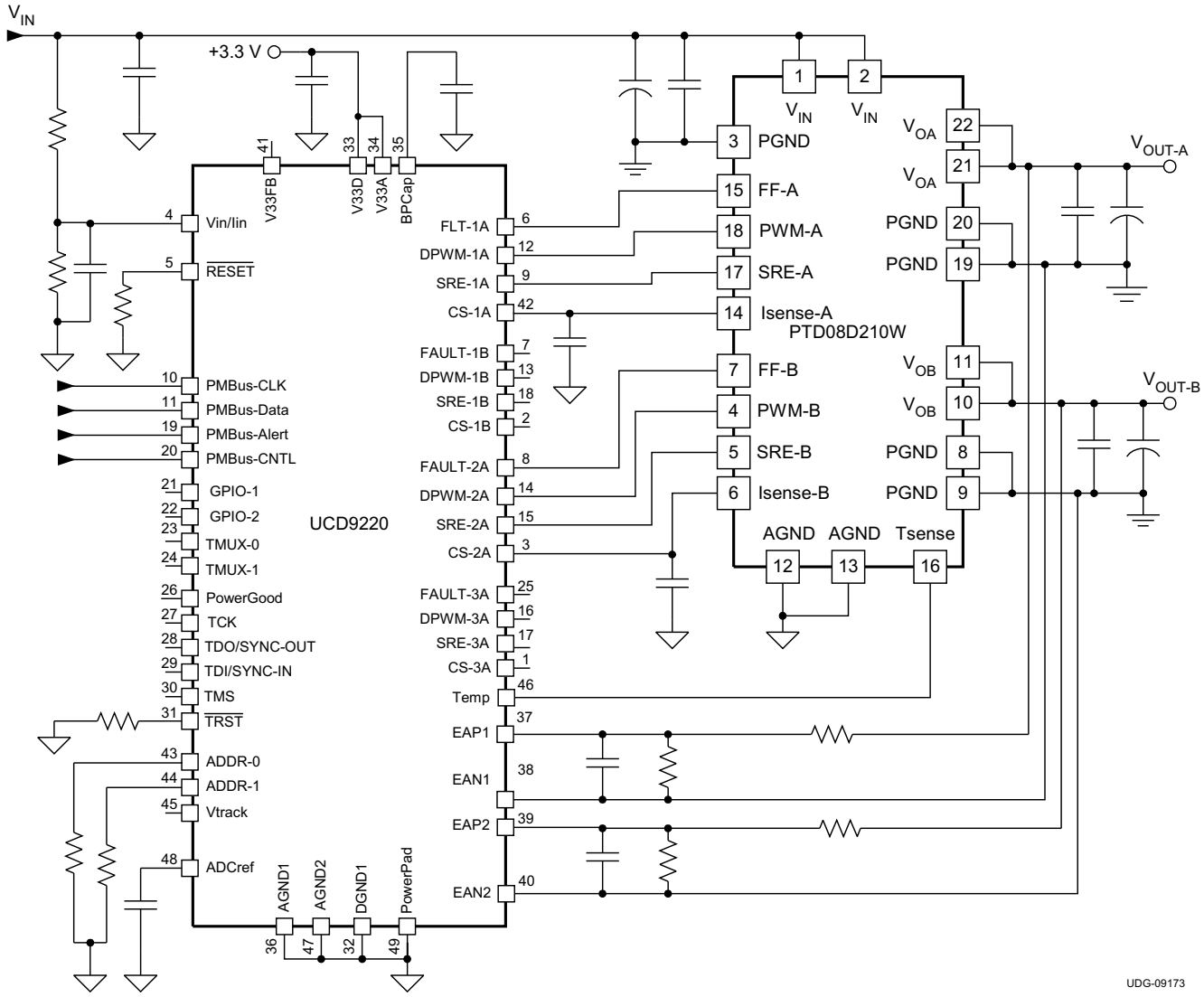


Figure 22. Typical Dual-Output Application Schematic

Note: A low dropout linear regulator such as the TI TPS715A33 can provide the 3.3-V bias power to the UCD9220.

Figure 23 shows the UCD9220 power supply controller working with a single PTD08D210W power module. The dual outputs of the PTD08D210W have been paralleled, allowing up to 20A of output current. When operating the PTD08D210W in parallel configuration the dual inputs must be tied together and driven from a single output of the digital power controller. **Multiple PTD08D210W modules must not be paralleled.**

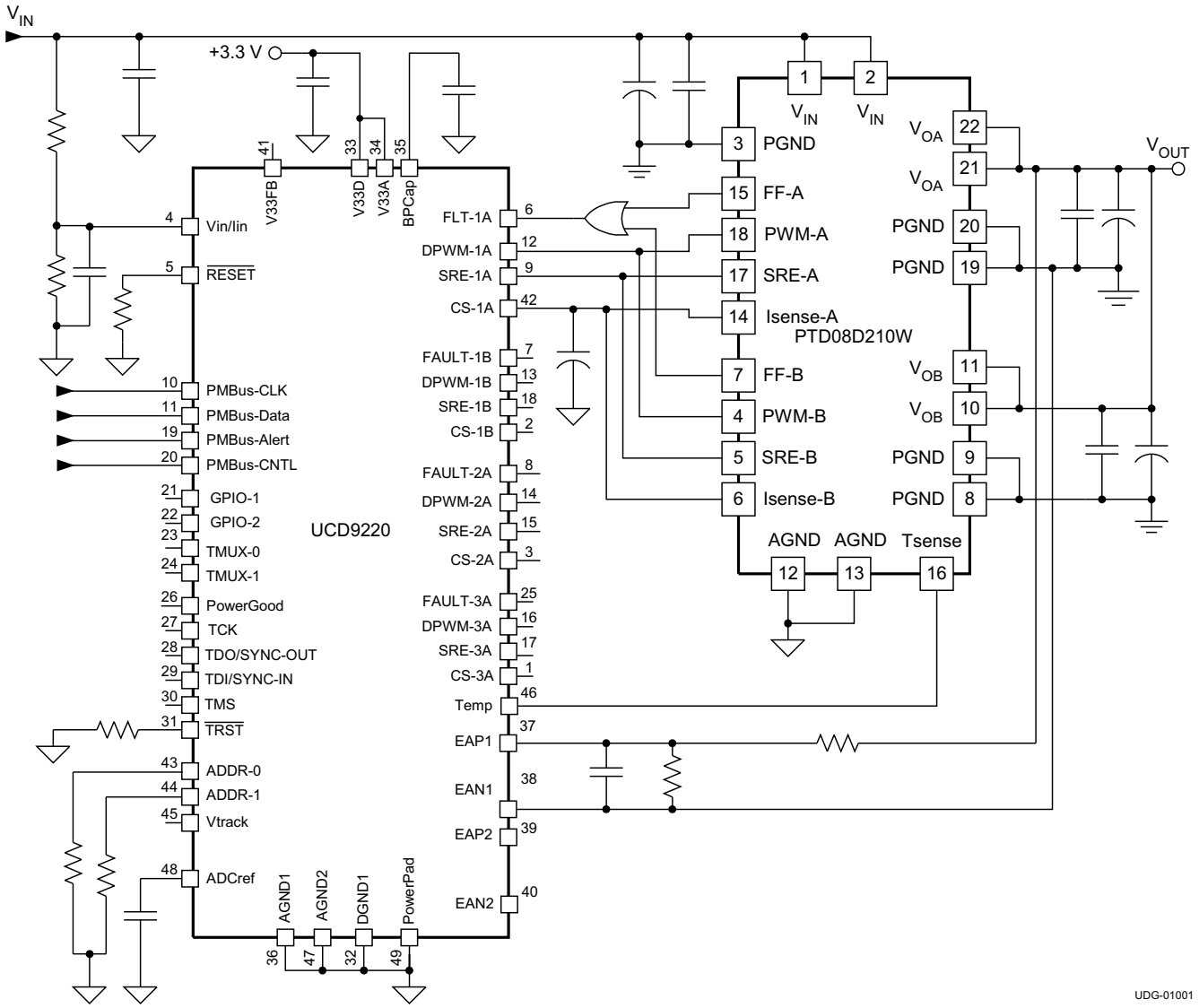


Figure 23. Typical Paralleled-Output Application Schematic

Note 1: A low dropout linear regulator such as the TI TPS715A33 can provide the 3.3-V bias power to the UCD9220.

Note 2: An OR-gate such as the TI 74LVC1G32 should be used to sense a fault signal on either FF-A or FF-B.

UCD9240 Graphical User Interface (GUI)

When using the UCD92x0 digital controller along with digital PowerTrain modules to design a digital power system, several internal parameters of the modules are required to run the Fusion Digital Power Designer GUI. See the plant parameters below for the PTD08D210W digital PowerTrain modules.

Table 1. PTD08D210W Plant Parameters

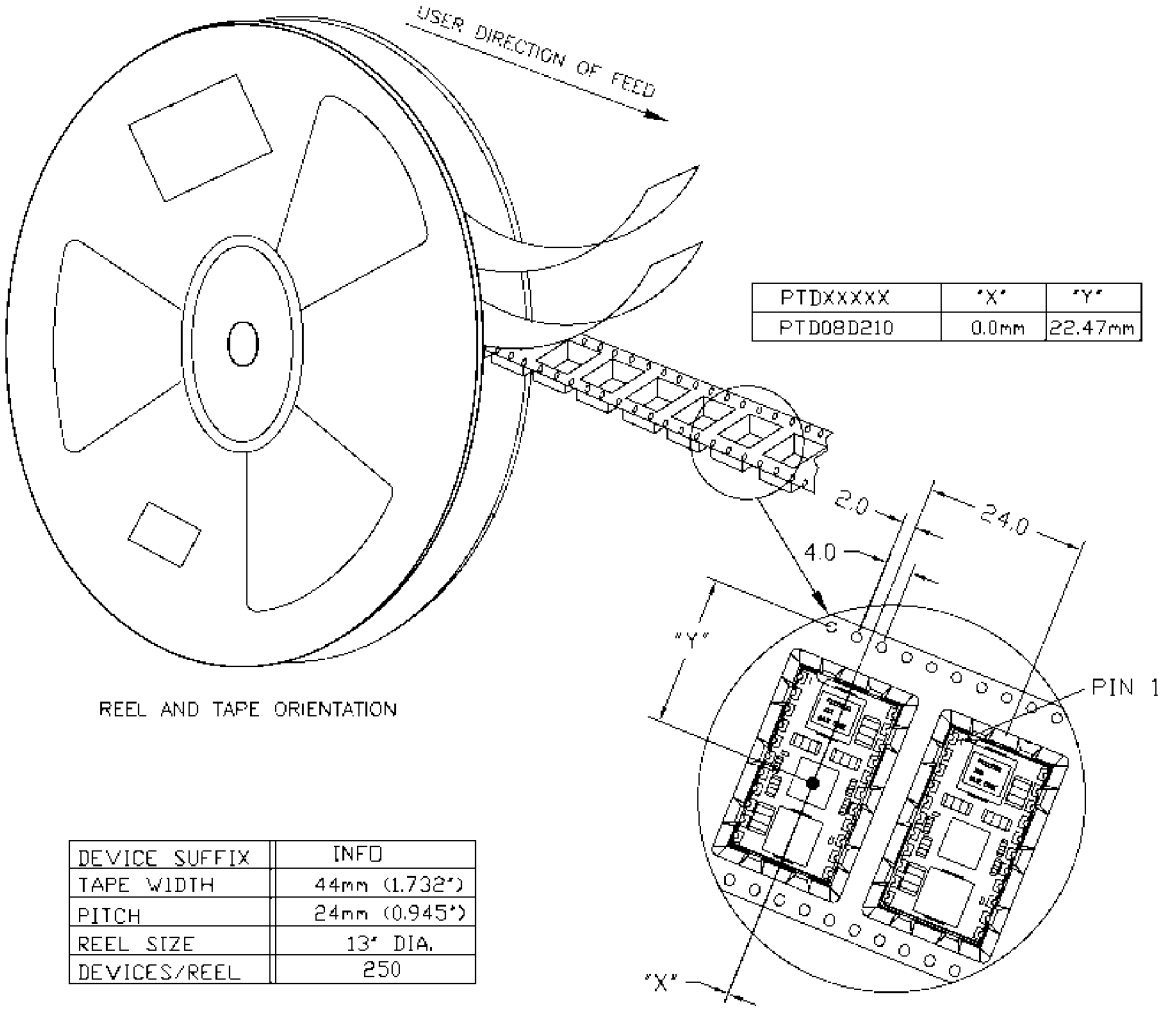
PTD08D210W Plant Parameters			
L (µH)	**DCR (mΩ)**	**$R_{DS(on)}$-high (mΩ)**	**$R_{DS(on)}$-low (mΩ)**
0.47	2.6	15.5	6.5

Internal output capacitance is present on the digital PowerTrain modules themselves. When using the GUI interface this capacitance information must be included along with any additional external capacitance. See the capacitor parameters below for the PTD08D210W digital PowerTrain modules.

Table 2. PTD08D210W Capacitor Parameters

PTD08D210W Capacitor Parameters			
C (µF)	**ESR (mΩ)**	**ESL (nH)**	**Quantity**
47	1.5	2.5	1

TAPE & REEL

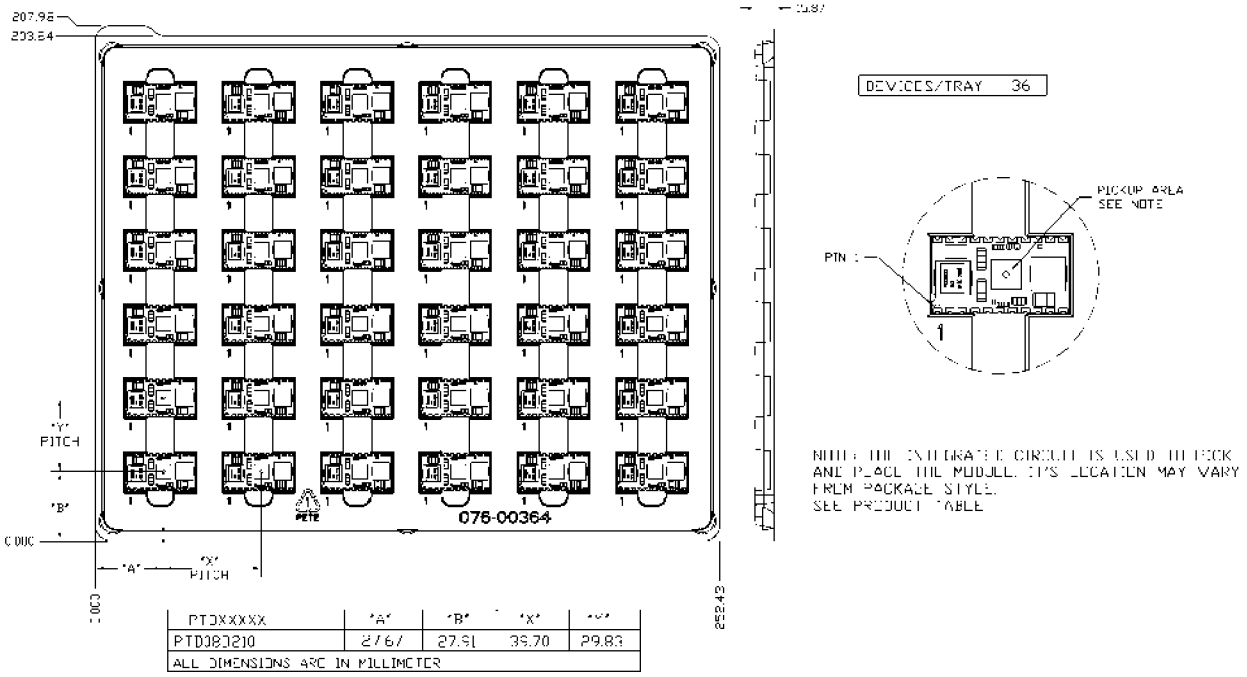


REEL AND TAPE ORIENTATION

PTDxxxxx	"X"	"Y"
PTD08D210	0.0mm	22.47mm

DEVICE SUFFIX	INFO
TAPE WIDTH	44mm (1.732")
PITCH	24mm (0.945")
REEL SIZE	13" DIA.
DEVICES/REEL	250

TRAY



PTDXXXXX	"A"	"B"	"X"	"Y"
PTD08D210	27.67	27.91	39.70	29.83
ALL DIMENSIONS ARE IN MILLIMETER				

NOTE: THE INTEGRATED CIRCUIT IS USED TO PICK AND PLACE THE MODULE. IT'S LOCATION MAY VARY FROM PACKAGE STYLE. SEE PRODUCT TABLE

REVISION HISTORY

Changes from Revision A (FEBRUARY 2010) to Revision B	Page
• Added Caution regarding paralleling multiple modules.	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTD08D210WAC	ACTIVE	DIP MODULE	EFS	22	36	RoHS (In Work) & Green (In Work)	Call TI	Level-3-260C-168 HR	-40 to 85		Samples
PTD08D210WACT	ACTIVE	DIP MODULE	EFS	22	250	RoHS (In Work) & Green (In Work)	Call TI	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

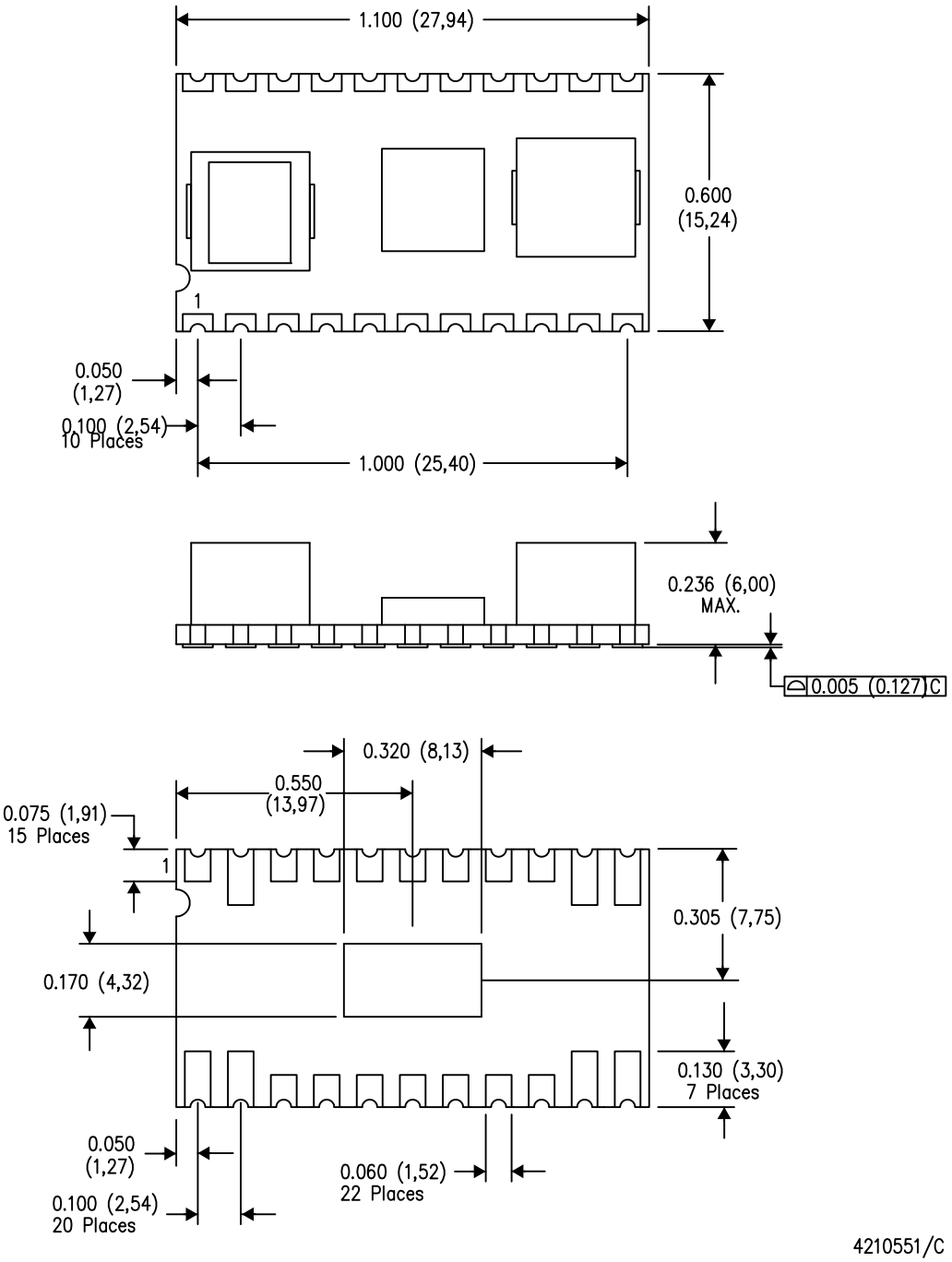
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

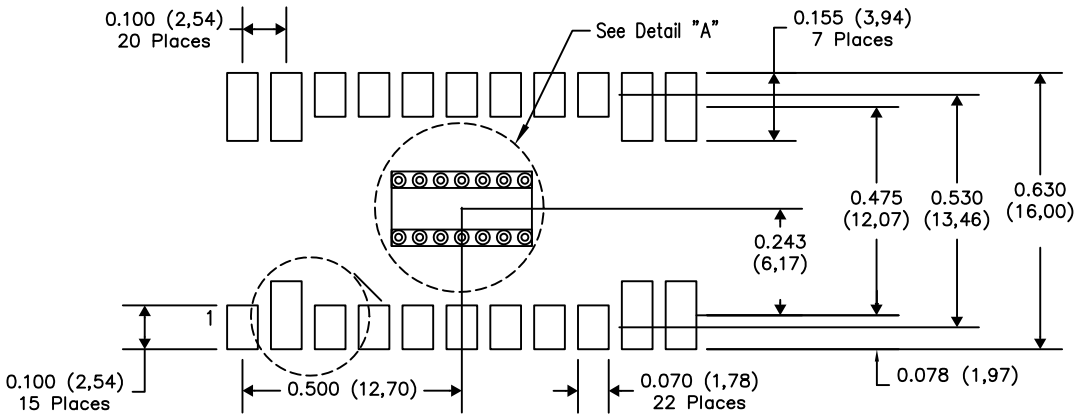
EFS (R–PDSS–T22) SINGLE SIDED MODULE



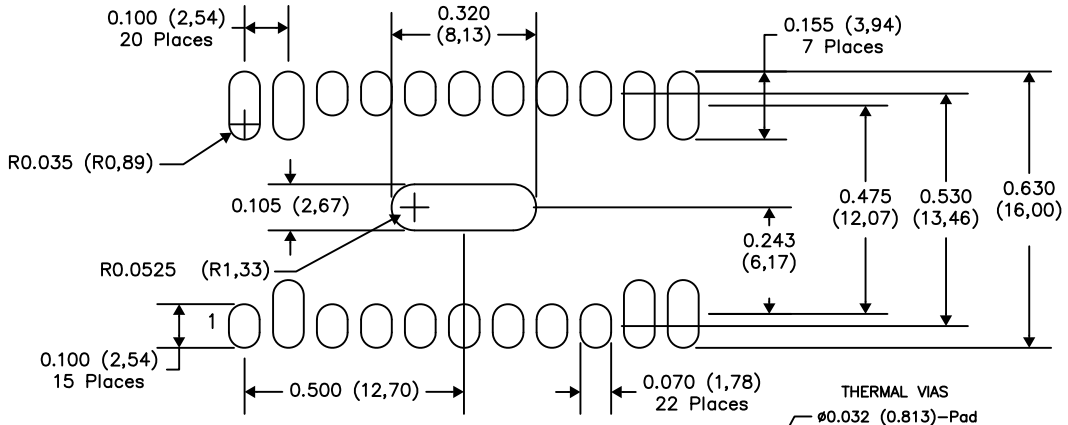
NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).

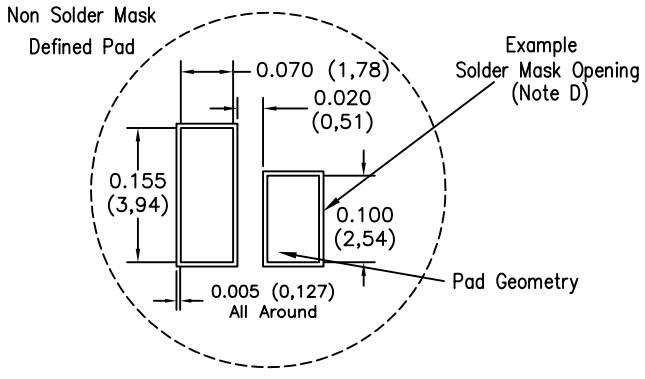
EFS (R–PDSS–T22) SINGLE SIDED MODULE

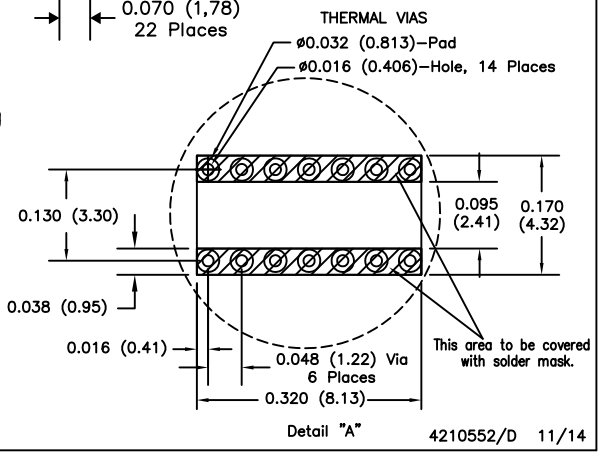
Example Board Layout



Example Stencil Design (Note E & F)







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NOTES:
A. All linear dimensions are in inches & millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. This pad must be at ground potential and be connected to an internal ground plane with multiple thermal vias.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Paste screen thickness: 0.006 (0,15).
G. 3 place decimals are ±0.010 (±0.25)

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