

TLC4541/5EVM, TLC3541/5EVM, TLC2551/2/5EVM AND TLV2541/2/5EVM

User's Guide

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of \pm 12 V and the output voltage range of 0 V and +5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C. The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated

Preface

Read This First

About This Manual

This user's guide describes the EVM used to evaluate ten different serial analog-to-digital converters. These converters are the TLC4541/5, TLC3541/5, TLC2551/2/5, and TLV2541/2/5; 16-bit, 14-bit, 12-bit, and 12-bit devices respectfully. A complete circuit description as well as a schematic and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

Chapter 1 - EVM Overview

Chaper 2 - Layout

Chapter 3 - EVM Bill of Materials and EVM Schematic

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, please identify this booklet by its title and literature number. Updated documents can also be obtained through our website at <a href="https://www.ti.com/www.ti.

Data Sheets	Literature Numbers
TLV2541/2/5	SLAS245
TLC2551/2/5	SLAS276
TLC3541/5	SLAS345
TLC4541/5	SLAS293
OPA132	SBOS054
REF102	SBVS003
SN74HC1G125DBV	SCLS377

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

1	EVM	1 Overview	1-1
	1.1	Introduction	1-2
	1.2	Features	1-2
	1.3	Default Jumper Settings	
	1.4	Analog Interface	
	1.5	Digital Interface	
	1.6	Power Supplies	
	1.7	Voltage References	
	1.8	EVM Operation	1-5
2	Lavo	out	2-1
	•		
3		1 Bill of Materials and EVM Schematic	
	3.1	EVM Bill of Materials	
	3.2	EVM Schematic	3-3
		Eiguro	
		Figure	3
=			=
2-1		Top Assembly Layer	
2-2		Ground Plane Layer	
2-3		Voltage Plane Layer	
2-4	1 I	Bottom Assembly (Viewed From Top)	2-3
		Table	9
		Table	. J
		Cia ala lagrat Ohannal	4 0
1-1 1-2		Single Input Channel	
1-2		Dual Input Channels	
1-3		TLC4541EVM, TLC3541EVM, TLC2551EVM, and TLV2541EVM	
1-5		TLC4545EVM, TLC3545EVM, TLC2552/5EVMs, and TLV2542/5EVMs	
1-6		Analog Input Connector J1	
1-7		Digital Connector J2	
3-1		EVM Bill of Materials	
- '			

Chapter 1

EVM Overview

This chapter provides an overview of the TLC4541/5EVM, TLC3541/5EVM, TLC2551/2/5EVM and TLV2541/2/5EVM.

Topi		Page
1.1	Introduction	1-2
1.2	Features	1-2
1.3	Default Jumper Settings	1-3
1.4	Analog Interface	1-4
1.5	Digital Interface	1-4
1.6	Power Supplies	1-5
1.7	Voltage References	1-5
1.8	EVM Operation	1-5

1.1 Introduction

The series of TLC4541/5, TLC3541/5, TLC2551/2/5 and TLV2541/2/5 are high-performance low-power, miniature, CMOS, serial analog to digital converters (ADCs). The low power performance of these ADCs is further enhanced by an auto-power-down mode incorporated in each series. Three series of the devices run at a maximum sample rate of 200 Ksps and have their own internal conversion clock. The TLC2551/2/5 series runs at 360 Ksps and uses the external SCLK for conversion.

The EVM is designed to accommodate all of the above devices. The analog input signal is buffered through an operational amplifier follower. The data output (DO) signal, from the device under test (DUT), is conditioned through a digital buffer. An on-board voltage reference is generated and buffered to drive the DUT. An off-board reference, which is user optional, can be supplied by reconfiguring jumper (W3). The analog electronics operates with bipolar or unipolar power supplies, by changing two jumpers.

1.2 Features

The EVM is a full featured board designed to accommodate ten serial ADCs. Device types and resolutions are listed in the following tables:

Table 1-1. Single Input Channel

Device	Resolution
TLC4541	16 Bits
TLC3541	14 Bits
TLC2551	12 Bits
TLV2541	12 Bits

Table 1-2. Pseudo DIfferential Input Channels

Device	Resolution
TLC4545	16 Bits
TLC3545	14 Bits
TLC2555	12 Bits
TLV2545	12 Bits

Table 1-3. Dual Input Channels

Device	Resolution
TLC2552	12 Bits
TLV2542	12 Bits

1.3 Default Jumper Settings

Table 1-4. TLC4541EVM, TLC3541EVM, TLC2551EVM, and TLV2541EVM

Designator		1-2	2-3
W1	Enables reference offset for single-supply amplifier U1	Not installed	N/A
W2	Connects or bypasses buffer U1 to DUT	Not installed	Installed
W3	Connects onboard or offboard REF	Installed	Not installed
W4	Connects FS to pin 7 on single input DUTs	Not installed	Installed
W5	Connects - SCLK to pin 5 for single input ADCs	Installed	Not installed
W6	Connects either +Va or +5 V to positive power pin of op-amps U1 and U3	Installed	Not installed
W7	Connects either –Va or GND to negative power pin of op-amps U1 and U3	Installed	Not installed

Table 1-5. TLC4545EVM, TLC3545EVM, TLC2552/5EVMs, and TLV2542/5EVMs

Designator		1-2	2-3
W1	Enables reference offset for single-supply amplifier U1	Not installed	N/A
W2	Connects or bypasses buffer U1 to DUT	Not installed	Installed
W3	Connects onboard or offboard REF	Installed	Not installed
W4	Connects SCLK to pin 7 on dual input DUTs	Installed	Not installed
W5	Connects -AIN0 to pin 5 on dual input DUT	Not installed	Installed
W6	Connects either +Va or +5 V to positive power pin of op-amps U1 and U3	Installed	Not installed
W7	Connects either -Va or GND to negative power pin of op-amps U1 and U3	Installed	Not installed

1.4 Analog Interface

The EVM board is designed for easy interfacing to analog sources such as signal generators and sensors. The buffer amplifier U1 is in a follower configuration, non-inverting gain of one. Output of this buffer drives the AIN(+) pin of the DUT through a $33-\Omega$ resistor (R4). If desired, the user can bypass U1 by connecting pins 1-2 of jumper W2. For low level common mode rejection (< 0.2V P-P) dual input pseudo-differential devices TLC4545, TLC3545, TLC2555 or TLV2545 can be used, byassing U1.

Table 1-6. Analog Input Connector J1

Pin	Signal	Description
J1.2	AIN0	Analog input signal to the non-inverting input of U1
J1.4	-AIN0	Second input to dual and pseudo differential devices
J1.6		N/C
J1.8		N/C
J1.10		N/C
J1.12		N/C
J1.14		N/C
J1.16		N/C
J1.18	REF+	External refence voltage for the DUT
J1.20		N/C

1.5 Digital Interface

The EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual-row header and socket combination at P2. This header/socket provides access to the digital control and serial data pins for all 10 of the 12-, 14-, and 16-bit ADCs. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1-7. Digital Connector J2

Pin Number	Signal	Description
J2.1	CS	Chip select – Active low signal, enables data transfer and device configuration
J2.3	CLKXa	Serial clock—damped with 33- Ω resistor
J2.5	CLKRa	Serial Clock
J2.7	FSXa	Frame sync—damped with $33-\Omega$ resistor
J2.9	FSRa	Frame sync (see Note)
J2.11	Reserved	
J2.13	DXRa	Serial data out
J2.15	Reserved	
J2.17	Reserved	
J2.19	Reserved	

Note: When using a single input ADC, TLC4541, TLC3541, TLC2551 or TLV2541, Frame Sync must be held at V_{DD}.

1.6 Power Supplies

The EVM requires three power supplies.

- 1) A dual-tracking ± 12 -V supply for the dual-supply op amps U1 and U3. The voltage reference (REF02) is supplied by the +12-V supply. Jumpers W6 and W7 are default settings for this voltage condition.
- 2) A single +5-V supply is used for the ADC (DUT) and the digital interface. Op amps U1 and U3 can be used in a unipolar power supply mode (+5 V and ground) by shorting pins 2-3 of jumper W6 and W7.

1.7 Voltage References

The EVM can be configured to use its onboard reference (REF02) by connecting pins1-2 of jumper W3. For an external reference source, configure W3 by connecting pins 2-3 and a DC supply reference voltage to pin 18 of J1.

1.8 EVM Operation

DC voltages can be applied to the EVM board either through the 10-pin standard power connector (J3) or the test points labeled –12 V, +12 V, +5, and GND. Apply the appropriate current limited (500 mA max) DC sources to the board prior to connecting the analog input and digital control signals. The digital control signals are applied directly to P2, or the EVM can be connected to a DSP interface board. The interface board is equipped with a power connector to mate with the 10-pin power connector (J3) on the EVM to supply the required voltages.

There are a number of interface options available for this style of EVM. Consult the product folder for a complete list of DSP interface cards and optional analog interface modules. If the interface options listed are not suitable, contact the PIC at (972) 644-5580, for the latest information.

Chapter 2

Layout

This chapter provides the board layouts.

Figure 2 - 1. Top Assembly Layer

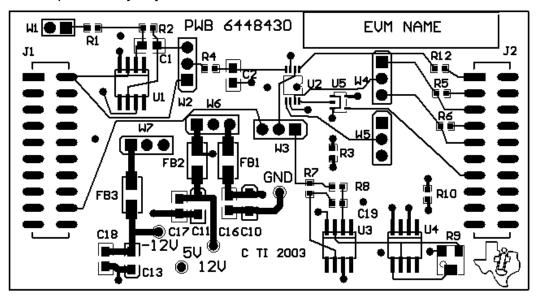


Figure 2-2. Ground Plane Layer

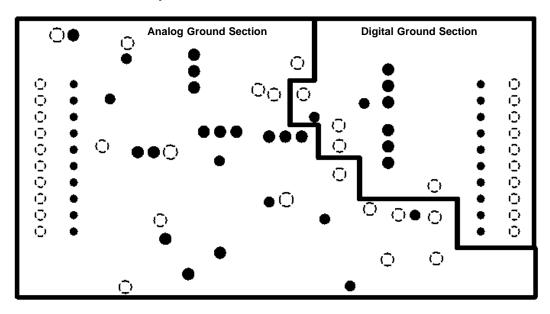


Figure 2-3. Voltage Plane Layer

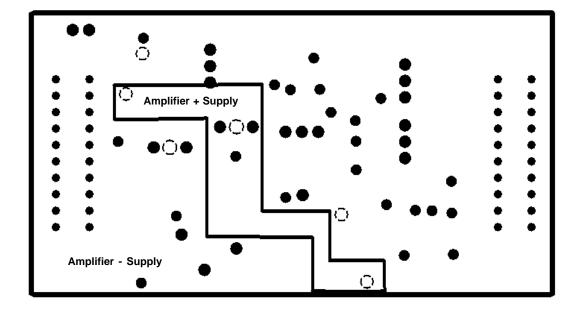
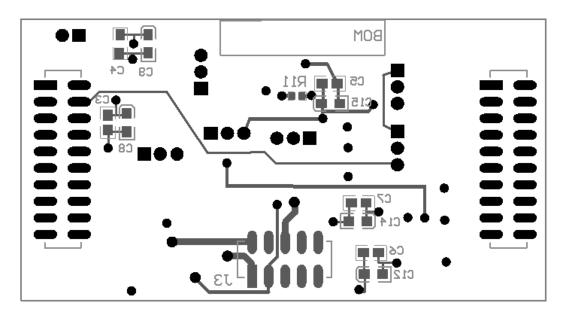


Figure 2 - 4. Bottom Assembly (Viewed From Top)



Chapter 3

EVM Bill of Materials and EVM Schematic

This chapter provides a bill of materials and schematic for the TLC4541/5EVM, TLC3541/5EVM, TLC2551/2/5EVM and TLV2541/2/5EVM.

Topic	Page
3.1	EVM Bill of Materials
3.2	EVM Schematic

3.1 EVM Bill of Materials

The following table contains a complete bill of materials for the TLC4541/5EVM, TLC3541/5EVM, TLC2551/2/5EVM and TLV2541/2/5EVM. Contact the Product Information Center (PIC) or e-mail dataconvapps@list.ti.com if you have questions regarding this EVM.

Table 3-1. EVM Bill of Materials

Ref Des	Description	Vendor	Part Number
C1 C2	NI		
C19	10 pF	Panasonic or equivalent	ECJ-1VC1H100D
C3 C4 C5 C6			
C7 C16 C17 C18	0.1 μF	Panasonic or equivalent	ECJ-2YB1H104K
C8 C9 C10 C11			
C12 C13 C14 C15	10uF	Panasonic or equivalent	ECS-T1CX106R
FB1 FB2 FB3	SM_FB_2773044447	Fair-Rite	2744044447
J1 J2	Header 10 × 2	Samtec	TSM-110-01-T-DV-P
J3	Header 5 × 2	Samtec	SSW-105-22-F-D-VS-K
P1 P2	Socket 10 × 2	Samtec	SSW-110-22-F-D-VS-K
PCB	Gerbers	Texas Instruments	6448430
R1 R3 R10	NI	Panasonic or equivalent	
R2 R11 R12	0R	Panasonic or equivalent	ERJ-3GEY0R00V
R4 R5 R6	33R	Panasonic or equivalent	ERJ-3GEYJ330V
R7 R8	100R	Panasonic or equivalent	ERJ-3GEYJ101V
R9	NI	Bourns	3214W-103E
SH1 - SH7	Shunts	Samtec or equivalent	SNT-100-BK-T-H
U1 U3	Precision op amp	Texas Instruments	OPA132AU
U2	TLC4541		TLC4541IDGK
U4	REF02	Texas Instruments	REF02AU
U5	SN74AHC1G125DBV	Texas Instruments	SN74AHC1G125DBV
W1	2POS_JUMPER	Samtec	TSW-102-07-L-S
W2 W3 W4	3POS_JUMPER	Samtec	TSW-103-07-L-S
W5 W6 W7			
GND	Black test point loop	Keystone	5001
12V 5V 12V	Red test point loop	Keystone	5000

3.2 EVM Schematic

The schematic diagram for the TLC4541/5EVM, TLC3541/5EVM, TLC2551/2/5EVM and TLV2541/2/5EVM is furnished as an attachement to this chapter.

