B10G4750N12DL

LDMOS 3-stage integrated Doherty MMIC

AMPLEON

Rev. 1 — 10 January 2023 Product data sheet

1. Product profile

1.1 General description

The B10G4750N12DL is a 3-stage 12 W fully integrated Doherty MMIC solution using Ampleon's state of the art LDMOS technology. The carrier and peaking device, input splitter, output combiner, and output matching are integrated in a single package. This multiband device is perfectly suited as a general purpose device in the frequency range from 4700 MHz to 5000 MHz. Available in LGA outline.

Table 1. Performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 31 mA (driver and final stages); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.50$ V; measured in an Ampleon application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA [1]	4900	28	1.585	31.1	32.6	−30.2

[1] Test signal: 1-carrier W-CDMA; PAR = 9.9 dB.

1.2 Features and benefits

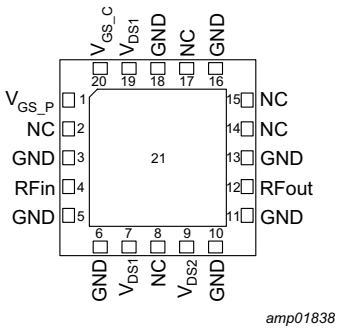
- Integrated input splitter
- Integrated output combiner
- Very high efficiency
- Designed for broadband operation (frequency 4700 MHz to 5000 MHz)
- Independent control of carrier and peaking bias
- Integrated ESD protection
- Excellent thermal stability
- High power gain, input and output matched to impedance 50 Ω
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard GSM, W-CDMA, LTE and NR small cell base stations in the 4700 MHz to 5000 MHz frequency range

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.
RFout is DC grounded.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{GS_P}	1	gate-source voltage of peaking
NC	2	not connected (connection to ground is allowed)
GND	3	ground (connection to ground is required)
RFin	4	RF input
GND	5	ground (connection to ground is required)
GND	6	ground (connection to ground is required)
V_{DS1}	7	drain-source voltage of driver stages
NC	8	not connected (connection to ground is allowed)
V_{DS2}	9	drain-source voltage of final stages
GND	10	ground (connection to ground is required)
GND	11	ground (connection to ground is required)
RFout	12	RF output
GND	13	ground (connection to ground is required)
NC	14	not connected (connection to ground is allowed)
NC	15	not connected (connection to ground is allowed)
GND	16	ground (connection to ground is required)
NC	17	not connected (connection to ground is allowed)
GND	18	ground (connection to ground is required)

Table 2. Pin description *…continued*

Symbol	Pin	Description
V_{DS1}	19	drain-source voltage of driver stages
V_{GS_C}	20	gate-source voltage of carrier
GND	21	RF ground (connection to ground is required)

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
LGA-7x7-20-2	B10G4750N12DLX	9349 605 89525	TR13; 3000-fold; 16 mm; dry pack	3000
	B10G4750N12DLZ	9349 605 89515	TR13; 1000-fold; 16 mm; dry pack	1000

4. Block diagram

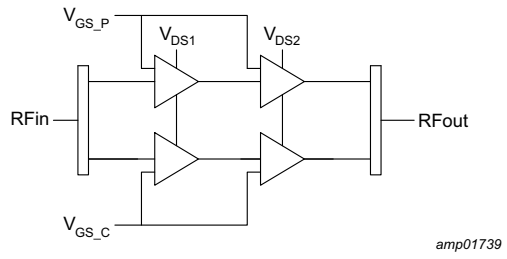


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–55	+125	°C
T_j	junction temperature	[1]	-	175	°C
T_{case}	case temperature	[1]	-	125	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; $P_{L(AV)}$ = 1.585 W [1]	7.8	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 9.9 dB.

7. Characteristics

Table 6. DC characteristics
T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 30 mA	1.65	2.13	2.75	V
I_{GSS}	gate leakage current	V_{GS} = +9 V/–5 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = +9 V/–5 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 60 V	-	-	1.4	µA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 60 V	-	-	1.4	µA

Table 7. RF characteristics
Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 30 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; P_L = 1.585 W; f = 5 GHz. Unless otherwise specified, measured in an Ampleon production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: CW pulsed						
G_p	power gain		27	30	-	dB
η_D	drain efficiency		26	32	-	%
RL_{in}	input return loss		-	–13	–8	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		39.5	41	-	dBm

8. Application information

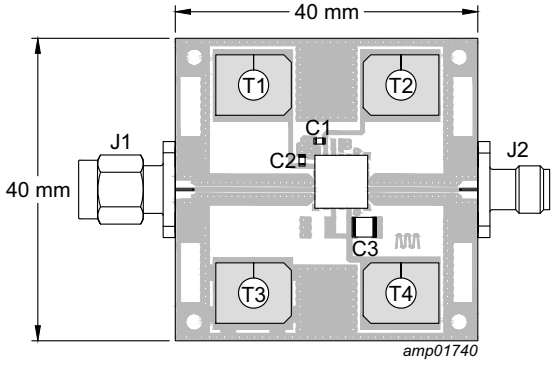
Table 8. Typical performance

T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 31 mA (driver and final stages); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.50$ V; Test signal: 1-carrier W-CDMA; PAR = 9.9 dB; unless otherwise specified, measured in an Ampleon 4700 MHz to 5000 MHz frequency band application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 4900 MHz [1]	-	42.1	-	dBm
η_D	drain efficiency	10.1 dB OBO ($P_{L(AV)}$ = 32 dBm); f = 4900 MHz	-	32.6	-	%
G_p	power gain	$P_{L(AV)}$ = 32 dBm; f = 4900 MHz	-	31.1	-	dB
G_{flat}	gain flatness	$P_{L(AV)}$ = 32 dBm; f = 4700 MHz to 5000 MHz	-	0.9	-	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 32 dBm; f = 4900 MHz	-	−30.2	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	f = 4850 MHz	-	0.08	-	dB/°C
K	Rollett stability factor	T_{case} = −40 °C; f = 0.6 GHz to 8.1 GHz [2]	-	>1	-	

[1] Pulsed CW power sweep measurement (δ = 10 %, t_p = 100 µs).

[2] S-parameters measured in a demo circuit.



Printed-Circuit Board (PCB): Rogers 4350B; ε_r = 3.66; thickness = 0.254 mm; thickness of copper plating = 35 µm.

Fig 3. Component layout

Table 9. Demo test circuit list of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1 µF, 25 V [1]	
C3	multilayer ceramic chip capacitor	10 µF, 50 V [1]	
J1	coaxial panel connector male		Huber+Suhner: 13_SMA-50-0-2-/111_N
J2	coaxial panel connector female		Huber+Suhner: 23_SMA-50-0-2-/111_N
T1, T2, T3, T4	PCB terminal	6.3 mm x 0.81 mm, 4.1 mm	TE connectivity

[1] Murata or capacitor of same quality.

8.1 Ruggedness in a Doherty operation

8.1.1 Output mismatch ruggedness

The B10G4750N12DL is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 32 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; P_i corresponding to $P_{L(3dB)} - 5$ dB under Z_S = 50 Ω load; f = 5000 MHz (1-carrier W-CDMA); T_{case} = 25 °C.

8.1.2 Wideband noise ruggedness

The B10G4750N12DL is capable of withstanding an AWGN (Additive White Gaussian Noise) with 11.2 dB PAR, OBW (Occupied BandWidth) of 900 MHz, under the following conditions: V_{DS} = 32 V; I_{Dq} = 32 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; 3 dB P_i overdrive from P_L = 34 dBm (corresponding to $P_{L(3dB)} - 9$ dB); f = 4850 MHz; T_{case} = 25 °C.

9. Package outline

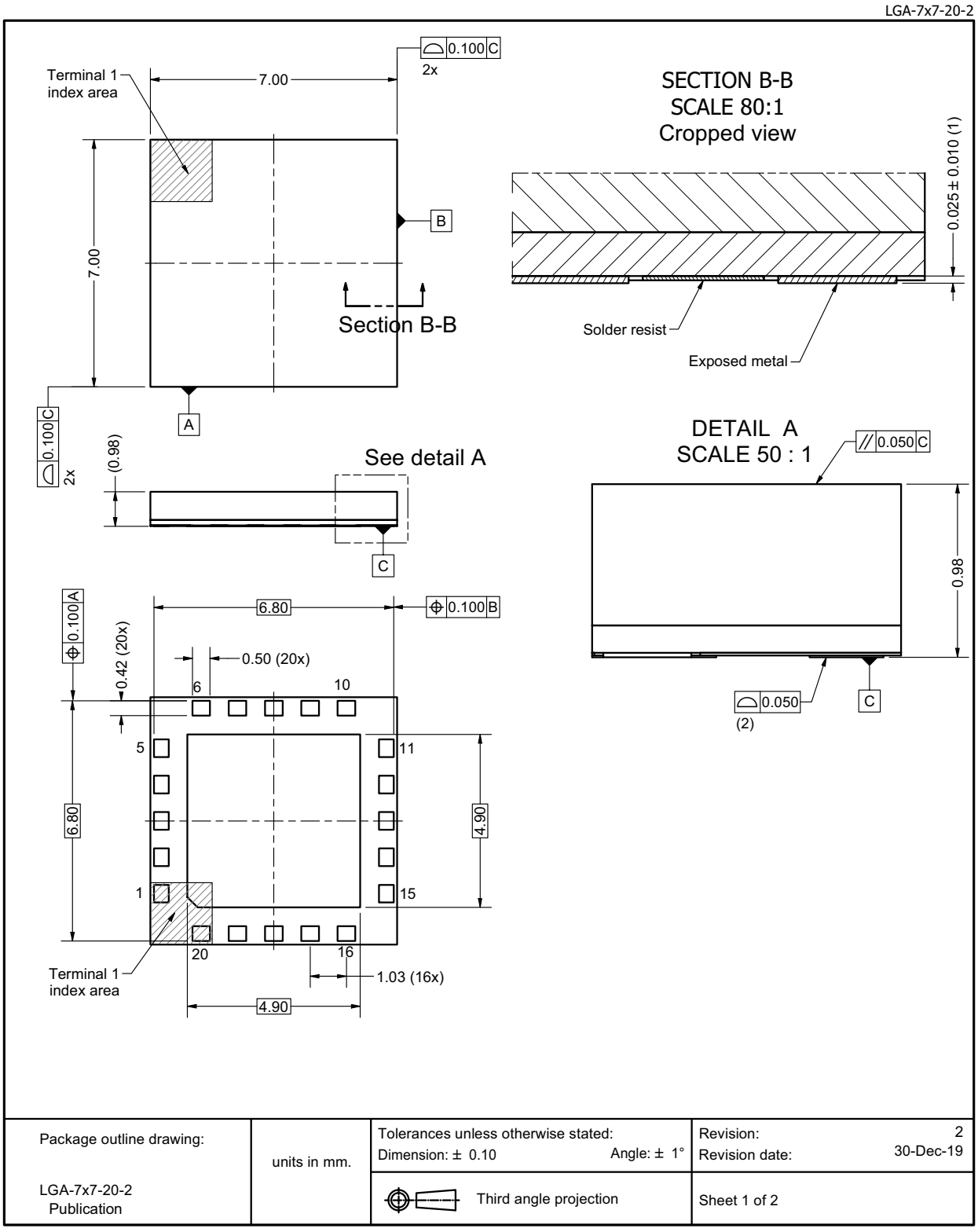


Fig 4. Package outline LGA-7x7-20-2 (sheet 1 of 2)

LGA-7x7-20-2

Drawing Notes	
Item	Description
1	Metal thickness of solder pads.
2	Flatness with respect to exposed metal

Package outline drawing: LGA-7x7-20-2	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.10 Angle: ± 1° Third angle projection	Revision: 2 Revision date: 30-Dec-19 Sheet 2 of 2

Fig 5. Package outline LGA-7x7-20-2 (sheet 2 of 2)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
NR	New Radio
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
B10G4750N12DL v.1	20230110	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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15. Contents

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