LCD Segment Driver series

For 128～140 Segment type LCD
LCD Segment Driver
BU9728AKV, BU9795AKV/FV/GUW

● Outline

This is LCD segment driver for 126 to 140 segment type display. There is a lineup which is suitable for multi function display and is integrated display RAM and power supply circuit for LCD driving with 4 common output type: BU9728AKV and BU9795AKV/FV/GUW.

BU9728AKV 128Segment (SEG32×COM4) Driver

● Feature (BU9728AKV)

1) 4wire serial interface (SCK, SD, $\overline{C/D}$, $\overline{CS}$)
2) Integrated RAM for display data (DDRAM) : 32 × 4bit (Max 128 Segment)
3) LCD driving port: 4 Common output, 32 Segment output
4) Display duty: 1/4 duty
5) Integrated Oscillator circuit (external resister type)
6) Integrated Power supply circuit for LCD driving (1/3 bias)
7) Low voltage / low power consumption design: +2.5～5.5V

● Uses (BU9728AKV)

DVC, Car audio, Telephone

● Absolute Maximum Ratings (Ta=25degree, VSS=0V) (BU9728AKV)

Parameter	Symbol	Limits	Unit	Remarks
Power Supply Voltage1	VDD	-0.3 ～ +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.3 ～ +7.0	V	LCD drive voltage
Allowable loss	Pd	400	mW	When use more than Ta=25°C, subtract 4mW per degree.
Operational temperature range	Topr	-40 ～ +85	degree	
Storage temperature range	Tstg	-55 ～ +125	degree	
Input voltage range	VIN	-0.3 to VDD+0.3	V	
Output voltage range	VOUT	-0.3 to VDD+0.3	V	

*This product is not designed against radioactive ray.

● Recommend operating conditions (Ta=25degree, VSS=0V) (BU9728AKV)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage1	VDD	2.5	-	5.5	V	
Power Supply Voltage2	VLCD	0	-	VDD	V	VDD≧V1≧V2≧V3≧VSS
Oscillator frequency	fOSC	-	36	-	KHz	Rf=470kΩ

∗This document is not delivery specifications.

Jul. 2008

● Electrical Characteristics (BU9728AKV)

DC Characteristics (VDD=2.5～5.5V, VSS=0V, Ta=25degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition	Terminal
		Min.	Typ.	Max.			
“H” level input voltage	VIH1	0.8×VDD	-	VDD	V	VO=0.9×VDD or 0.1×VDD	SC1, SD, SCK, $\overline{C/D}$, $\overline{CS}$, $\overline{RESET}$
“L” level input voltage	VIL1	0	-	0.2×VDD	V	VO=0.1×VDD or 0.9×VDD	
LCD Driver on resistance	RON	-	-	30	kΩ	|ΔVON|=0.1V	SEG0～31, COM0～3
“L” level Input current1	IIL1	-	-	100	μA	VIN=0	$\overline{RESET}$
“L” level Input current2	IIL2	-	-	2	μA	VIN=0	OSC1, SD, SCK, $\overline{C/D}$, $\overline{CS}$
“H” level Input current	IIH	-2	-	-	μA	VIN=VDD	OSC1, SD, SCK, $\overline{C/D}$, $\overline{CS}$, $\overline{RESET}$
Input capacitance	CI	-	5	-	pF		SD, SCK, $\overline{C/D}$, $\overline{CS}$
Power consumption	IDD	-	0.05	1	μA	*2 Display OFF	VDD
		-	40	80	μA	*3 Display ON	
		-	100	250	μA	*4 MPU Access	

*1: LCD Driver on resistance is not included internal power supply impedance

*2: V3=0V, All input terminal are connected to VDD or VSS.

*3: V3=0V, Rf=470kΩ, except of OSC1 terminals are connected to VDD or VSS.

*4: V3=0V, Rf=470kΩ, fSCK=200kHz

AC Characteristics (VDD=2.5～5.5V, VSS=0V, Ta=25degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
SCK rise time	tTLH	-	-	100	ns	
SCK fall time	tTHL	-	-	100	ns	
SCK cycle time	tCYC	800	-	-	ns	
Wait time for command	tWAIT	800	-	-	ns	
SCK pulse width ”H”	tWH1	300	-	-	ns	
SCK pulse width ”L”	tWL1	300	-	-	ns	
SD setup time	tSU1	100	-	-	ns	
SD hold time	tH1	100	-	-	ns	
$\overline{CS}$ pulse width ”H”	tWH2	300	-	-	ns	
$\overline{CS}$ pulse width ”L”	tWL2	6400	-	-	ns	
$\overline{CS}$ setup time	tSU2	100	-	-	ns	
$\overline{CS}$ hold time	tH2	100	-	-	ns	
C/$\overline{D}$ setup time	tSU3	100	-	-	ns	
C/$\overline{D}$ hold time	tH3	100	-	-	ns	Based on SCK 8th clock rising
C/$\overline{D}$ – CS time *5	tCCH	100	-	-	ns	Based on $\overline{CS}$ rising
C/$\overline{D}$ – SCK time *5	tSCH	100	-	-	ns	Based o SCK 8th clock falling

*5: Should satisfy either one condition

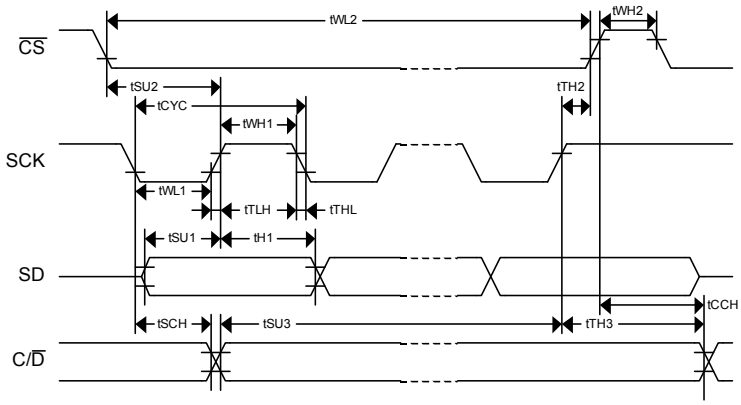


Fig. BU9728AKV-1 Interface timing

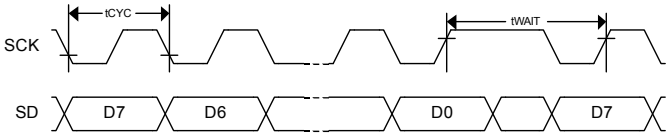


Fig. BU9728AKV-2 Command cycle

● Reference data (BU9728AKV)

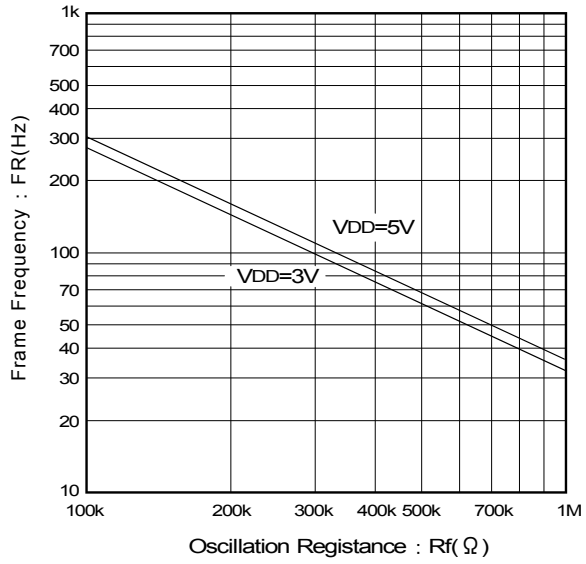


Fig. BU9728AKV-3 Frame frequency vs. Resister value

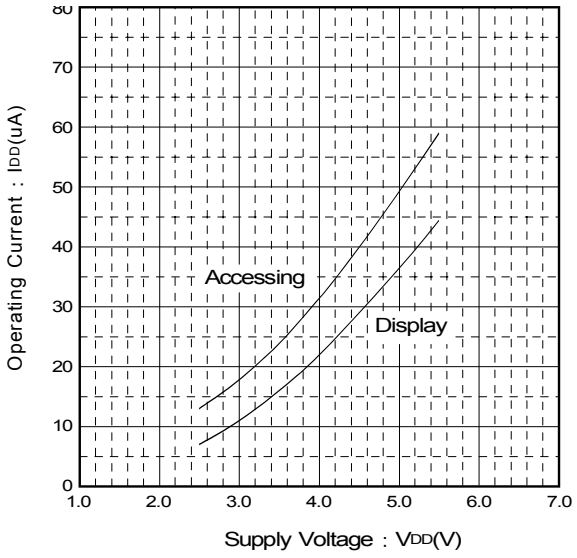


Fig. BU9728AKV-4 Power consumption vs. Power supply

● Block Diagram (BU9728AKV)

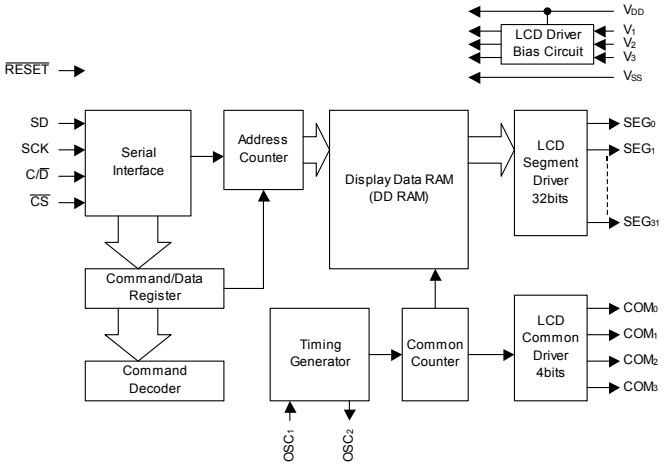


Fig. BU9728AKV-5 Block diagram

●Pin Arrangement (BU9728AKV)

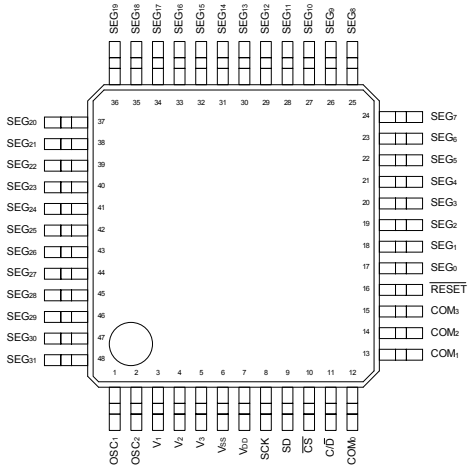


Fig. BU9728AKV-6 Pin arrangement

● Terminal description (BU9728AKV)

Terminal	No.	Type	Function
OSC1 OSC2	1 2	I O	Int clock use mode, connect resister between OSC1 and OSC2. Ext clock use mode, input clock from OSC1, OSC2 keep OPEN.
V1～V3	3～5		Power supply for LCD driving. Keep VDD≧V1≧V2≧V3≧VSS condition.
VSS	6		VSS terminal
VDD	7		VDD terminal
SCK	8	I	Serial clock input
SD	9	I	Serial data input
$\overline{CS}$	10	I	Chip select input “L”: active
$\overline{C/D}$	11	I	Command data judgment input “L”: display data, “H”: command
COM0～3	12～15	O	LCD COMMON output
$\overline{RESET}$	16	I	Reset input terminal. It will be initialized with "L" level input. Reset address counter, Set display off status.
SEG0～31	17～48	O	LCD SEGMENT output

● Block Description (BU9728AKV)

○ ADDRESS COUNTER

An address counter shows the address of DDRAM. Address data are transferred to the address counter automatically when an address set is written in the command/data register.

After data are written in DDRAM, +1 or +2 is done automatically with an address counter. The choice of +1 or +2 is done automatically by the next condition.

DDRAM 8bit writing (in the 8 clock of SCK, C/$\overline{D}$= "L") → +2

DDRAM 4bit rewriting (in the 8 clock of SCK, C/$\overline{D}$= "H") → +1

And, when it is counted to 1FH, an address becomes 00H with an address counter by the next count up.

○ DISPLAY DATA RAM (DDRAM)

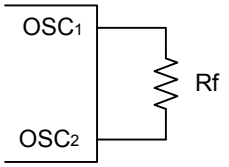
A display data RAM (DDRAM) is used to store display data. That capacity is 32 address × 4 bits. DDRAM and the relations of the display position are as the following.

DDRAM address

BIT	00	01	02	03	04	05	06	07	·····	1D	1E	1F	
D0													COM0
D1													COM1
D2													COM2
D3													COM3

○ TIMING GENERATER

It will be started to oscillate by connecting Rf between OSC1, OSC2, and generated display timing signal. Also it will be able to do by external clock input.



(It is possible that Oscillating Frequency is changed with Rf.)

Fig. BU9728AKV-7 Rf Oscillator Circuit

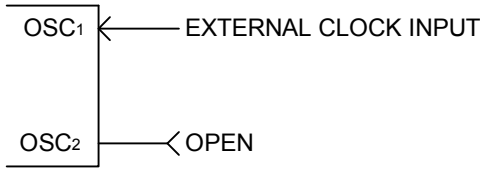


Fig. BU9728AKV-8 External Clock Input

○ LCD DRIVE POWER SUPPLY

LCD drive power supply occurs by BU9728AKV. LCD voltage is given by VDD- V3, and it causes V1=2･VLCD/3, V2=VLCD/3. When input LCD power supply by using external breeder register etc.

Please keep below condition.

$$VDD \geqq V1 \geqq V2 \geqq V3 \geqq VSS$$

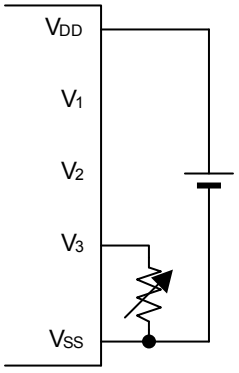


Fig. BU9728AKV-9 Internal Power supply use

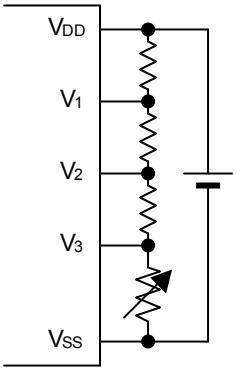


Fig. BU9728AKV-10 External Power supply use

● DETAIL OF COMMANDS (BU9728AKV)

There is the following thing in the command (The 8×n clock of SCK is C/D= "H".) of BU9728AKV.

○ ADDRESS SET

MSB LSB

0	0	0	A	A	A	A	A

Address data shown as AAAAA by the binary system is set on the address counter.
Address does +2 every time indication data input (for 8bit) completes input.

○ DISPLAY ON

MSB LSB

0	0	1	*	*	*	*	*

*:Don't Care

There are no relations with the contents of the display data RAM (DDRAM).
And all display is turned on. In this case, the contents of DDRAM don't change.

○ DISPLAY OFF

MSB LSB

0	1	0	*	*	*	*	*

*:Don't Care

There are no relations with the contents of the display data RAM (DDRAM).
In this case, the contents of DDRAM don't change.

○ DISPLAY START

MSB LSB

0	1	1	*	*	*	*	*

*:Don't Care

It will be started to oscillate and to display in accordance with the contents of DDRAM.

○ REWRITING OF THE DISPLAY DATA RAM (DDRAM)

MSB LSB

1	0	0	*	D	D	D	D

*:Don't Care

The binary four bits data DDDD are written in DDRAM.
A writing address is address ordered by the address set command.
Then, after this command is carried out, an address does + 1 automatically.

○ RESET

MSB LSB

1	1	0	*	*	*	*	*

*:Don't Care

Please execute this command first after Power on. It will be initialized as follow conditions;

- Display OFF
- Address counter reset

● Recommendation circuit example (BU9728AKV)

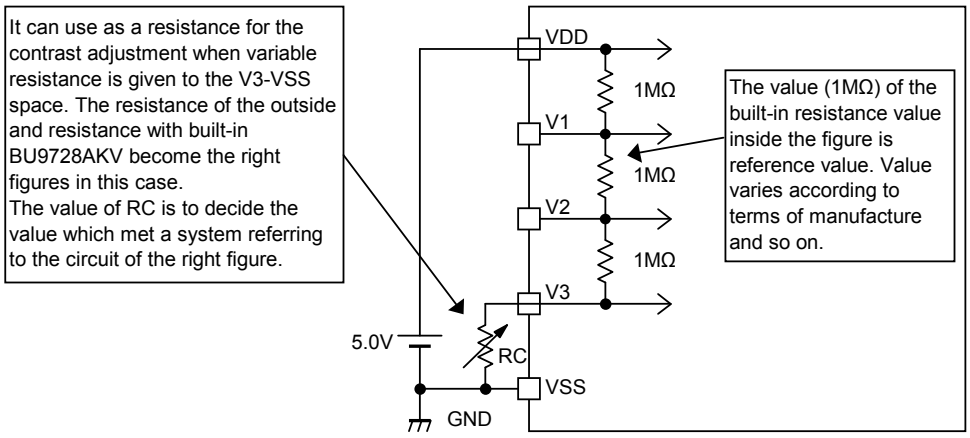
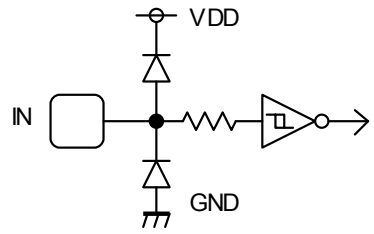
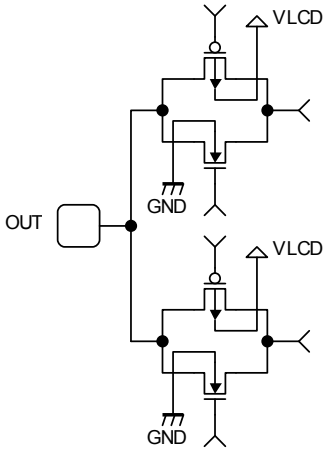
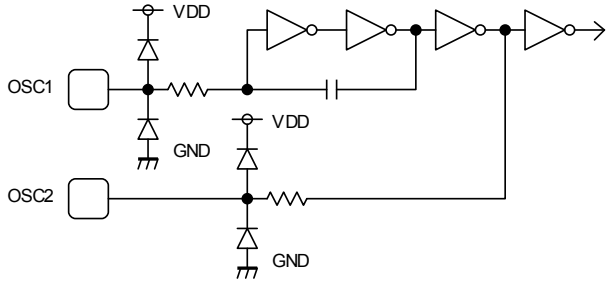


Fig. BU9728AKV-11 When a contrast adjustment mechanism is used.

● INPUT OUTPUT CIRCUIT (BU9728AKV)

Name	I/O	Circuit	Name	I/O	Circuit
SD SCK $\overline{C/D}$ $\overline{CS}$	I		SEG0 ～ SEG31 COM0 ～ COM3	O	

Name	I/O	Circuit
OSC1 OSC2		

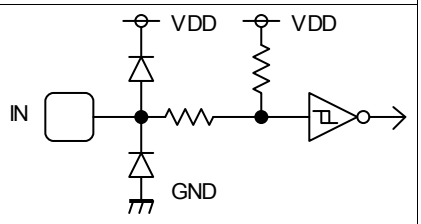
Name	I/O	Circuit
$\overline{RESET}$	I	

Fig. BU9728AKV-14 INPUT OUTPUT circuit

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

● Order form name selection

B	U	9	7	2	8	A	K	V	–	E	2

ROHM form name

Part No.

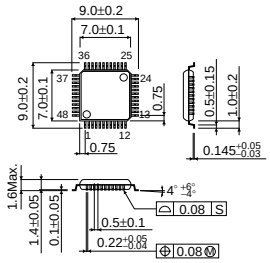
Package type
KV=VQFP

Packaging and forming specification

E2 =Reel-shaped emboss taping

VQFP48C

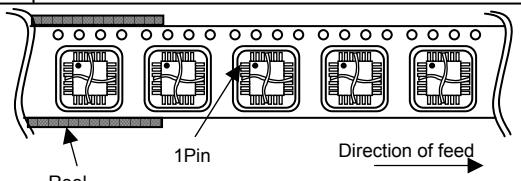
<Dimension>



(Unit:mm)

< Packing information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*When you order , please order in times the amount of package quantity.

BU9795AKV/FV/GUW MAX140Segment (SEG35×COM4) Driver

● Feature (BU9795AKV/AFV/AGUW)

1) 3wire serial interface (CSB, SD, SCL)
2) Integrated RAM for display data (DDRAM) : 35 × 4bit (Max 140 Segment)
3) LCD driving port: 4 Common output,
   Segment: 35output (BU9795AKV), 31output (BU9795AGUW), 27output (BU9795AFV)
4) Display duty: 1/4 duty
5) Integrated Buffer AMP for LCD driving power supply
6) 1/2bias, 1/3bias selectable
7) No external components
8) Low power/ Ultra low power consumption design: +2.5～5.5V

● Uses (BU9795AKV/AFV/AGUW)

Telephone, FAX, Portable equipment (POS, ECR, PDA etc.),
DSC, DVC, Car audio, Home electrical appliance, Meter equipment etc.

● Line-up

Parameter	BU9795AKV	BU9795AFV	BU9795AGUW
Segment output	35	27	31
Common output	4	4	4
Package	VQFP48C	SSOP-B40	VBGA48W040

● Absolute Maximum Ratings (Ta=25degree, VSS=0V) (BU9795AKV/AFV/AGUW)

Parameter	Symbol	Limits	Unit	Remark
Power supply voltage1	VDD	-0.5 ～ +7.0	V	Power supply
Power supply voltage2	VLCD	-0.5 ～ VDD	V	LCD drive voltage
Allowable loss	Pd	0.6	W	When use more than Ta=25°C, subtract 6mW per degree.(BU9795AKV)
		0.7	W	When use more than Ta=25°C, subtract 7mW per degree (BU9795AFV)
		0.27	W	When use more than Ta=25°C, subtract 2.7mW per degree (BU9795AGUW)
Input voltage range	VIN	-0.5 ～ VDD+0.5	V	
Operational temperature range	Topr	-40 ～ +85	degree	
Storage temperature range	Tstg	-55 ～ +125	degree	

*This product is not designed against radioactive ray.

● Recommend operating conditions (Ta=25degree,VSS=0V) (BU9795AKV/AFV/AGUW)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply voltage2	VLCD	0	-	VDD-2.4	V	LCD drive voltage

* Please use VDD-VLCD≧2.4V condition.

● Electrical Characteristics(BU9795AKV/AFV/AGUW)

DC Characteristics (VDD=2.5～5.5V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter		Symbol	Limit			Unit	Condition
			MIN	TYP	MAX		
“H” level input voltage		VIH	0.7VDD	-	VDD	V	
“L” level input voltage		VIL	VSS	-	0.3VDD	V	
“H” level input current		IIH	-	-	1	uA	
“L” level input current		IIL	-1	-	-	uA	
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10uA
	COM	RON	-	3.5	-	kΩ	
VLCD supply voltage		VLCD	0	-	VDD -2.4	V	VDD-VLCD≧2.5V
Standby current		Ist	-	-	5	uA	Display off, Oscillator off
Power consumption 1		IDD1	-	12.5	30	uA	VDD=3.3[V], Ta=25, Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption 2		IDD2	-	20	40	uA	VDD=3.3[V], Ta=25, Normal mode, FR=80Hz 1/3 bias, Line inverse

● Oscillation Characteristics (BU9795AKV/AFV/AGUW)

(VDD=2.5～5.5V,VSS=0V, Ta=-40～85degree)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	f_{CLK}	56	80	104	Hz	FR = 80Hz setting
Frame frequency1	f_{CLK1}	70	80	90	Hz	VDD=3.5V, 25degree

● MPU interface Characteristics (BU9795AKV/AFV/AGUW)

(VDD=2.5V～5.5V,VSS=0V, Ta=-40～85degree)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
SCL cycle time	tSCY	400	-	-	ns	
“H” SCL pulse width	tSHW	100	-	-	ns	
“L” SCL pulse width	tSLW	100	-	-	ns	
SD setup time	tSDS	20	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
“H” CSB pulse width	tCHW	50	-	-	ns	

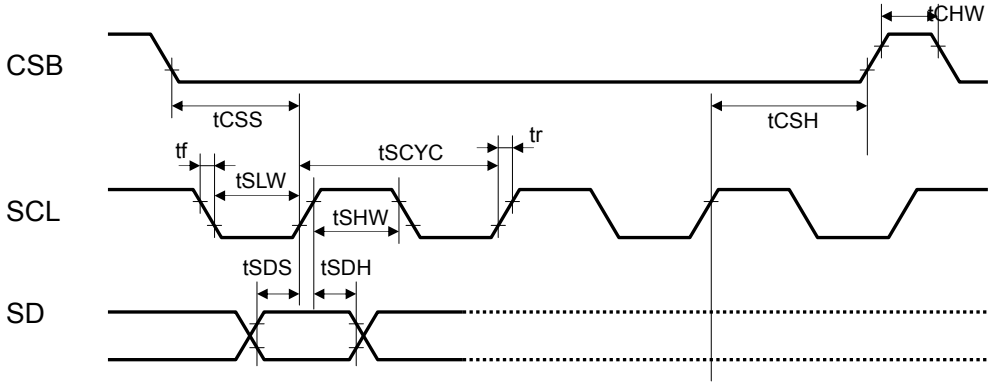


Fig.BU9795AKV/FV/GUW-1 3wire Serial timing waveform

* BU9795AKV

● Block Diagram

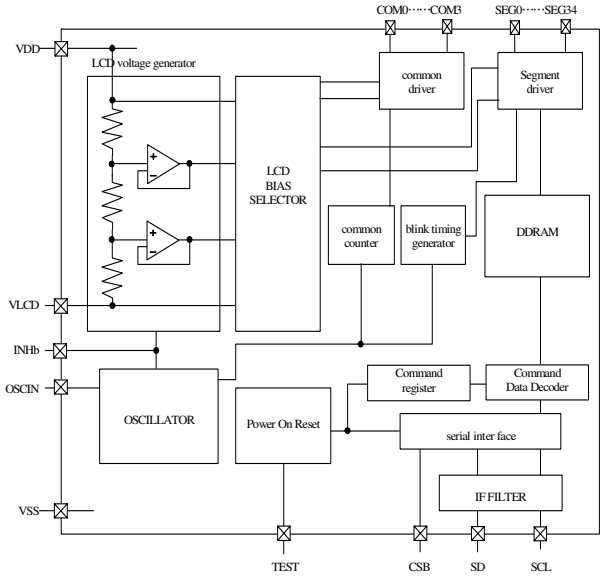


Fig. BU9795AKV /AFV /AGUW-2A
BU9795AKV Block diagram

● Pin Arrangement

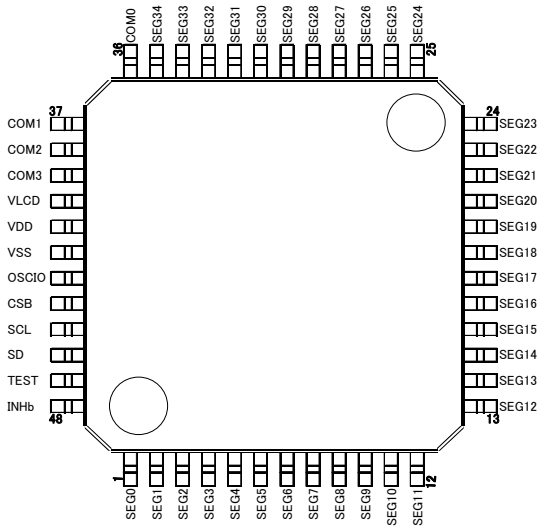


Fig. BU9795AKV /AFV /AGUW-3A
BU9795AKV Pin arrangement

● Terminal description

Terminal	Terminal No.	I/O	Function
INHb	48	I	Input terminal for turn off display H: turn on display L: turn off display
TEST	47	I	Test input (ROHM use only) Must be connect to VSS
OSCIO	43	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	46	I	serial data input
SCL	45	I	serial data transfer clock
CSB	44	I	Chip select : “L” active
VSS	42		GND
VDD	41		Power supply
VLCD	40		Power supply for LCD driving
SEG0-34	1-35	O	SEGMENT output for LCD driving
COM0-3	36-39	O	COMMON output for LCD driving

* BU9795AFV

● Block Diagram

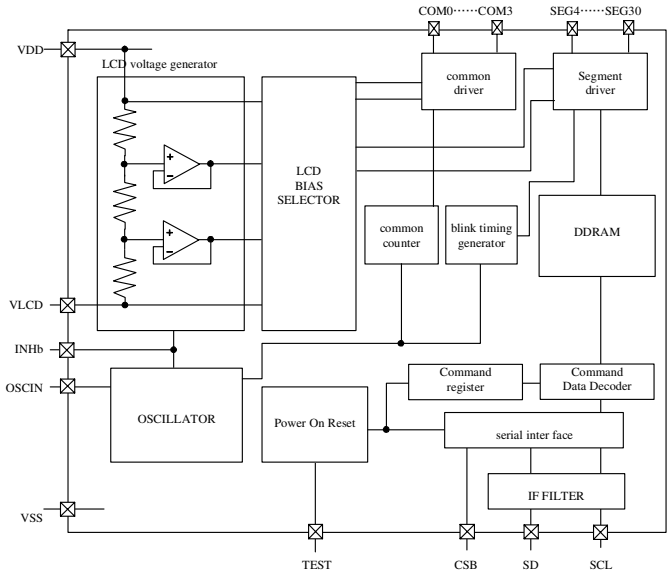


Fig. BU9795AKV /AFV /AGUW-2B
BU9795AFV Block diagram

● Pin Arrangement

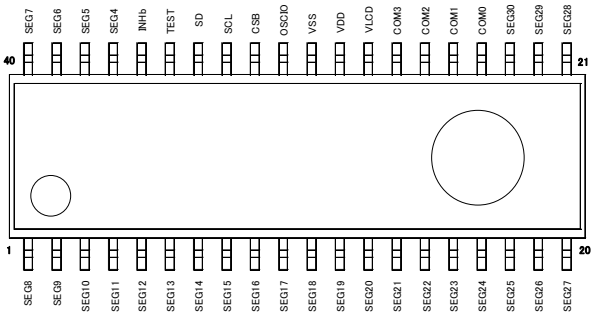


Fig. BU9795AKV /AFV /AGUW-3B
BU9795AFV Pin arrangement

● Terminal description

Terminal	Terminal No.	I/O	Function
INHb	36	I	Input terminal for turn off display H: turn on display L: turn off display
TEST	35	I	Test input (ROHM use only) Must be connect to VSS
OSCIO	31	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	34	I	serial data input
SCL	33	I	serial data transfer clock
CSB	32	I	Chip select : “L” active
VSS	30		GND
VDD	29		Power supply
VLCD	28	I	Power supply for LCD driving
SEG4-30	1-23, 37-40	O	SEGMENT output for LCD driving
COM0-3	24-27	O	COMMON output for LCD driving

* BU9795AGUW

● Block Diagram

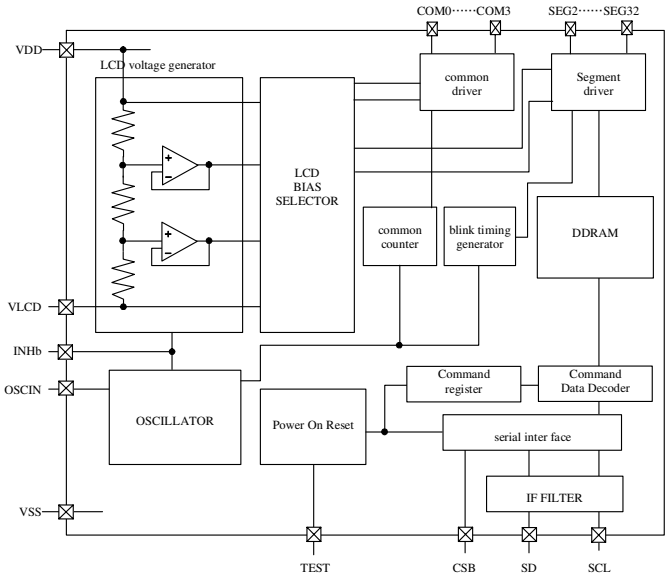


Fig. BU9795AKV /AFV /AGUW-2C
BU9795AGUW Block diagram

● Pin Arrangement

	1	2	3	4	5	6	7
G	(NC)	SEG13	SEG15	SEG18	SEG20	SEG22	(NC)
F	SEG11	SEG12	SEG16	SEG17	SEG21	SEG23	SEG24
E	SEG9	SEG10	SEG14	SEG19	SEG25	SEG27	SEG26
D	SEG7	SEG6	SEG8	SEG5	SEG30	SEG28	SEG29
C	SEG4	SEG3	SEG2	CSB	COM3	SEG32	SEG31
B		INHb	SD	VSS	VDD	COM1	COM0
A	(NC)	TEST2	SCL	OSCIO	VLCD	COM2	(NC)

Fig. BU9795AKV /AFV /AGUW-3C
BU9795AGUW Pin arrangement

● Terminal description

Terminal	I/O	Function
INHb	I	Input terminal for turn off display H: turn on display L: turn off display
TEST	I	Test input (ROHM use only) Must be connect to VSS
OSCIO	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	I	serial data input
SCL	I	serial data transfer clock
CSB	I	Chip select : “L” active
VSS		GND
VDD		Power supply
VLCD	I	Power supply for LCD driving
SEG2-32	O	SEGMENT output for LCD driving
COM0-3	O	COMMON output for LCD driving

(Caution) About terminal number, please refer to above pin arrangement

● Command Description (BU9795AKV/AFV/AGUW)

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

○ **Mode Set (MODE SET)**

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(*:Don't care)

Set display ON and OFF

Setting	P3	Reset initialize condition
Display OFF (DISPOFF)	0	○
Display ON (DISPON)	1	

Set bias level

Setting	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

○ **Address set (ADSET)**

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

Address data is specified in P[4:0] and P2 (ICSET command) as follows.

	MSB			LSB
Internal register	Address [5]	Address [4]	・・・	Address [0]
Bit of each command	ICSET [P2]	ADSET [P4]	・・・	ADSET [P0]

○ **Display control (DISCTL)**

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Frame frequency

Setting	P4	P3	Reset initialize condition
80Hz	0	0	○
71Hz	0	1	
64Hz	1	0	
53Hz	1	1	

Set LCD drive waveform

Setting	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Set Power save mode

Setting	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

∗ VDD-VLCD>=3.0V is required for High power mode.

○ Set IC Operation (ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2: MSB data of DDRAM address. Please refer to “ADSET” command.

Setting	P2	Reset initialize condition
Address MSB‘0’	0	○
Address MSB‘1’	1	

Set Software Reset condition

Setting	P1
No operation	0
Software Reset	1

Switch between internal clock and external clock.

Setting	P0	Reset initialize condition
Internal clock	0	○
External clock input	1	

○ Blink control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

Set blink condition

Setting	P1	P0	Reset initialize condition
OFF	0	0	○
0.5 Hz	0	1	
1 Hz	1	0	
2 Hz	1	1	

○ All pixel control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON. OFF

Setting	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

Setting	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

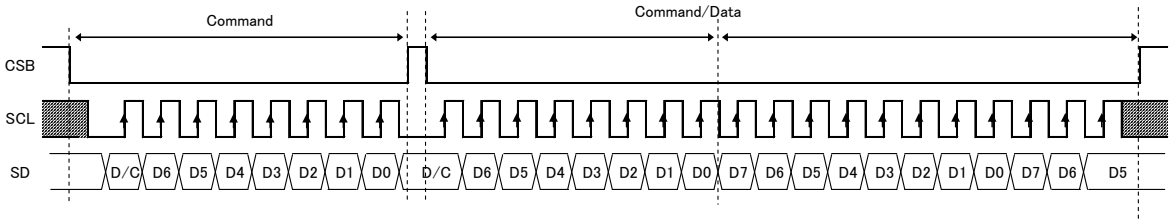
.

● Function description (BU9795AKV/AFV/AGUW)

○ Command and data transfer method

○ 3-SPI (3wire Serial interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB="H",
and CSB="L" makes SD and SCL input enable.
The protocol of 3-SPI transfer is as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data,
and continuously in order of D6 to D0 are followed after CSB ="L".
(Internal data is latched at the rising edge of SCL, it converted to 8bits parallel data
at the falling edge of 8th CLK.)



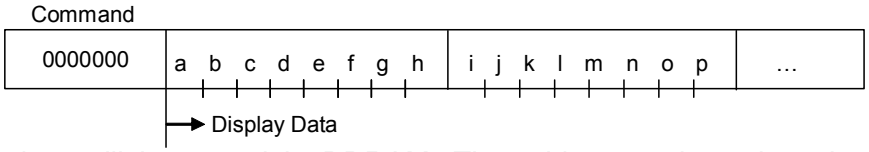
D/C = "H" : Command D/C = "L" : Data

Fig. BU9795AKV /AFV /AGUW-10 3-SPI Command/Data transfer format

○Write display data and transfer method

* BU9795AKV

This LSI have Display Data RAM (DDRAM) of 35×4=140bit.
The relationship between data input and display data, DDRAM data and address are as follows.



8 bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data.

Data can be continuously written in DDRAM by transmitting Data continuously.
(When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.

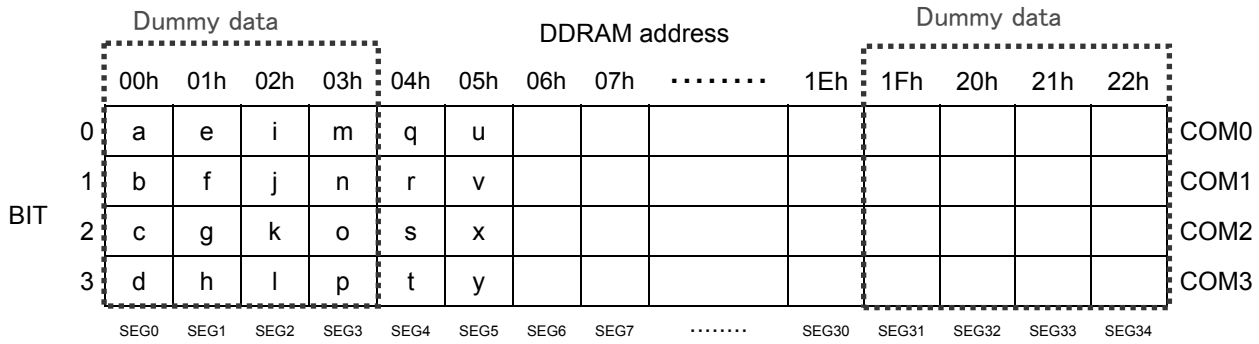
DDRAM address

BIT	00h	01h	02h	03h	04h	05h	06h	07h	·····	1Eh	1Fh	20h	21h	22h	
0	a	e	i	m	q	u									COM0
1	b	f	j	n	r	v									COM1
2	c	g	k	o	s	x									COM2
3	d	h	l	p	t	y									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	·····	SEG30	SEG31	SEG32	SEG33	SEG34	

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

* BU9795AFV

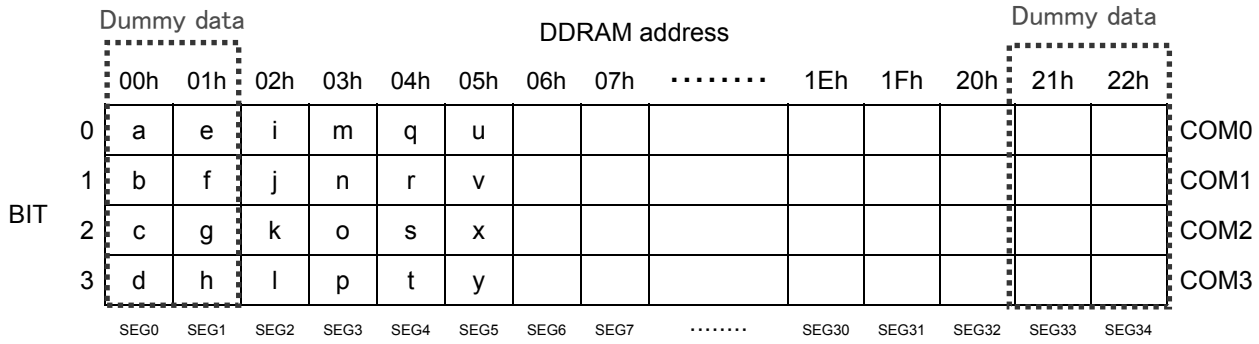
As SEG0, SEG1, SEG2, SEG3, SEG31, SEG32, SEG33, SEG34 are not output, these address will be dummy address.



As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB=”L”→”H” before 4bits data transfer.

* BU9795AGUW

As SEG0, SEG1, SEG33, SEG34 are not output, these address will be dummy address.



As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB=”L”→”H” before 4bits data transfer.

○ Reset (initial) condition

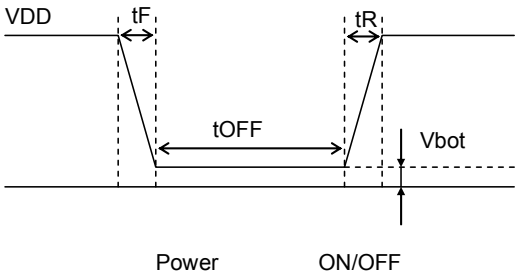
Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Refer to Command Description about initialize value of register.

● **Cautions of Power-On condition** (BU9795AKV /AFV /AGUW)

This LSI has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

1. Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation.



Recommendation condition of tR,tF,tOFF,Vbot

tR	tF	tOFF	Vbot
Less than 1ms	Less than 1ms	More than 150ms	Less than 0.1V

Fig. BU9795AKV /AFV /AGUW-18 Power on-off waveform

2. If it is difficult to meet above conditions, execute the following sequence after Power-On. Because it doesn’t accept the command in power off, it is necessary to care that correspondence by software reset doesn’t become alternative to POR function completely.

(1) CSB=”L”→”H” condition

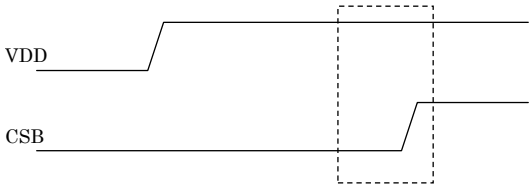


Fig. BU9795AKV-19 CSB Timing

(2) After CSB”H”→“L”, execute Software Reset (ICSET command).

● IO Circuit (BU9795AKV /AFV /AGUW)

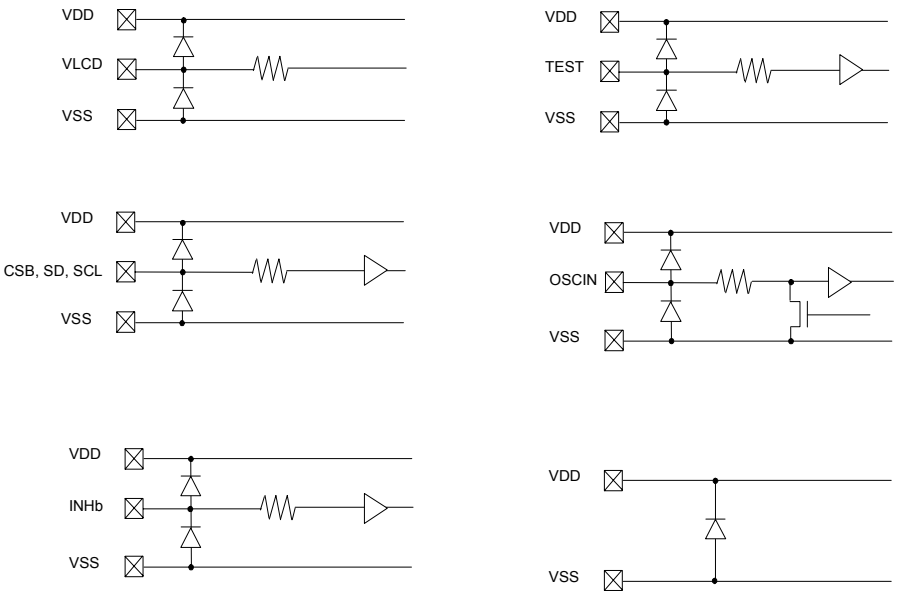


Fig. BU9795AKV /AFV /AGUW-20 IO circuit

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

● Order form name selection

B	U	9	7	9	5	A	K	V	–	E	2

ROHM form name

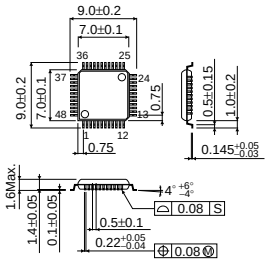
Part No.

Package type
KV=VQFP
FV= SSOP-B
GUW=VBGA

Packaging and forming specification
E2 =Reel-shaped emboss taping

VQFP48C

<Dimension>



(Unit:mm)

< Packing information >

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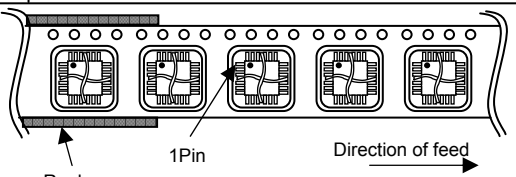
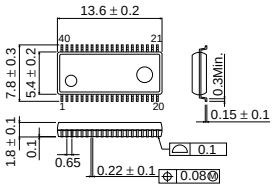
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*When you order , please order in times the amount of package quantity.

SSOP-B40

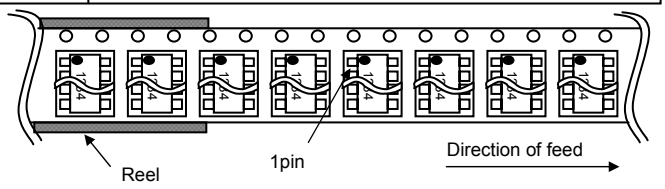
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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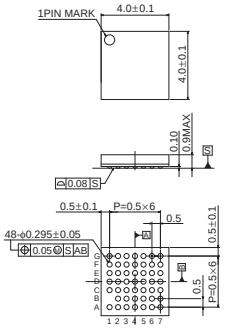
VBGA048W040

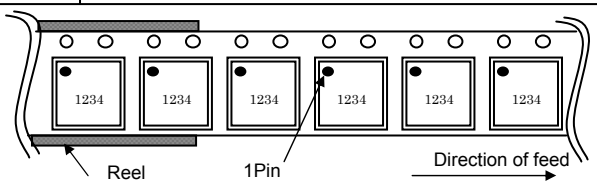
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.)



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