

SN74CBT16212C

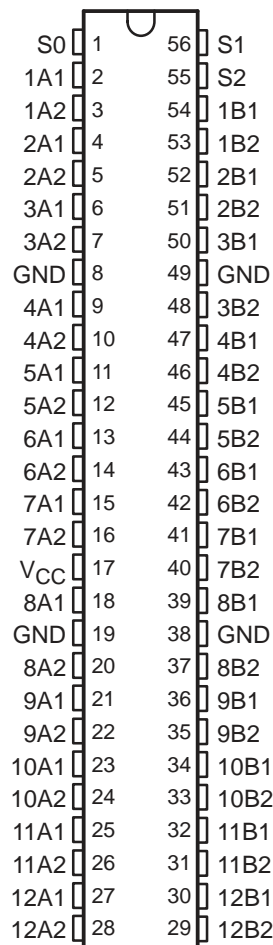
24-BIT FET BUS-EXCHANGE SWITCH

5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS146A – OCTOBER 2003 – REVISED JANUARY 2004

- Member of the Texas Instruments Widebus™ Family
- Undershoot Protection for Off-Isolation on A and B Ports Up To -2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 3 \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{iO(OFF)} = 8 \text{ pF}$ Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 5 \mu\text{A}$ Max)
- V_{CC} Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16212CDL	CBT16212C
		Tape and reel	SN74CBT16212CDLR	
	TSSOP – DGG	Tube	SN74CBT16212CDGG	CBT16212C
		Tape and reel	SN74CBT16212CDGGR	
	TVSOP – DGV	Tape and reel	SN74CBT16212CDGVR	CY212C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

SN74CBT16212C
24-BIT FET BUS-EXCHANGE SWITCH
5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS146A – OCTOBER 2003 – REVISED JANUARY 2004

description/ordering information (continued)

The SN74CBT16212C is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{ON}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16212C provides protection for undershoot up to -2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT16212C operates as a 24-bit bus switch, or as a 12-bit bus-exchange that provides data exchanging between four signal ports. The select (S0, S1, S2) inputs control the data path of the bus-exchange switch. When the bus-exchange switch is ON, the A port is connected to the B port, allowing bidirectional data flow between ports. When the bus-exchange switch is disabled, a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, each select input should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

FUNCTION TABLE
(each 12-bit bus-exchange)

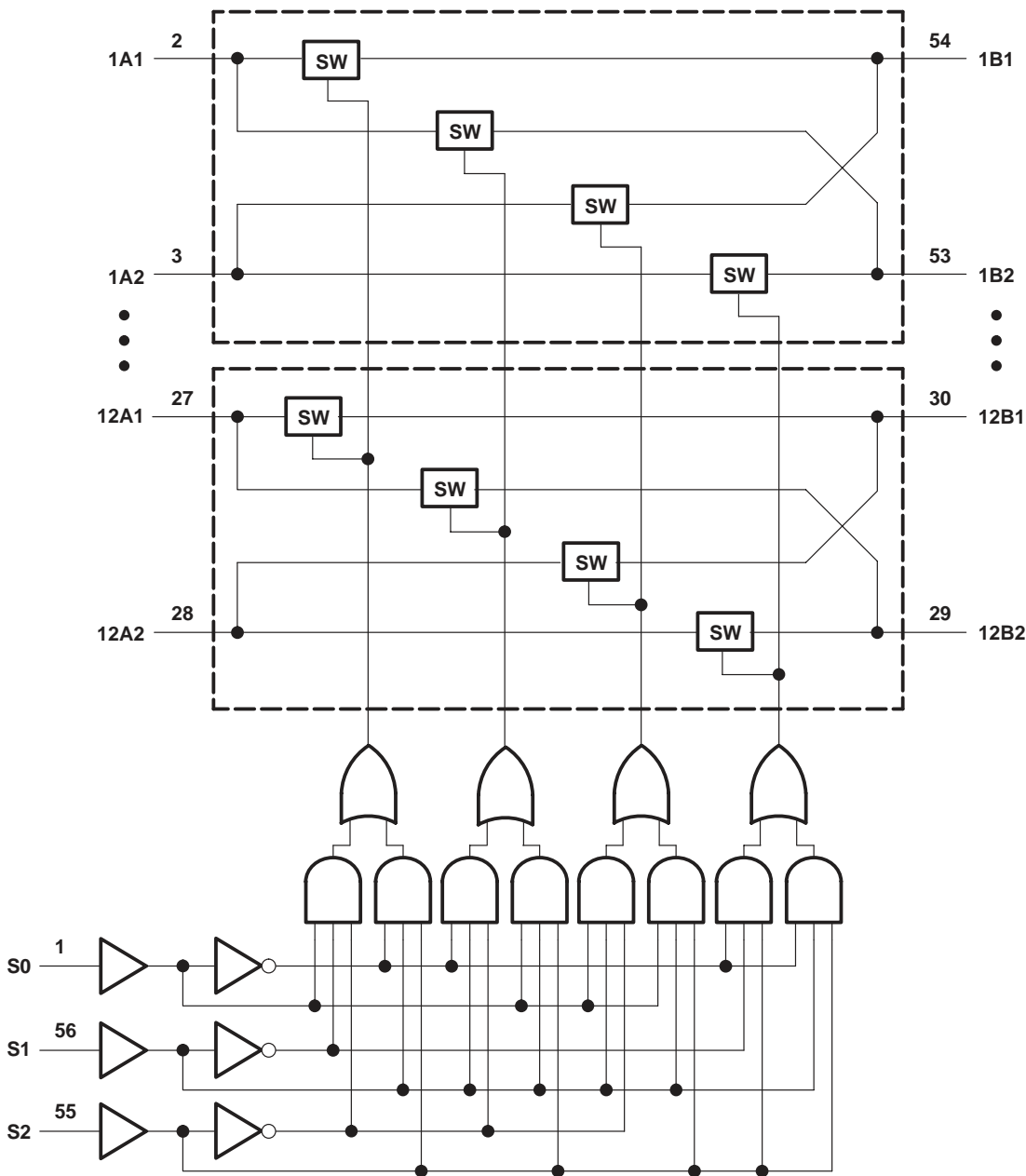
INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port A2 port = B1 port



SN74CBT16212C
24-BIT FET BUS-EXCHANGE SWITCH
5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS146A - OCTOBER 2003 - REVISED JANUARY 2004

logic diagram (positive logic)



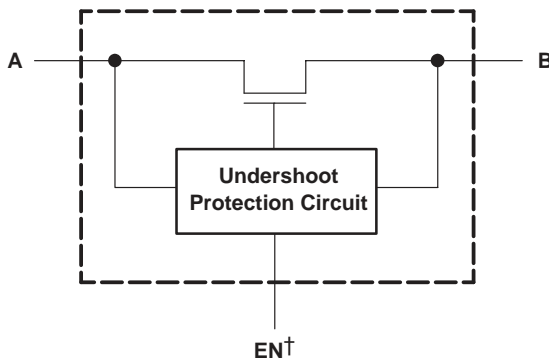
SN74CBT16212C

24-BIT FET BUS-EXCHANGE SWITCH

5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS146A – OCTOBER 2003 – REVISED JANUARY 2004

simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	-0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	-50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	± 128 mA
Continuous current through V_{CC} or GND terminals	± 100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGG package	64°C/W
	DGV package	48°C/W
	DL package	56°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4	5.5	V
V_{IH} High-level control input voltage	2	5.5	V
V_{IL} Low-level control input voltage	0	0.8	V
$V_{I/O}$ Data input/output voltage	0	5.5	V
T_A Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74CBT16212C
24-BIT FET BUS-EXCHANGE SWITCH
5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS146A – OCTOBER 2003 – REVISED JANUARY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT		
V_{IK}	Control inputs	$V_{CC} = 4.5\text{ V}$,	$I_{IN} = -18\text{ mA}$			-1.8	V		
V_{IKU}	Data inputs	$V_{CC} = 5\text{ V}$,	$0\text{ mA} > I_I \geq -50\text{ mA}$, $V_{IN} = V_{CC}$ or GND, Switch OFF			-2	V		
I_{IN}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_{IN} = V_{CC}$ or GND			± 1	μA		
I_{OZ}^\ddagger		$V_{CC} = 5.5\text{ V}$,	$V_O = 0$ to 5.5 V , $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND			± 10	μA		
I_{off}		$V_{CC} = 0$,	$V_O = 0$ to 5.5 V , $V_I = 0$			10	μA		
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_{I/O} = 0$, $V_{IN} = V_{CC}$ or GND, Switch ON or OFF			7.5	μA		
ΔI_{CC}^\S	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V , Other inputs at V_{CC} or GND			2.5	mA		
C_{in}	Control inputs	$V_{IN} = 3\text{ V}$ or 0				3.5	pF		
$C_{iO(OFF)}$		$V_{I/O} = 3\text{ V}$ or 0 ,	Switch OFF, $V_{IN} = V_{CC}$ or GND			8	pF		
$C_{iO(ON)}$		$V_{I/O} = 3\text{ V}$ or 0 ,	Switch ON, $V_{IN} = V_{CC}$ or GND			19	pF		
r_{on}^\parallel		$V_{CC} = 4\text{ V}$, TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$, $I_O = -15\text{ mA}$			8	12	Ω	
			$V_I = 0$	$I_O = 64\text{ mA}$			3		6
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_O = 30\text{ mA}$			3		6
			$V_I = 2.4\text{ V}$, $I_O = -15\text{ mA}$				5		10

V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\#$	A or B	B or A	0.24		0.15		ns
$t_{pd(s)}$	S	A	7		1.5	6.4	ns
t_{en}	S	B	7.2		1.5	7	ns
t_{dis}	S	B	7.7		1.5	7.5	ns

The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SN74CBT16212C

24-BIT FET BUS-EXCHANGE SWITCH

5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS146A – OCTOBER 2003 – REVISED JANUARY 2004

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	$V_{CC} = 5.5 \text{ V}$, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

† All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

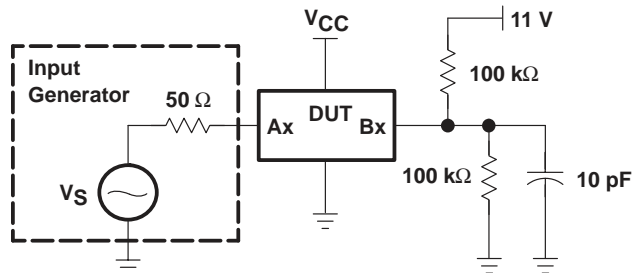


Figure 1. Device Test Setup

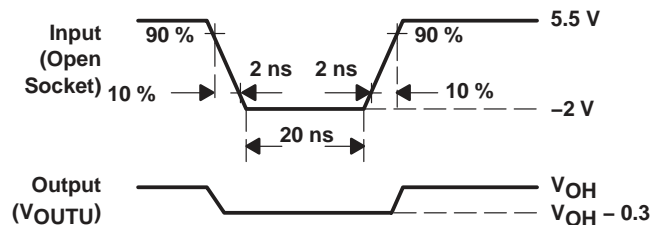
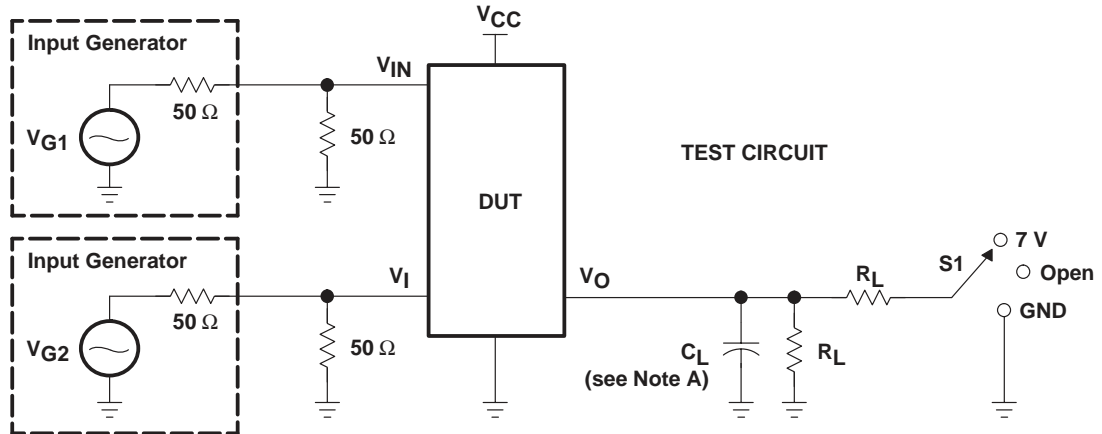
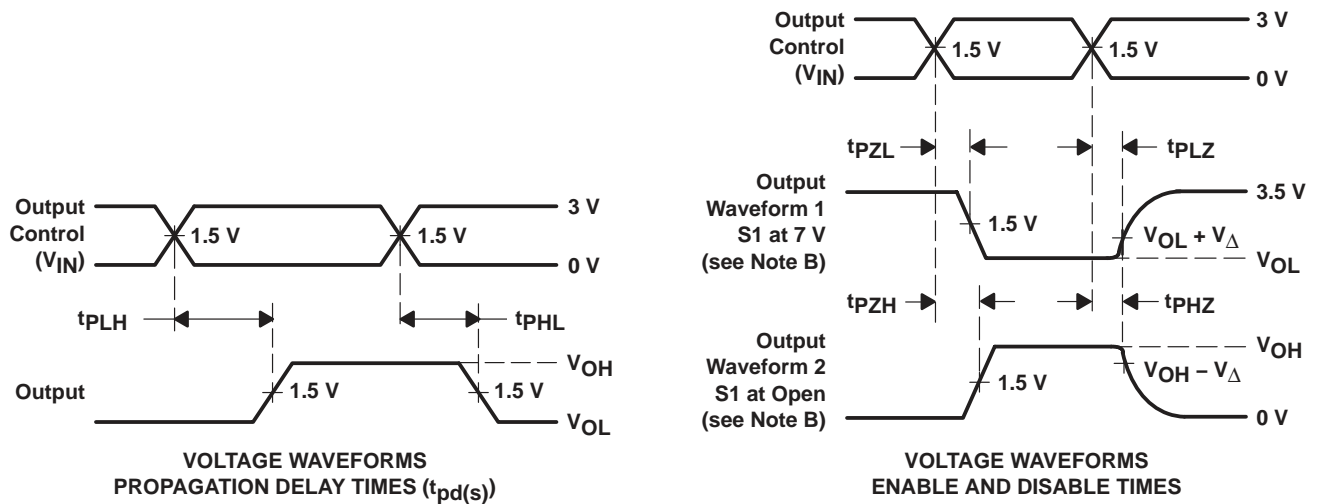


Figure 2. Transient Input Voltage (V_i) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd} (s)	5 V ± 0.5 V	Open	500 Ω	V _{CC} or GND	50 pF	
	4 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	5 V ± 0.5 V	Open	500 Ω	V _{CC}	50 pF	0.3 V
	4 V	Open	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PZH} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT16212CDGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212C	Samples
SN74CBT16212CDGVR	ACTIVE	TVSOP	DGV	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY212C	Samples
SN74CBT16212CDL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212C	Samples
SN74CBT16212CDLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16212C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16212CDGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CBT16212CDGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CBT16212CDLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16212CDGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CBT16212CDGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CBT16212CDLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE

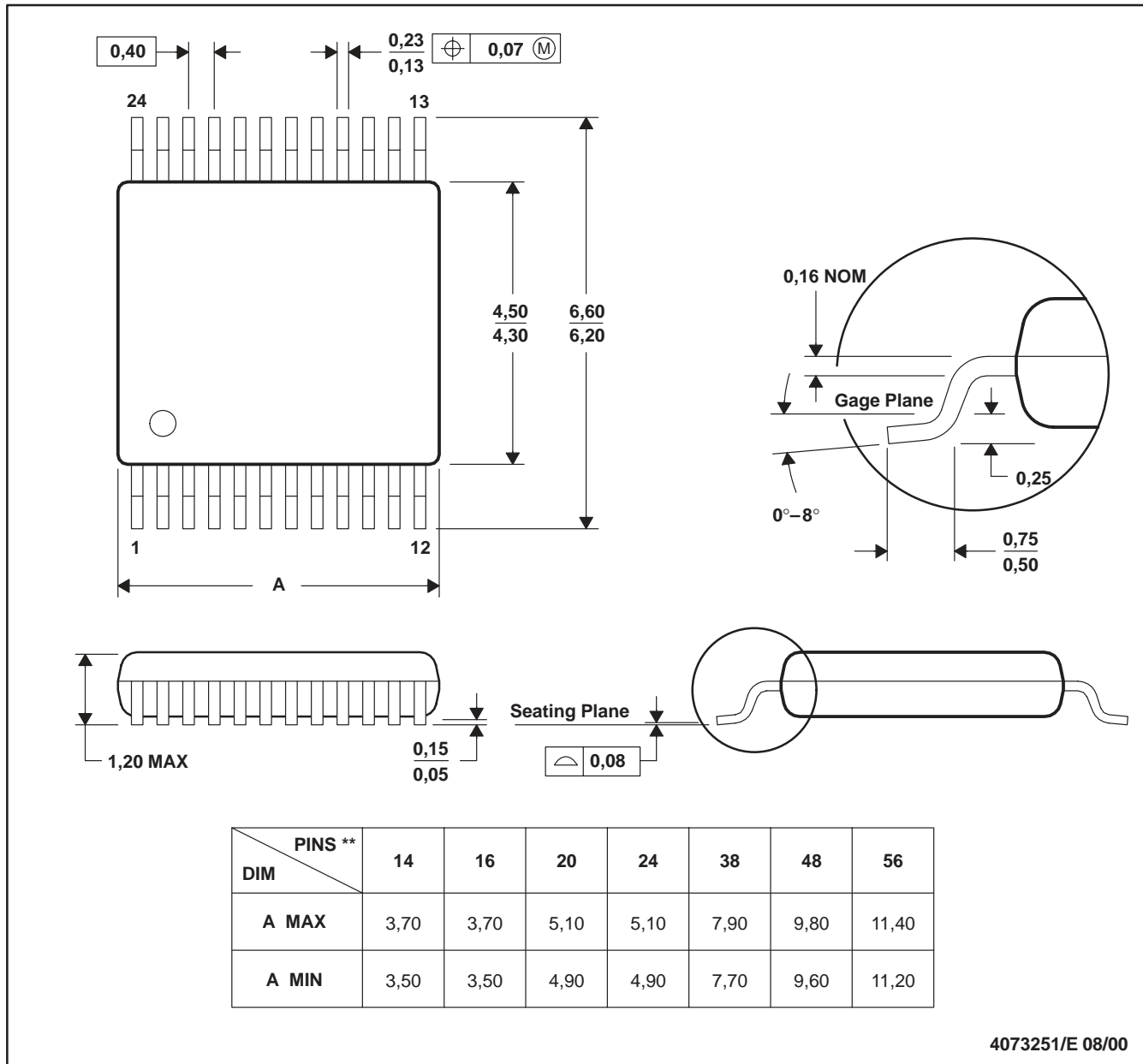

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT16212CDL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

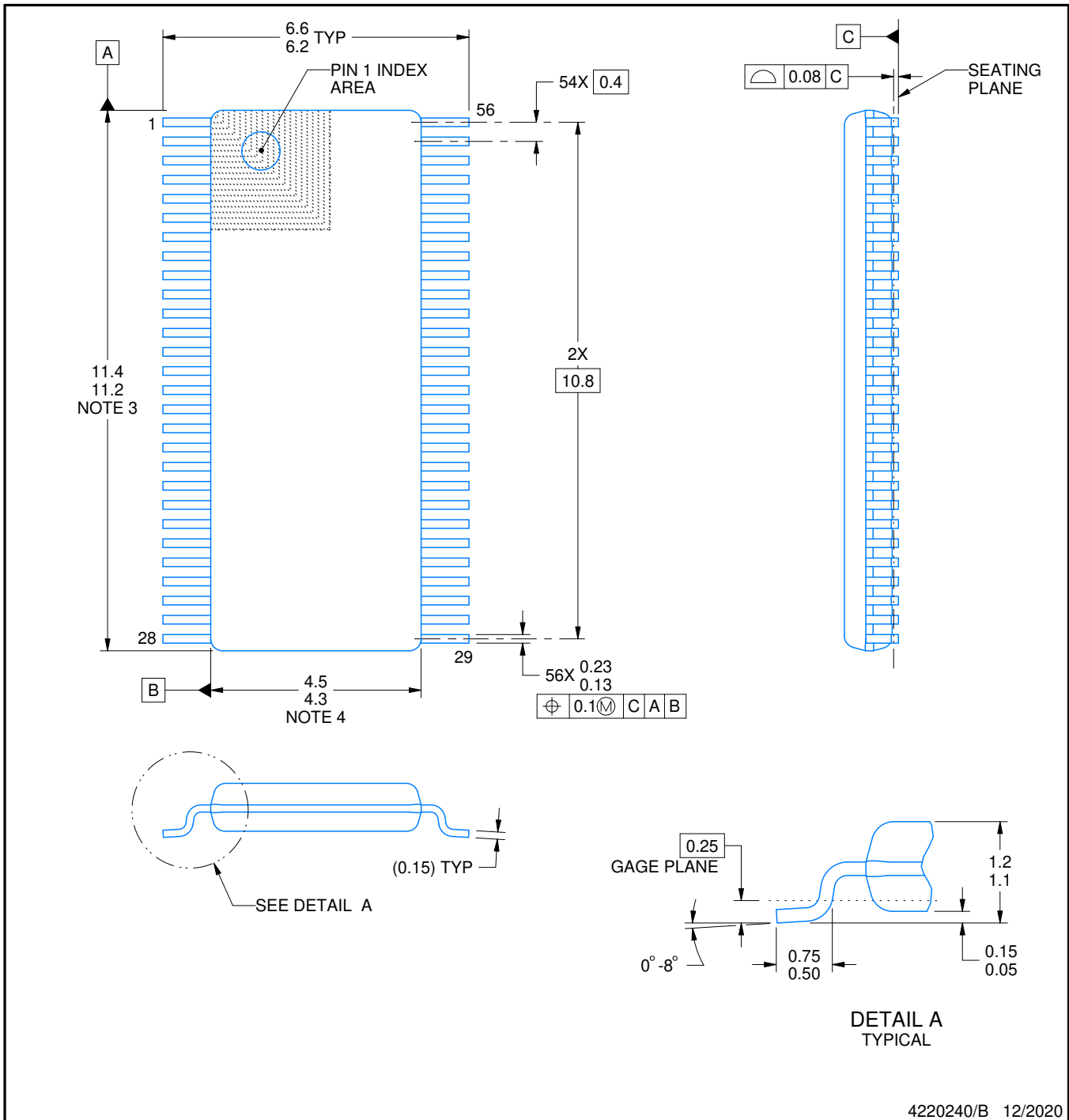
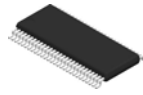
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



NOTES:

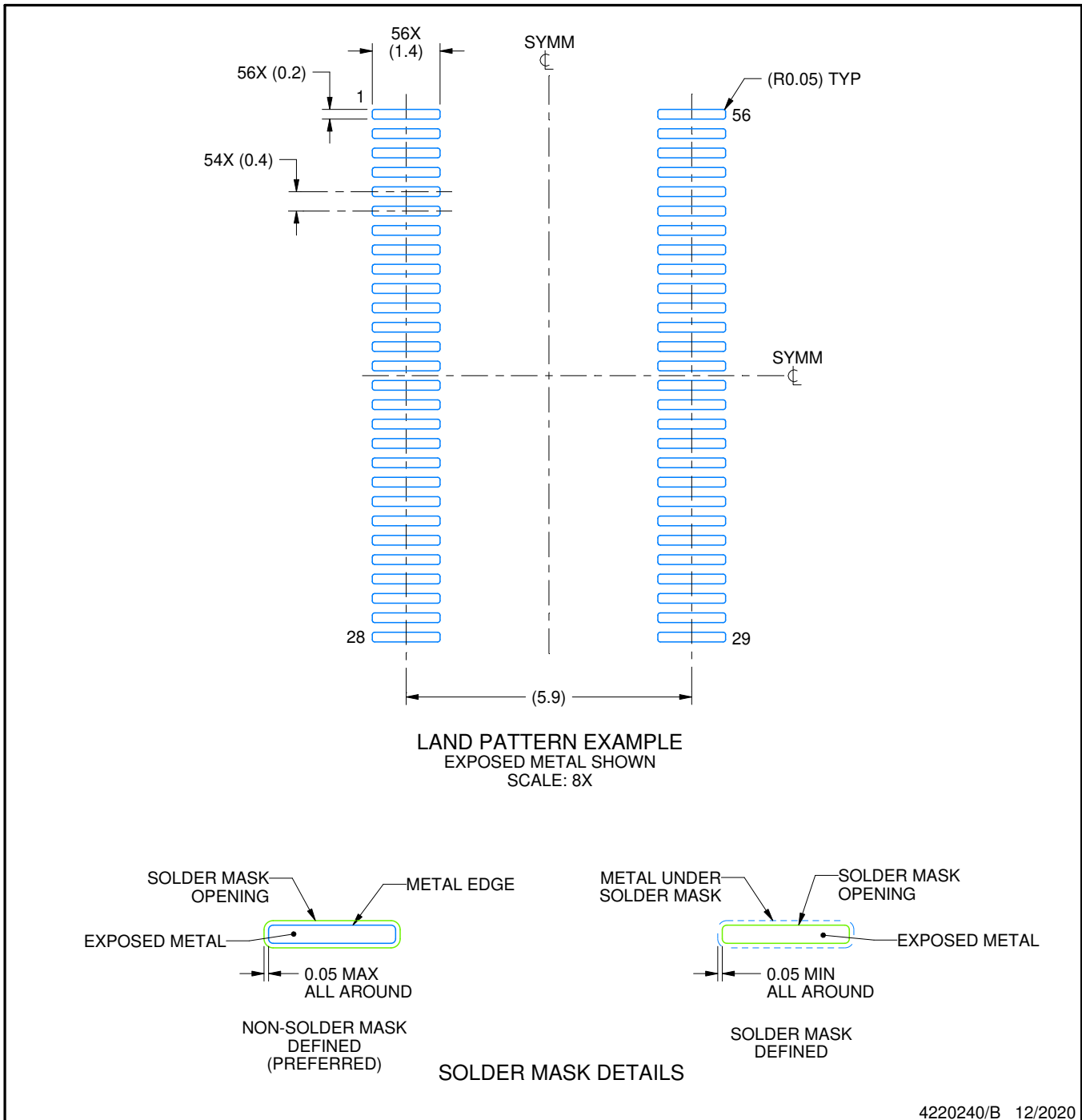
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

EXAMPLE BOARD LAYOUT

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

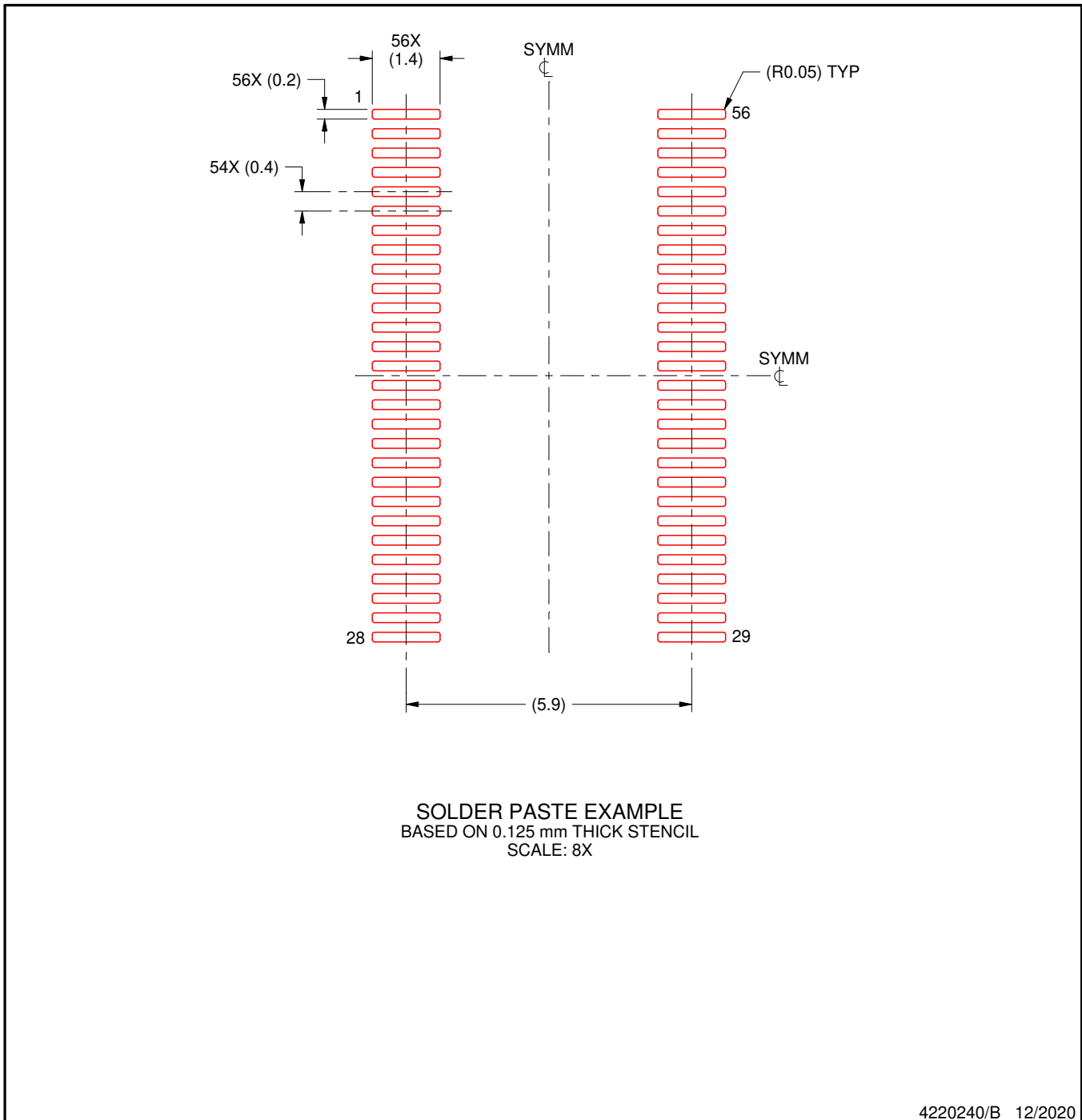
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



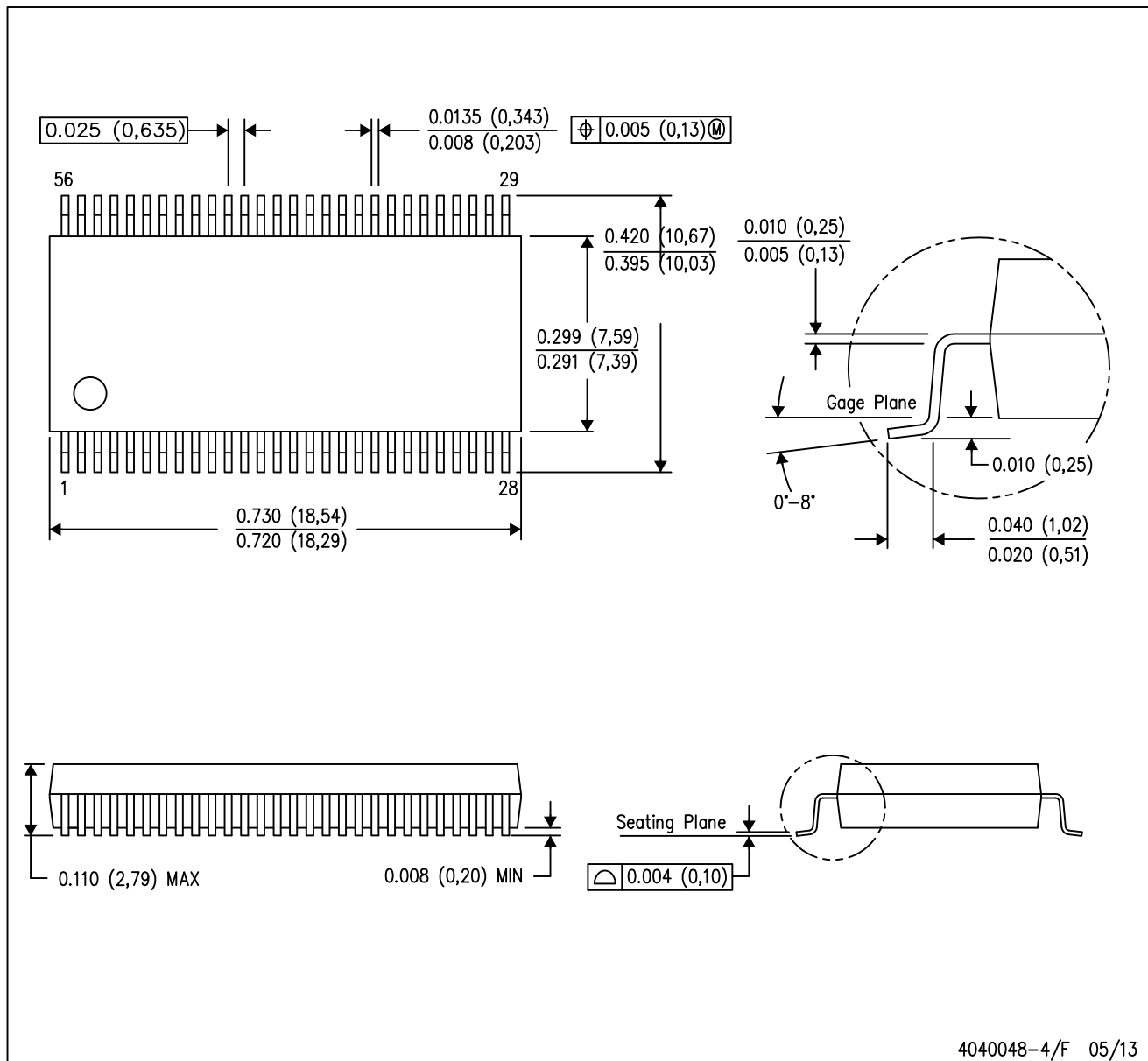
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

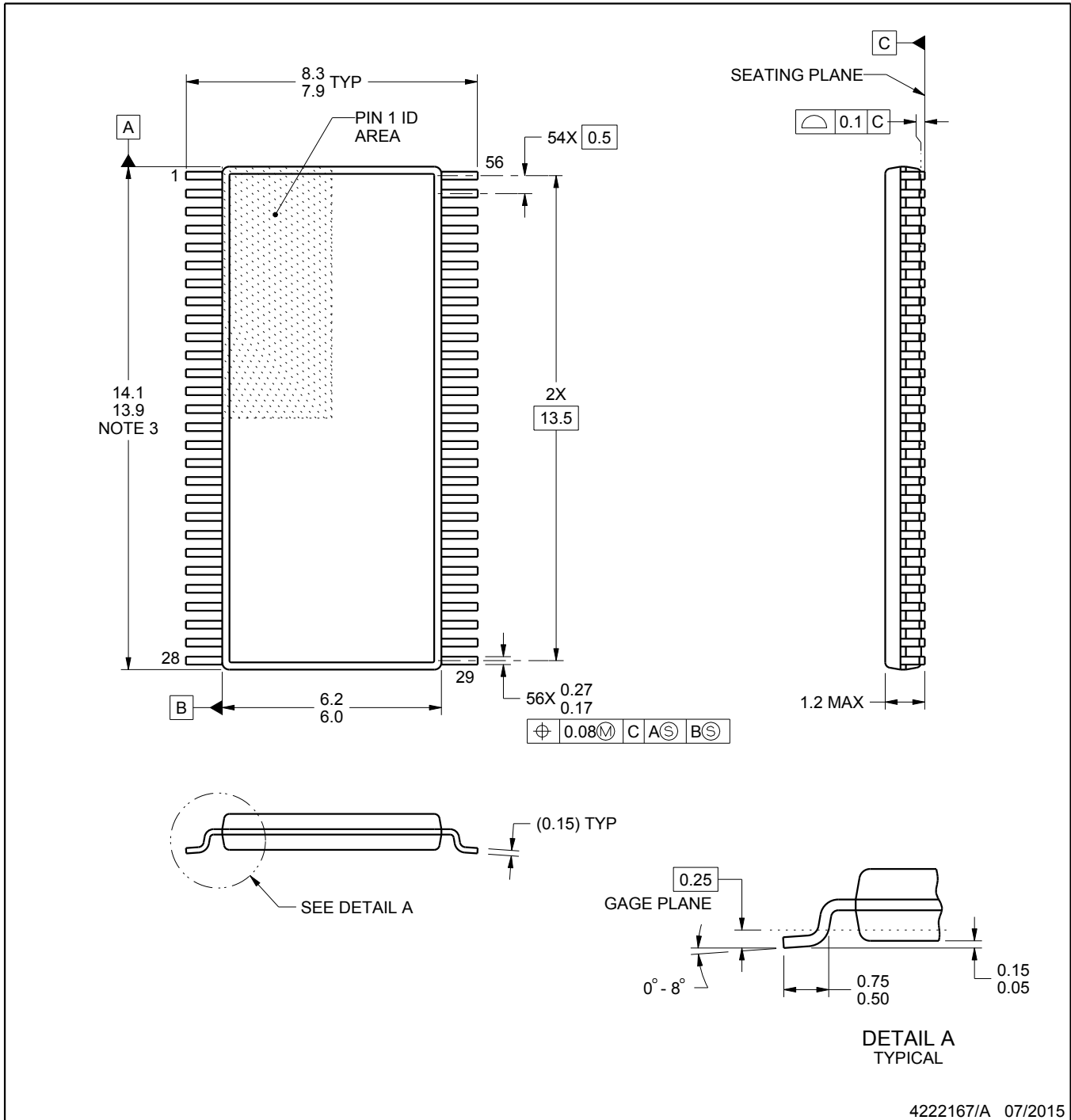
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



4222167/A 07/2015

NOTES:

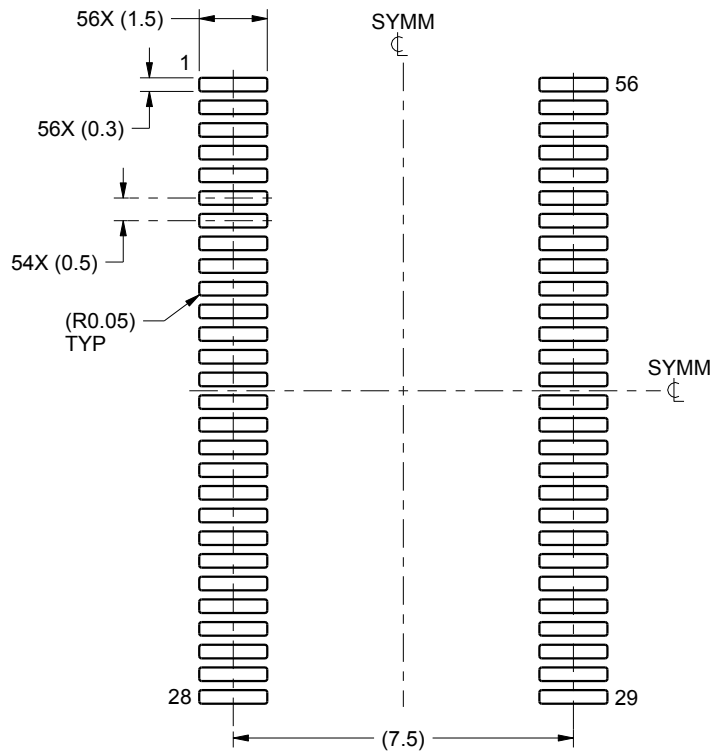
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

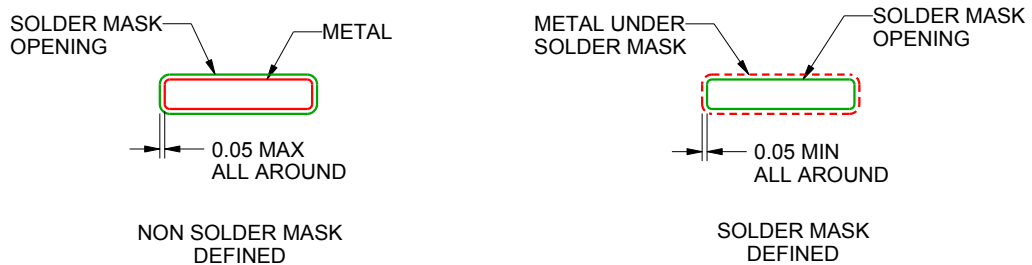
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

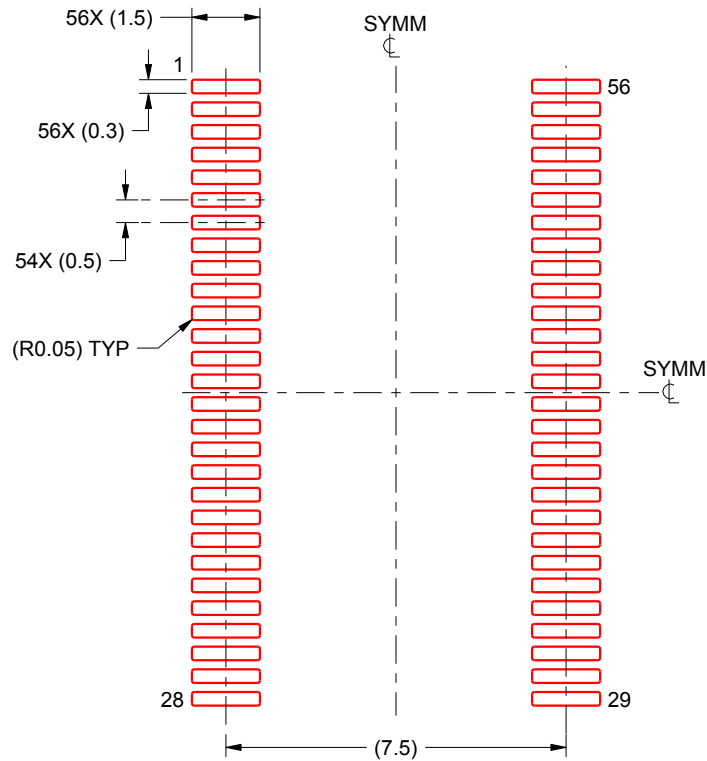
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated