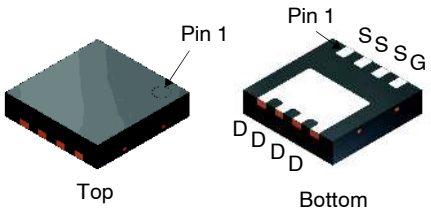
MOSFET – P-Channel, POWERTRENCH®

-20 V, -56 A, 6.5 mΩ

FDMC6688P

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
−20 V	6.5 mΩ @ −4.5 V	−56 A
	9.8 mΩ @ −2.5 V	
	20 mΩ @ −1.8 V	



PQFN8 3.3X3.3, 0.65P
(Power 33)
CASE 483AX

General Description

This P−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for $R_{DS(on)}$, switching performance and ruggedness.

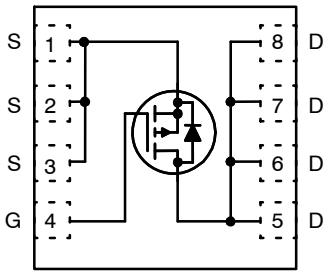
Features

- Max $R_{DS(on)}$ = 6.5 mΩ at V_{GS} = −4.5 V, I_D = −14 A
- Max $R_{DS(on)}$ = 9.8 mΩ at V_{GS} = −2.5 V, I_D = −11 A
- Max $R_{DS(on)}$ = 20 mΩ at V_{GS} = −1.8 V, I_D = −9 A
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- Load Switch
- Battery Management
- Power Management
- Reverse Polarity Protection

PIN ASSIGNMENT



MARKING DIAGRAM

Z = Assembly Plant Code
YWW = Date Code (Year & Week)
KK = Lot Traceability Code
FDMC6688P = Specific Device Code

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	−20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current −Continuous, T_C = 25°C −Continuous, T_A = 25°C (Note 1a) −Pulsed (Note 3)	 −56 −14 −226	A
P_D	Power Dissipation T_C = 25°C T_A = 25°C (Note 1a)	 30 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
FDMC6688P	PQFN8 (Power 33) (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

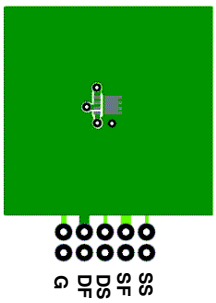
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−20	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	–	−16	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V	–	–	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−0.4	−0.75	−1	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	–	3	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On−Resistance	V_{GS} = −4.5 V, I_D = −14 A	–	5.3	6.5	mΩ
		V_{GS} = −2.5 V, I_D = −11 A	–	7	9.8	
		V_{GS} = −1.8 V, I_D = −9 A	–	10.7	20	
		V_{GS} = −4.5 V, I_D = −14 A, T_J = 125°C	–	7.3	11	
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −14 A	–	80	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	–	4956	7435	pF
C_{oss}	Output Capacitance		–	678	1020	pF
C_{rss}	Reverse Transfer Capacitance		–	618	930	pF
R_g	Gate Resistance		–	4.5	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −10 V, I_D = −14 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	–	19	35	ns
t_r	Rise Time		–	33	53	ns
$t_{d(off)}$	Turn−Off Delay Time		–	119	190	ns
t_f	Fall Time		–	68	109	ns
Q_g	Total Gate Charge	V_{DD} = −10 V, I_D = −14 A, V_{GS} = −4.5 V	–	44	61	nC
Q_{gs}	Gate to Source Charge		–	7.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	11	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −14 A (Note 2)	–	−0.8	−1.2	V
		V_{GS} = 0 V, I_S = −2 A (Note 2)	–	−0.6	−1.2	
t_{rr}	Reverse Recovery Time	I_F = −14 A, di/dt = 100 A/μs	–	26	41	ns
Q_{rr}	Reverse Recovery Charge		–	10	20	nC

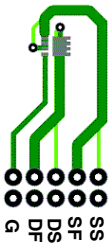
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Pulse Id refers to Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS

(T_J = 25°C Unless Otherwise Noted)

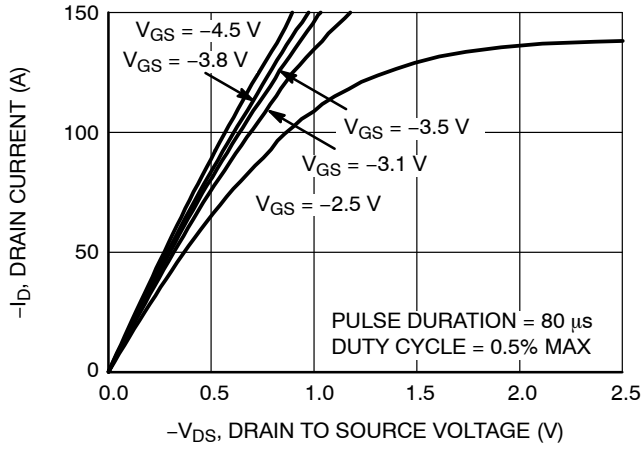


Figure 1. On−Region Characteristics

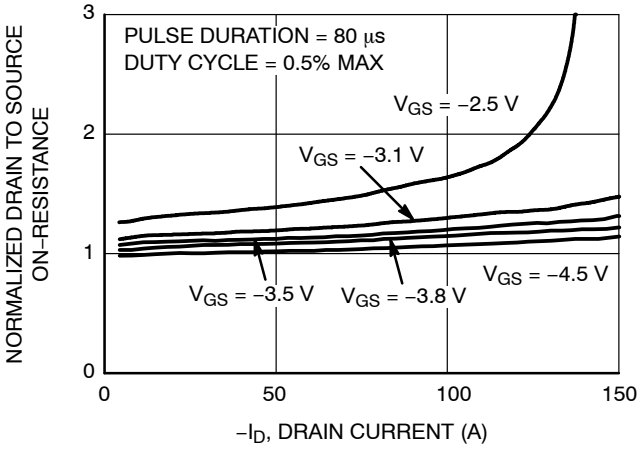


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

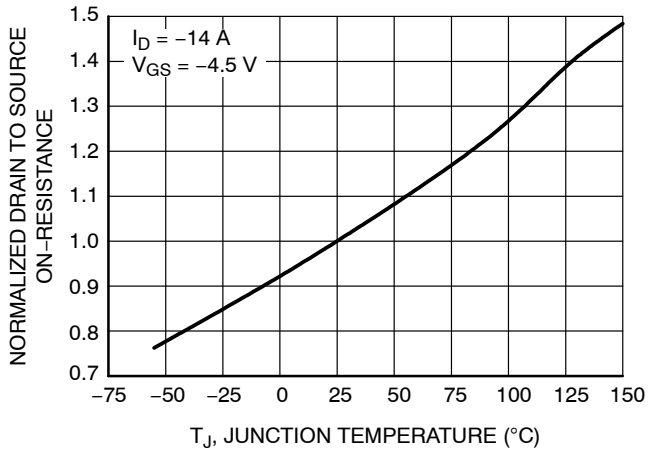


Figure 3. Normalized On−Resistance vs. Junction Temperature

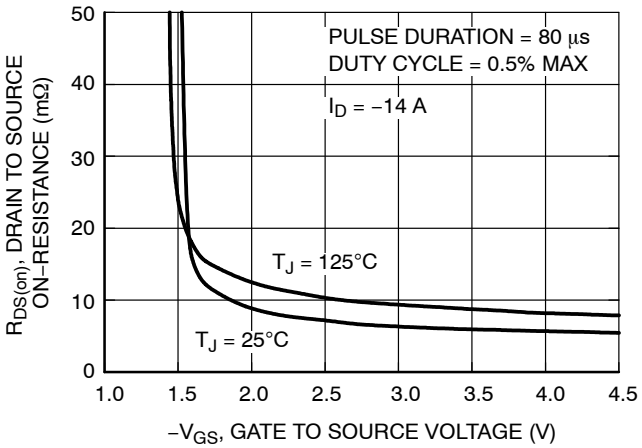


Figure 4. On−Resistance vs. Gate to Source Voltage

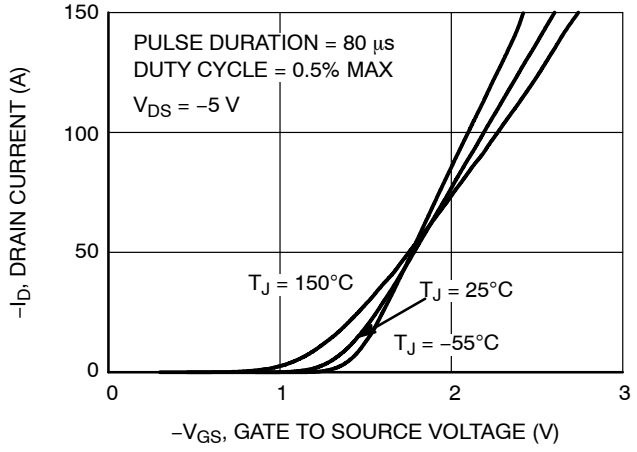


Figure 5. Transfer Characteristics

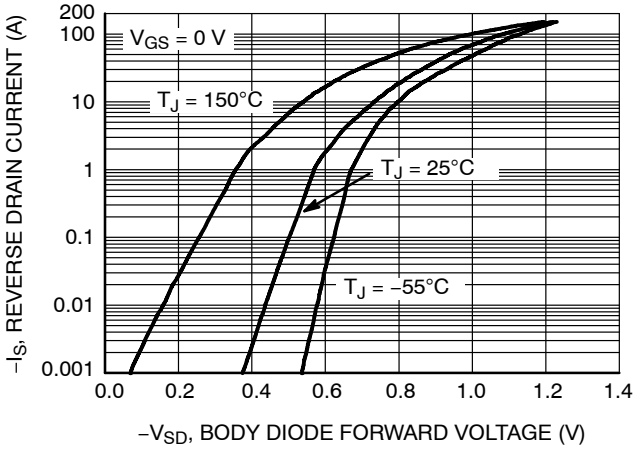


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(T_J = 25°C Unless Otherwise Noted)

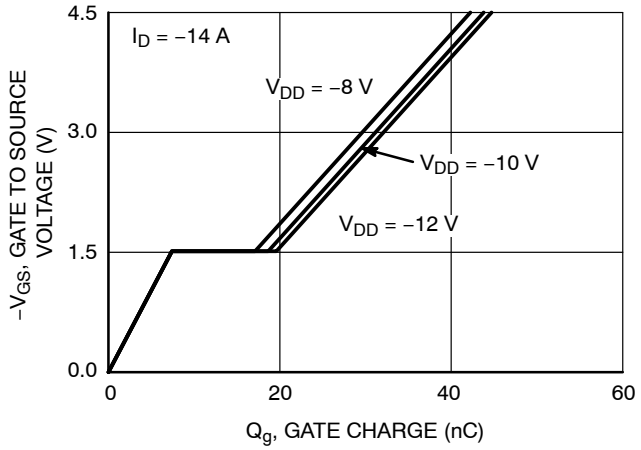


Figure 7. Gate Charge Characteristics

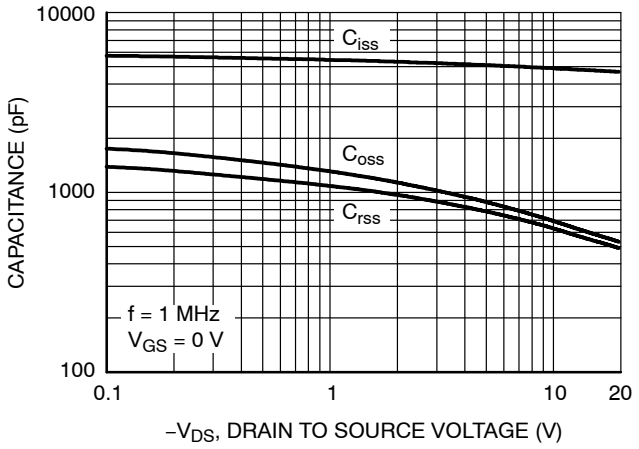


Figure 8. Capacitance vs. Drain to Source Voltage

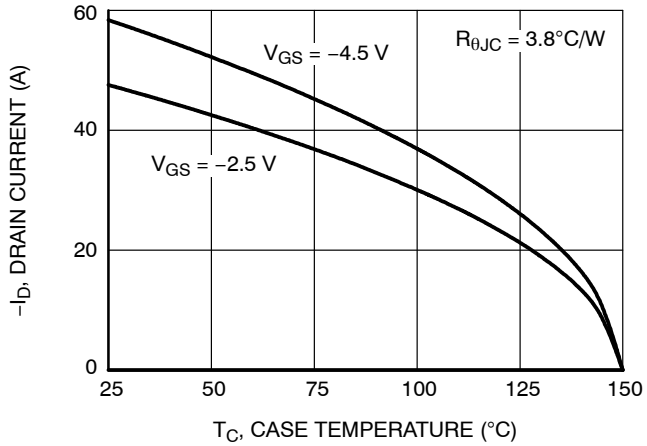


Figure 9. Maximum Continuous Drain Current vs. Case Temperature

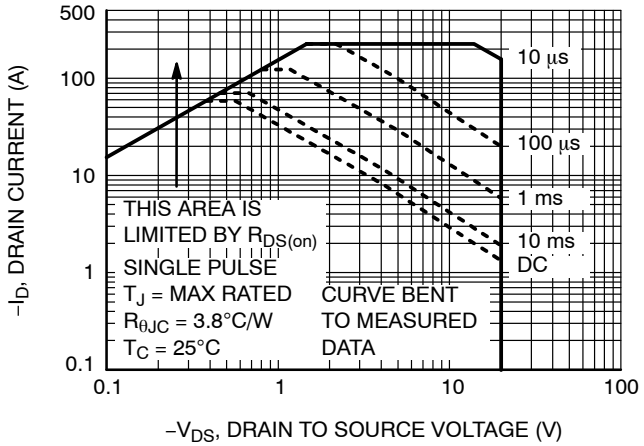


Figure 10. Forward Bias Safe Operating Area

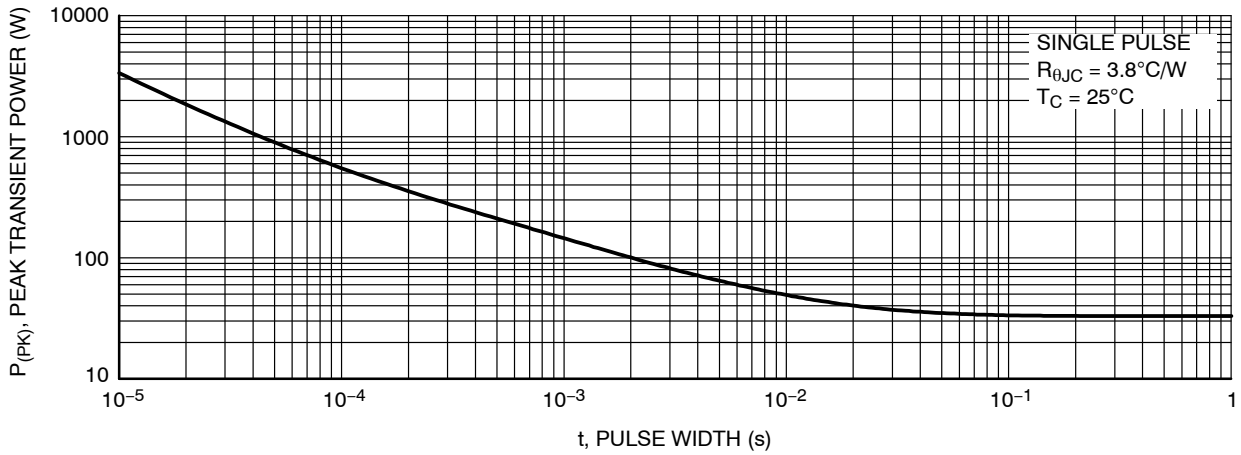


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

(T_J = 25°C Unless Otherwise Noted)

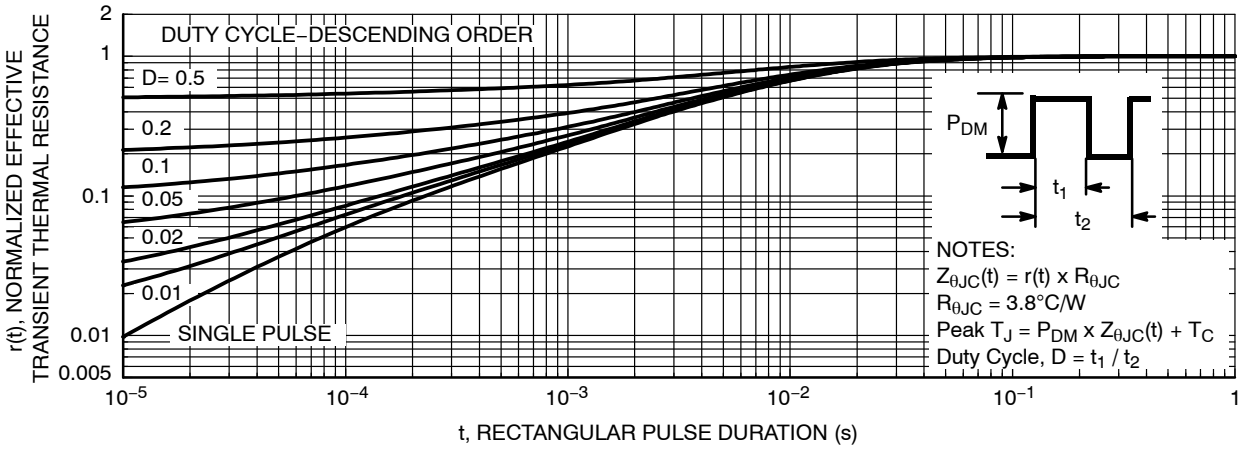
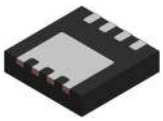


Figure 12. Junction−to−Case Transient Thermal Response Curve

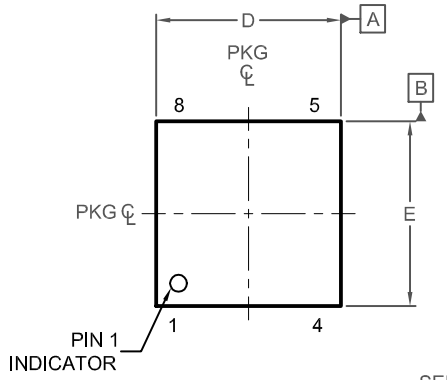
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

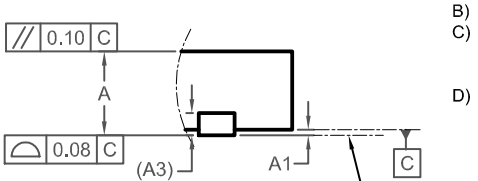
ON Semiconductor®



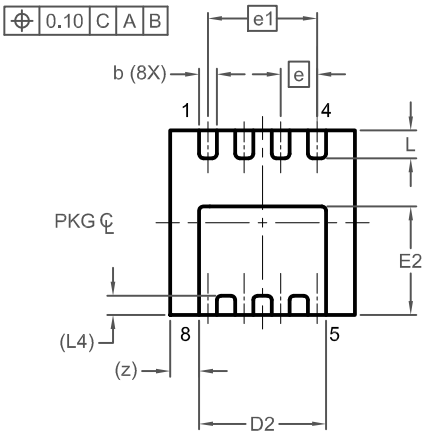
PQFN8 3.3X3.3, 0.65P
CASE 483AX
ISSUE B

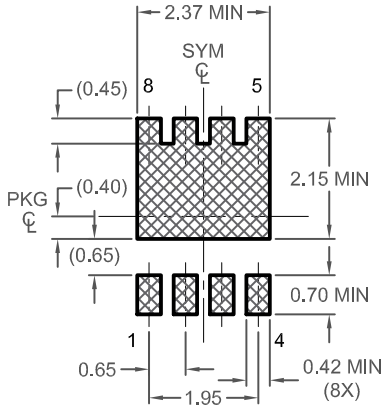
DATE 24 JUN 2022





DETAIL A
SCALE: 2X





LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
E	3.20	3.30	3.40
E2	1.84	1.94	2.04
e		0.65 BSC	
e1		1.95 BSC	
L	0.40	0.50	0.60
L4		0.34 REF	
z		0.52 REF	

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