



DS1649/DS3649/DS1679/DS3679 Hex TRI-STATE® TTL to MOS Drivers

General Description

The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

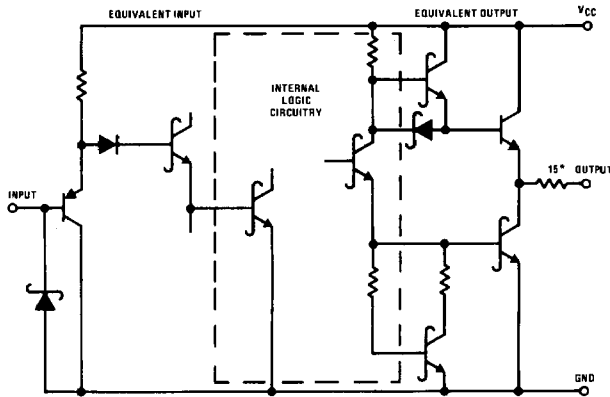
The DS1649/DS3649 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast-switching

output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
 - Typ 9 ns driving 50 pF
 - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



*DS1649/DS3649 only

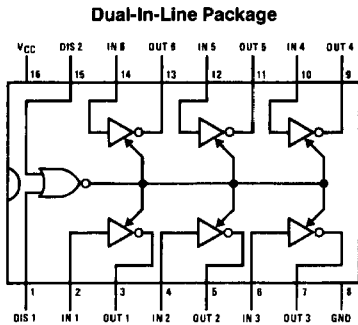
TL/F/7515-1

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care
Hi-Z = TRI-STATE mode

Connection Diagram

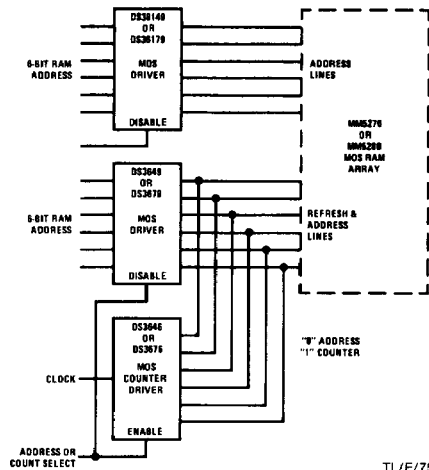


Top View

TL/F/7515-2

Order Number DS1649J, DS3649J,
DS1679J, DS3679J, DS3649N or DS3679N
See NS Package Number J16A or N16A

Typical Application



TL/F/7515-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	-1.5V
Storage Temperature Range	-65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1649, DS1679	-55	+125	°C
DS3649, DS3679	0	+70	°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Electrical Characteristics (Note 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V	
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V	
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5.5V, V_{IN} = 5.5V$		0.1	40	μA	
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5.5V, V_{IN} = 0.5V$		-50	-250	μA	
V_{CLAMP}	Input Clamp Voltage	$V_{CC} = 4.5V, I_{IN} = -18 mA$		-0.75	-1.2	V	
V_{OH}	Logical "1" Output Voltage (No Load)	$V_{CC} = 4.5V, I_{OH} = -10 \mu A$	DS1649/DS1679	2.7	3.6		V
			DS3649/DS3679	2.8	3.6		
V_{OL}	Logical "0" Output Voltage (No Load)	$V_{CC} = 4.5V, I_{OL} = 10 \mu A$	DS1649/DS1679		0.25	0.4	V
			DS3649/DS3679		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	$V_{CC} = 4.5V, I_{OH} = -1.0 mA$	DS1649	2.4	3.5		V
			DS1679	2.5	3.5		V
			DS3649	2.6	3.5		V
			DS3679	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	$V_{CC} = 4.5V, I_{OL} = 20 mA$	DS1649		0.6	1.1	V
			DS1679		0.4	0.5	V
			DS3649		0.6	1.0	V
			DS3679		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	$V_{CC} = 4.5V, V_{OUT} = 0V$ (Note 4)		-250		mA	
I_{0D}	Logical "0" Drive Current	$V_{CC} = 4.5V, V_{OUT} = 4.5V$ (Note 4)		150		mA	
Hi-Z	TRI-STATE Output Current	$V_{OUT} = 0.4V$ to $2.4V$, DIS1 or DIS2 = 2.0V	-40		40	μA	
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$	One DIS Input = 3.0V All Other Inputs = X		42	75	mA
			All Inputs = 0V		11	20	mA

Switching Characteristics ($V_{CC} = 5V, T_A = 25^\circ C$) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{S\pm}$	Storage Delay Negative Edge	(Figure 1) $C_L = 50\text{ pF}$		4.5	7	ns
		$C_L = 500\text{ pF}$		7.5	12	ns
$t_{S\pm}$	Storage Delay Positive Edge	(Figure 1) $C_L = 50\text{ pF}$		5	8	ns
		$C_L = 500\text{ pF}$		8	13	ns
t_F	Fall Time	(Figure 1) $C_L = 50\text{ pF}$		5	8	ns
		$C_L = 500\text{ pF}$		22	35	ns
t_R	Rise Time	(Figure 1) $C_L = 50\text{ pF}$		6	9	ns
		$C_L = 500\text{ pF}$		21	35	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	$C_L = 50\text{ pF}$ $R_L = 2\text{ k}\Omega$ to V_{CC} (Figure 2)		10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$C_L = 50\text{ pF}$ $R_L = 2\text{ k}\Omega$ to GND (Figure 2)		8	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	$C_L = 50\text{ pF}$ $R_L = 400\Omega$ to V_{CC} (Figure 3)		15	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	$C_L = 50\text{ pF}$ $R_L = 400\Omega$ to GND (Figure 3)		10	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the $-55^\circ C$ to $+125^\circ C$ temperature range for the DS1649 and DS1679 and across the $0^\circ C$ to $+70^\circ C$ range for the DS3649 and DS3679. All typical values are for $T_A = 25^\circ C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

AC Test Circuits and Switching Time Waveforms

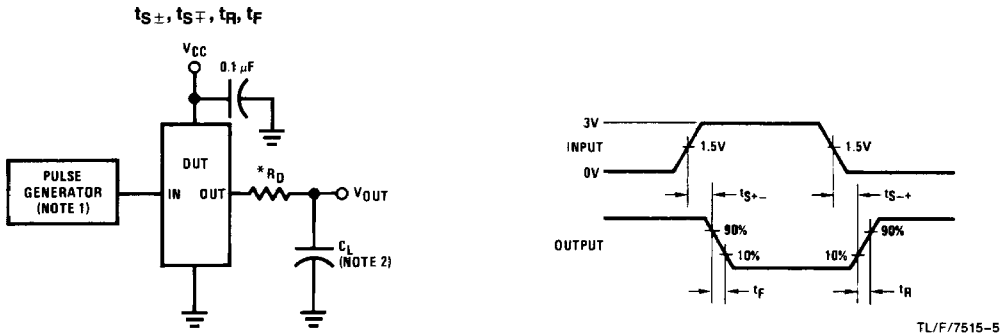
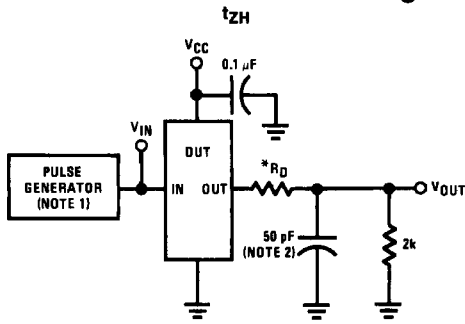
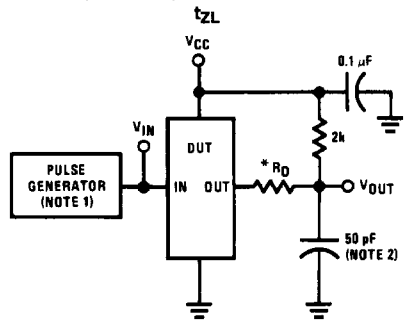


FIGURE 1

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/7515-6



TL/F/7515-7

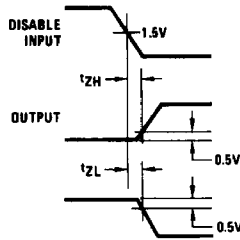
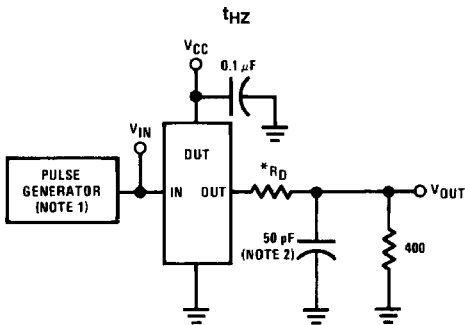
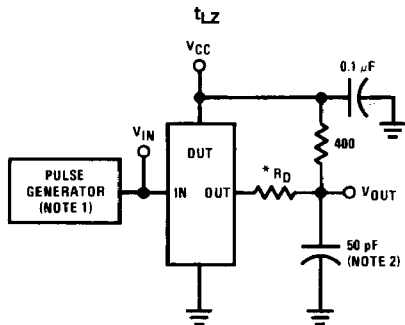


FIGURE 2

TL/F/7515-8



TL/F/7515-9



TL/F/7515-10

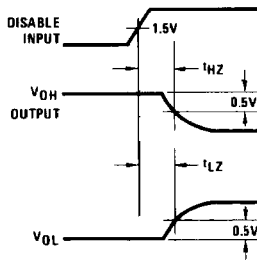


FIGURE 3

TL/F/7515-11

*Internal on DS1649 and DS3649

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$ and $PRR \leq 1\text{ MHz}$. Rise and fall times between 10% and 90% points $\leq 5\text{ ns}$.
Note 2: C_L includes probe and jig capacitance.