Mercury ZX1 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury ZX1 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury ZX1 SoC module.

Summary

This document first gives an overview of the Mercury ZX1 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-ZX1	Mercury ZX1 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-403-002	07	20.01.2022

Approval Information	Name	Position	Date
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Document History

Version	Date	Author	Comment
07	20.01.2022	WRUH	Corrected component height on top side
06	16.02.2021	DIUN	Added information on Mercury heatsinks, added Mercury+ ST1 to accesories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
05	25.07.2019	DIUN	Added information on voltage monitoring, power supplies, heat sink, Linux how-to guide, updated DDR memory types and EEPROM map description, corrected module dimensions, other style updates
04	21.08.2018	DIUN	Minor corrections and style updates
03	29.09.2017	DIUN	Updated for revision 3
02	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
01	27.12.2016	DIUN	Version 01

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

The Mercury ZX1 SoC module combines the Xilinx Zynq® -7030/7035/7045 All Programmable SoC (System-on-Chip) device with USB 2.0 On-The-Go PHY, PCIe® Gen2 ×4/×8, Gigabit Ethernet PHY, dual Fast Ethernet PHY, two fast DDR3 SDRAM memory channels, NAND flash, multi-gigabit transceivers, high-speed LVDS I/O, and a real-time clock, forming a complete and powerful embedded processing system.

The use of the Mercury ZX1 SoC module, in contrast to building a custom SoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mercury base boards, the Mercury ZX1 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [14] is available for the Mercury ZX1 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target and download all the required binaries, such as bitstream and FSBL (First Stage Boot Loader). It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mercury ZX1 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mercury ZX1 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mercury ZX1 SoC module.

1.1.5 Safety Recommendations and Warnings

Mercury modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury ZX1 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

It is possible to mount the Mercury ZX1 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury ZX1 SoC module.

The base board and module may be damaged if the module is mounted the wrong way round and powered up.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury ZX1 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Zynq®-7030/7035/7045 All Programmable SoC, FBG676/FFG676 package
  - Dual ARM® Cortex™-A9 MPCore™with CoreSight™ and NEON™ extension
  - Xilinx Kintex-7 28 nm FPGA fabric
- *Zynq-7030*: 170 user I/Os
  - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART) shared with FPGA I/Os
  - 138 FPGA I/Os (single-ended or differential)
    - 66 FPGA I/Os up to 3.3 V
    - 84 FPGA I/Os up to 1.8 V
  - 20 MGT signals (clock and data)
- *Zynq-7035/7045*: 178 user I/Os
  - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART) shared with FPGA I/Os
  - 126 FPGA I/Os (single-ended or differential)
    - 66 FPGA I/Os up to 3.3 V
    - 72 FPGA I/Os up to 1.8 V
  - 40 MGT signals (clock and data)
- *Zynq-7030*: 4 MGTs @ 6.6 Gbit/sec and 2 reference input clock differential pairs
- *Zynq-7035*: 8 MGTs @ 6.6 Gbit/sec and 4 reference input clock differential pairs
- *Zynq-7045*: 8 MGTs @ 10.3125 Gbit/sec and 4 reference input clock differential pairs
- PCIe Gen2 ×4/×8 (Xilinx integrated PCIe block)
- 1 GB DDR3 SDRAM connected to the Processing System (PS)
- 256 MB DDR3 SDRAM connected to the Programmable Logic (PL)
- 512 MB NAND flash
- 64 MB quad SPI flash
- Gigabit Ethernet
- Dual Fast Ethernet
- USB 2.0 On-The-Go (OTG)
- Real-time clock
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury ZX1 SoC module
- Mercury ZX1 SoC module documentation, available via download:
  - Mercury ZX1 SoC Module User Manual (this document)
  - Mercury ZX1 SoC Module Reference Design [2]
  - Mercury ZX1 SoC Module IO Net Length Excel Sheet [3]
  - Mercury ZX1 SoC Module FPGA Pinout Excel Sheet [4]
  - Mercury ZX1 SoC Module User Schematics (PDF) [5]
  - Mercury ZX1 SoC Module Known Issues and Changes [6]
  - Mercury ZX1 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mercury ZX1 SoC Module 3D Model (PDF) [8]
  - Mercury ZX1 SoC Module STEP 3D Model [9]
  - Mercury Mars Module Pin Connection Guidelines [10]
  - Mercury Master Pinout [11]
  - Mercury Heatsink Application Note [17]
  - Enclustra Build Environment [14] (Linux build environment; refer to Section 1.4.2 for details)
  - Enclustra Build Environment How-To Guide [15]

1.4 Accessories

1.4.1 Reference Design

The Mercury ZX1 SoC module reference design features an example configuration for the Zynq-7000 SoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [14] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [15] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.4.3 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.11.6 for further information on the available cooling options.

1.4.4 Mercury+ PE1 Base Board

- 168-pin Hirose FX10 module connectors (PE1-200: 2 connectors; PE1-300/400: 3 connectors)
- System controller
- Power control
- System monitor (PE1-300/400)
- Current sense (PE1-300/400)
- Low-jitter clock generator (PE1-300/400)
- microSD card holder
- User EEPROM
- eMMC managed NAND flash (PE1-300/400)
- PCIe ×4 interface
- USB 3.0 device connector
- USB 2.0 host connector (PE1-200: 1 connector; PE1-300/400: 4 connectors)
- Micro USB 2.0 device (UART, SPI, I2C, JTAG) connector
- 2 × RJ45 Gigabit Ethernet connectors
- mPCIe/mSATA card holder (USB only) (PE1-300/400)
- SIM card holder (optional, PE1-300/400 only)
- SMA clock and data in/out (optional, PE1-300/400 only)
- 1 × FMC LPC connector (PE1-200)
- 1 × FMC HPC connector (PE1-300)
- 2 × FMC LPC connector (PE1-400)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- 5 to 15 V DC supply voltage
- USB bus power (with restrictions)

Please note that the available features depend on the equipped Mercury module type and on the selected base board variant.

1.4.5 Mercury+ ST1 Base Board

- 168-pin Hirose FX10 module connectors (3 connectors)
- 2 × MIPI D-PHY connectors: CSI and CSI/DSI (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- SFP+ connector
- Low-jitter clock generator
- USB 3.0 device connector
- USB 3.0 host connector
- FTDI USB 2.0 device controller with micro USB device connector (UART, SPI, I2C, JTAG)
- 2 × RJ45 Gigabit Ethernet connectors
- 1 × FMC HPC connector (note: not all pins are available)
- 2 × 40-pin Anios pin header
- 3 × 12-pin IO headers
- microSD card holder
- 5 to 15 V DC supply voltage
- Form factor: 100 × 120 mm

Please note that the available features depend on the equipped Mercury module type.

1.5 Xilinx Tool Support

The SoC devices equipped on the Mercury ZX1 SoC module are supported by the Vivado HL WebPACK Edition or by the Vivado HL Design Edition software, depending on the device's density. Table 1 presents the correspondence between devices and tools. Please contact Xilinx for further information.

Module	Xilinx Tool Support	Costs
ME-ZX1-30	Vivado HL WebPACK Edition	Free of charge
ME-ZX1-35	Vivado HL Design Edition	Paid license required
ME-ZX1-45	Vivado HL Design Edition	Paid license required

Table 1: Xilinx Tool Support

2 Module Description

2.1 Block Diagram

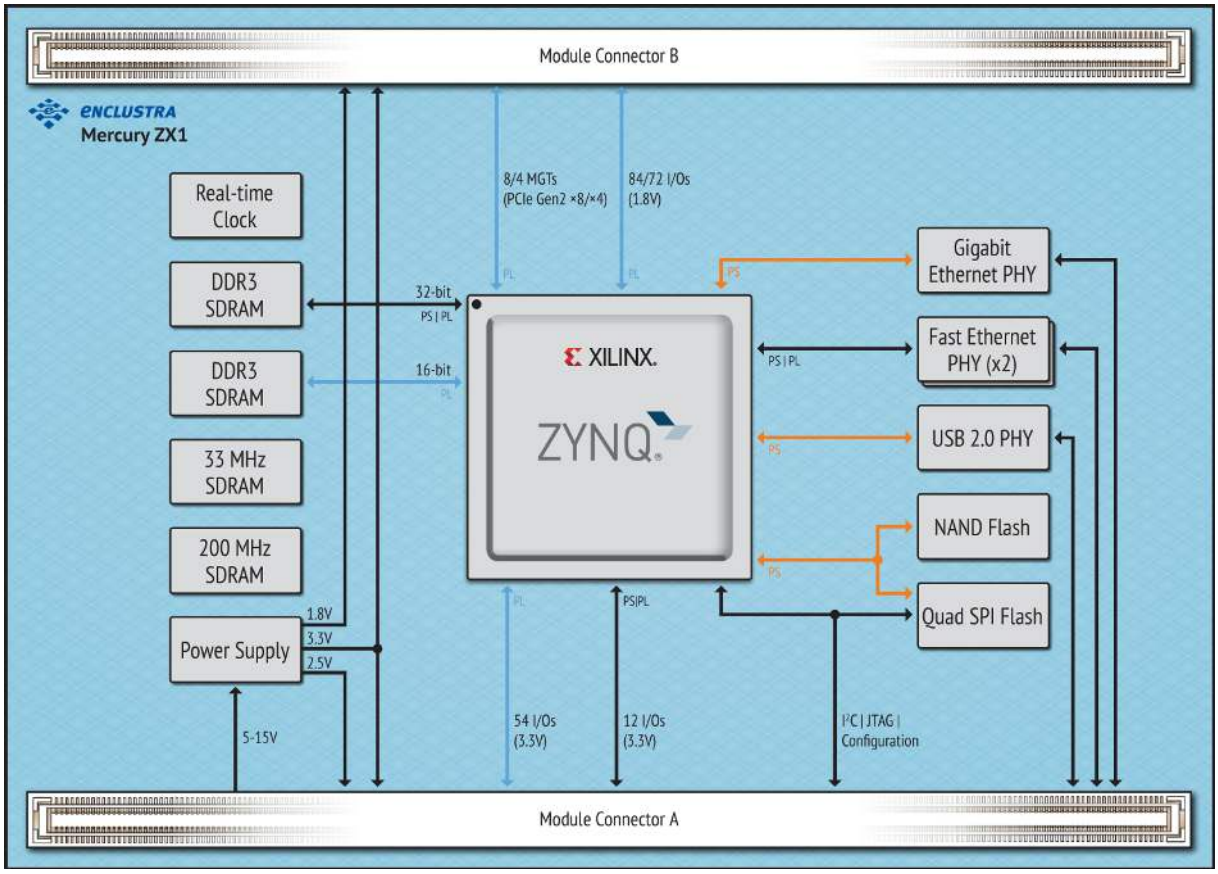

Figure 1: Hardware Block Diagram

The main component of the Mercury ZX1 SoC module is the Xilinx Zynq-7000 SoC device. Most of its I/O pins are connected to the Mercury module connector, making up to 150 regular user I/Os available to the user. Further, up to eight multi-gigabit transceivers with support for PCIe Gen2 ×8 are available on the module connector.

The SoC device can boot from the on-board QSPI flash, NAND flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The memory subsystem is built from a 512 MB NAND flash, a 64 MB quad SPI flash, 1 GB DDR3 SDRAM connected to the Processing System (PS) and 256 MB DDR3 SDRAM connected to the Programmable Logic (PL).

Further, the module is equipped with a Gigabit Ethernet PHY, dual Fast Ethernet PHY, and a USB 2.0 OTG PHY, making it ideal for communication applications.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 33.33 MHz crystal oscillator for the PS and a 200 MHz LVDS oscillator for the PL.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Four LEDs are connected to the SoC pins for status signaling.

2.2 Module Configuration and Product Models

Table 2 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Model	SoC	DDR3/DDR3L SDRAM (PS)	DDR3/DDR3L SDRAM (PL)	Temperature Range
ME-ZX1-30-2I-D10	XC7Z030-2FBG676I	1024 MB	256 MB	-40 to +85° C
ME-ZX1-35-1I-D10	XC7Z035-1FBG676I	1024 MB	256 MB	-40 to +85° C
ME-ZX1-45-2I-D10-P	XC7Z045-2FFG676I	1024 MB	256 MB	-40 to +85° C

Table 2: Standard Module Configurations

The product model indicates the module type and main features. Figure 2 describes the fields within the product model.

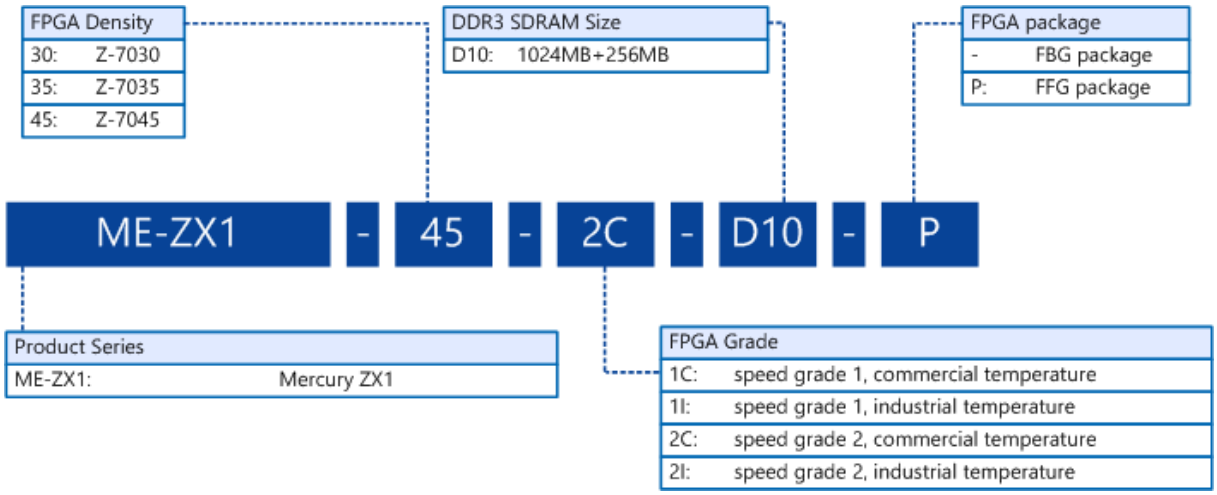

Figure 2: Product Model Fields

Please note that for the first revision modules or early access modules, the product model may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 EN-Numbers and Part Names

Every module is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

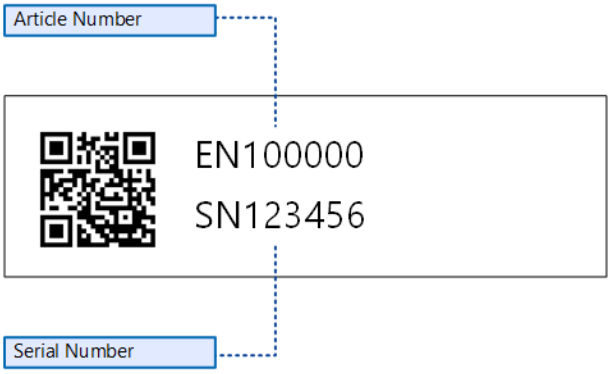

Figure 3: Module Label

The correspondence between EN-number and part name is shown in Table 3. The part name represents the product model, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mercury ZX1 SoC Module Known Issues and Changes document [6].

EN-Number	Part Name
EN100644	ME-ZX1-30-2I-D10-R1
EN100645	ME-ZX1-35-1I-D10-R1
EN100646	ME-ZX1-45-2I-D10-P-R1
EN101075	ME-ZX1-30-2C-D10-R2
EN101076	ME-ZX1-30-2I-D10-R2
EN101077	ME-ZX1-35-1C-D10-R2
EN101078	ME-ZX1-35-1I-D10-R2
EN101079	ME-ZX1-45-2C-D10-P-R2
EN101080	ME-ZX1-45-2I-D10-P-R2
EN101723	ME-ZX1-30-2C-D10-R3
EN101724	ME-ZX1-30-2I-D10-R3
EN101725	ME-ZX1-35-1C-D10-R3
EN101726	ME-ZX1-35-1I-D10-R3
EN101727	ME-ZX1-45-2C-D10-P-R3
EN101728	ME-ZX1-45-2I-D10-P-R3

Table 3: EN-Numbers and Part Names

2.4 Top and Bottom Views

2.4.1 Top View

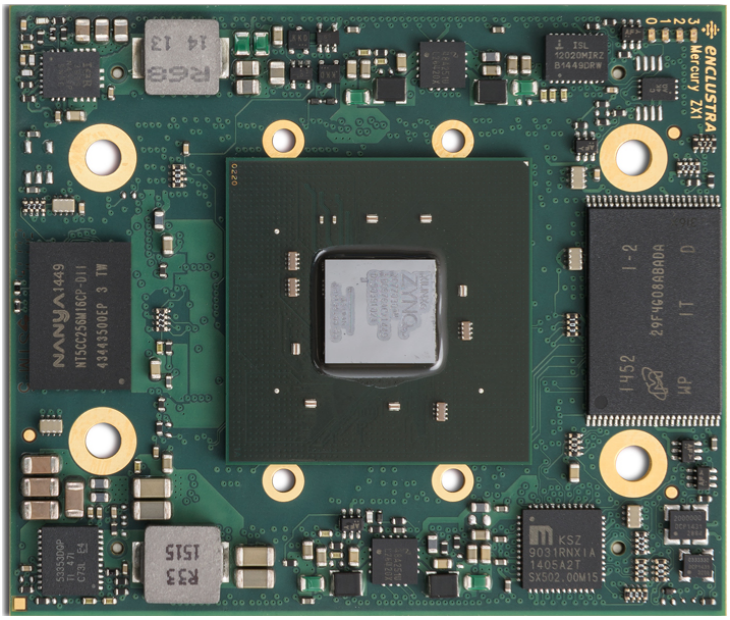

Figure 4: Module Top View

2.4.2 Bottom View

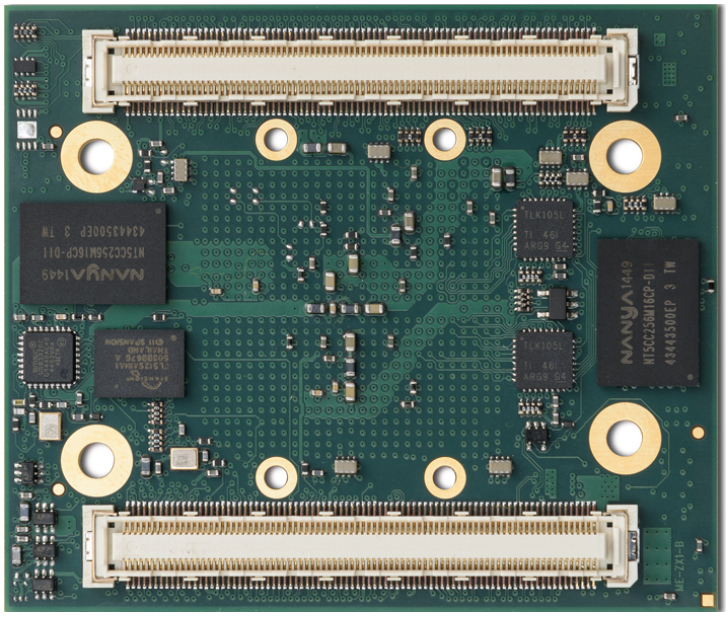

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

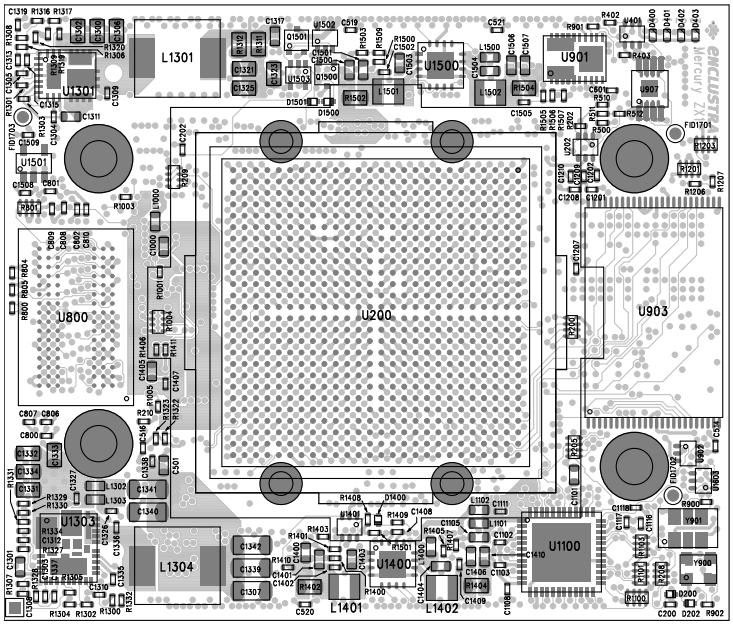

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

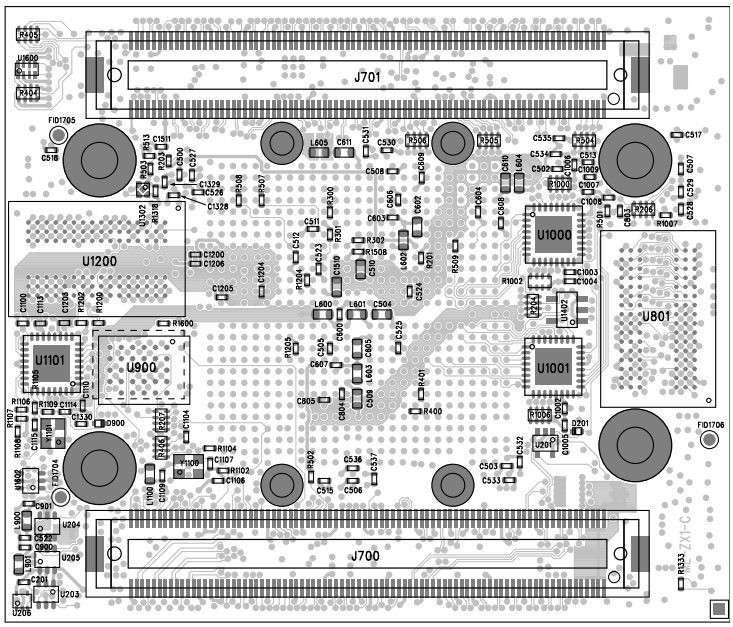

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

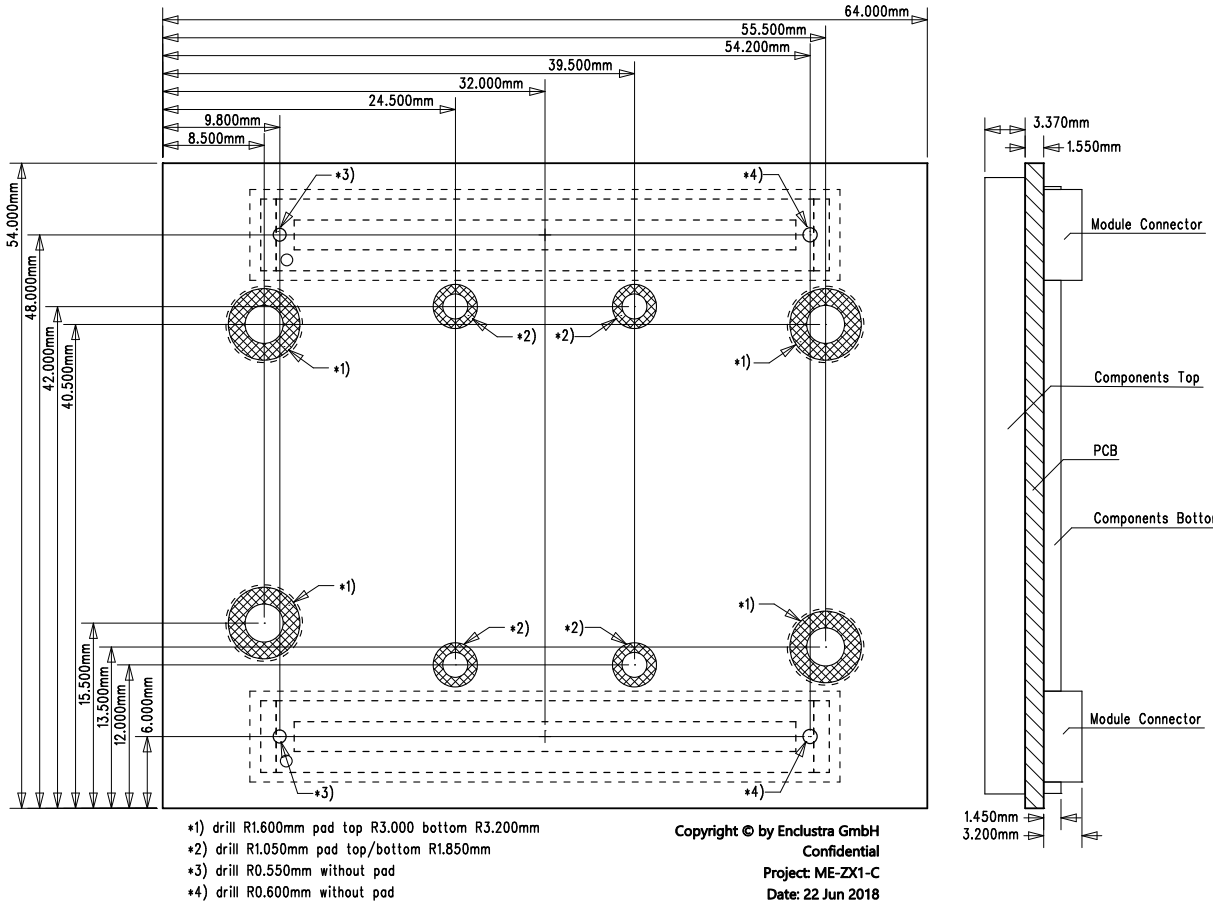

Figure 8: Module Footprint - Top View

Warning!

It is possible to mount the Mercury ZX1 SoC module the wrong way round on the base board - always check that the mounting holes on the base board are aligned with the mounting holes of the Mercury ZX1 SoC module.

2.7 Mechanical Data

Table 4 describes the mechanical characteristics of the Mercury ZX1 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	64 × 54 mm
Component height top	3.37 mm[1]
Component height bottom	1.45 mm
Weight	28 g

Table 4: Mechanical Data

2.8 Module Connector

Two Hirose FX10 168-pin 0.5 mm pitch headers with a total of 336 pins have to be integrated on the base board. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout Excel Sheet [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 5. Please refer to the connector datasheet for more information.

Reference	Type	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 5: Module Connector Types

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J700-1 to J700-168
- Connector B: from J701-1 to J701-168

[1] The component height on top of the module may vary due to different SoC heights for different assembly variants. 3.37 mm covers the maximum height. Please refer to [24] for detailed information.

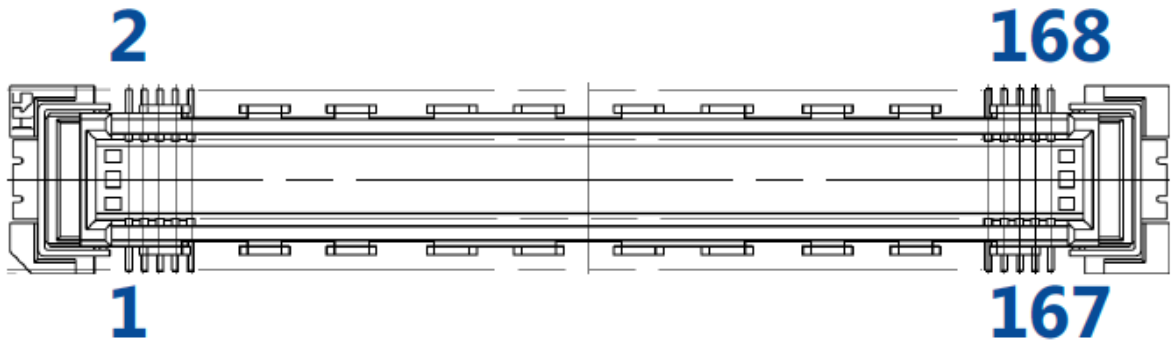

Figure 9: Pin Numbering for the Module Connector

Warning!

Do not use excessive force to latch a Mercury module into the Mercury connectors on the base board, as this could damage the module and the base board; always make sure that the module is correctly oriented before mounting it into the base board.

2.9 User I/O

2.9.1 Pinout

Information on the Mercury ZX1 SoC module pinout can be found in the Enclustra Mercury Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mercury ZX1 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR><_SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B33_L12_MRCC_J3_N is located on pin J3 of I/O bank 33, pair 12, it is an MRCC (Multi-Region Clock Capable) pin and it has negative polarity, when used in a differential pair.

For the signal lines shared between Programmable Logic (PL) and Processing System (PS), the naming convention is:
IO_<MIO_PIN>_<FUNCTION>_B<BANK>_<PACKAGE_PIN>

For example, IO_MIO44_SDD2_B12_AC17 is connected to FPGA pin AC17 and in parallel to the PS MIO pin 44.

Please note that for the shared pins only one of the driving pins (FPGA pin, MIO pin) may be active.

The multi-region clock capable pins are marked with "MRCC", while the single region clock capable pins are marked with "SRCC" in the signal name. For details on their function and usage, please refer to the Xilinx

documentation.

Table 6 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Diff.	Single-ended	I/O Bank	Comments
IO_<MIO_PIN>_<...>_B12_<...>	12	6	In/Out	In/Out	12	Shared between PL and PS
IO_B12_<...>	4	2	In/Out	In/Out	12	
IO_B13_<...>	50	24	In/Out	In/Out	13	
IO_B33_<...>	46	23	In/Out	In/Out	33	Only 36 signals available on XC7Z035/XC7Z045 devices
IO_B34_<...>	38	19	In/Out	In/Out	34	Only 36 signals available on XC7Z035/XC7Z045 devices
Total (XC7Z030)	**150**	**75**	-	-	-	
Total (XC7Z035/XC7Z045)	**138**	**68**	-	-	-	

Table 6: User I/Os

Please note that for the 7 Series FPGAs there are restrictions on the VCCO voltage when using LVDS I/Os; refer to Xilinx AR# 43989 for details.

2.9.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions.

I/O Pins with Different Functions Depending on the Equipped SoC Device

On the Mercury ZX1 SoC modules equipped with bigger SoC devices (XC7Z035/XC7Z045) there are eight MGT transceiver lines and four differential clock inputs available.

On the modules equipped with smaller SoC devices (XC7Z030) there are only four MGT transceiver lines and 2 differential clock inputs available. Instead, the transmission (TX) signals of the upper MGT pairs (pairs 4-7) and two differential clock pairs are rerouted to regular user I/Os from FPGA banks 33 and 34. The receiver (RX) signals of the upper MGT pairs are not connected to any FPGA bank on the smaller module.

Table 7 presents the I/O pin exceptions on the Mercury ZX1 SoC module.

I/O Name	Module Conn. Pin	Description	
		XC7Z030	XC7Z035/XC7Z045
MGT_REFCLK<2-3>_<...> MGT_TX<4-7>_<...>	B-3, 5, 7, 9 B-45, 47, 51, 53, 63, 65, 69, 71	These pins are connected to user I/Os in FPGA banks 33 and 34	These pins are connected to the MGTs in FPGA bank 111
MGT_RX<4-7>_<...>	B-48, 50, 54, 56, 60, 62, 66, 68	These pins are not connected	These pins are connected to the MGTs in FPGA bank 111

Table 7: I/O Pin Exceptions - I/O Pins with Different Functions Depending on the Equipped SoC Device

2.9.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mercury ZX1 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mercury ZX1 SoC module. Please use the information provided in the Mercury ZX1 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

2.9.4 I/O Banks

Table 8 describes the main attributes of the Programmable Logic (PL) and Processing System (PS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
MGT Bank 111 (not available on XC7Z030 device)	Module connector	1.2 V	-
MGT Bank 112	Module connector	1.2 V	-
Bank 0	Configuration	User selectable VCC_CFG_MIO_B12	-
Bank 12	Module connector, Fast Ethernet PHYs, I2C	User selectable VCC_CFG_MIO_B12	-

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
Bank 13	Module connector	User selectable VCC_IO_B13	IO_B13_L6_VREF_AB24_N IO_B13_L19_VREF_Y20_N
Bank 33	Module connector, oscillator	User selectable VCC_IO_B33	IO_B33_L6_VREF_E3_N IO_B33_L19_VREF_L7_N
Bank 34	Module connector, I2C, Fast Ethernet PHYs, LEDs	User selectable VCC_IO_B34	IO_B34_L6_VREF_H8_N IO_B34_L19_VREF_C3_N
Bank 35	DDR3 SDRAM (PL)	User selectable[2] VCC_DDR3	0.5 × VCC_DDR3
PS MIO0	QSPI and NAND flash	User selectable VCC_CFG_MIO_B12	-
PS MIO1	Module connector, USB PHY, Gigabit Ethernet PHY	User selectable VCC_CFG_MIO_B12	0.9 V
PS DDR	DDR3 SDRAM (PS)	User selectable[2] VCC_DDR3	0.5 × VCC_DDR3

Table 8: I/O Banks

2.9.5 VREF Usage

I/O standards referenced using VREF can be used on the Mercury module connector. The reference voltage has to be applied to all VREF pins of the respective I/O banks. If a bank is configured to use an I/O standard that does not need a reference voltage, the VREF pins of this bank on the module connector are available as user I/O pins.

The VREF pins are listed in the Mercury Master Pinout Excel Sheet [11].

Warning!

Use only VREF voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mercury ZX1 SoC module.

Do not leave a VREF pin floating when the used I/O standard requires a reference voltage, as this may damage the equipped SoC device, as well as other devices on the Mercury ZX1 SoC module.

[2] The DDR3 SDRAM supports voltages of 1.5 or 1.35 V. Please refer to Sections 2.15 and 2.16 for details.

2.9.6 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

The high performance (HP) I/O banks 33 and 34 are protected against too high supply voltages. If a voltage higher than 2.2 V is applied to the corresponding supply inputs on the module connector, the supply pins of the SoC device are disconnected, and the device is held in reset.

Signal Name	SoC Pins	Supported Voltages	Connector A Pins	Connector B Pins
VCC_CFG_MIO_B12	VCCO_0, VCC_IO_B12, VCCO_MIO0, VCCO_MIO1	1.8 V[3], 2.5 V - 3.3 V[4] ±5%	74, 77	-
VCC_IO_B13	VCCO_13	1.2 V - 3.3 V ±5%	38, 41	-
VCC_IO_B33	VCCO_33	1.35 V - 1.8 V ±5%	-	67, 95, 143
VCC_IO_B34	VCCO_34	1.35 V[5] - 1.8 V ±5%	-	64, 88, 140

Table 9: VCC_IO Pins

Note that the CFGBVS_0 pin is set automatically to GND (if VCC_CFG_MIO_B12 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_MIO_B12 is 2.5 V or 3.3 V).

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mercury ZX1 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mercury ZX1 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 10 illustrates the VCC_IO power requirements.

[3] NAND flash is disabled when VCC_CFG_MIO_B12 is 1.8 V.
[4] The RGMII Ethernet interface is specified only up to 2.5 V on the MIO pins by Xilinx. Please refer to Section 2.20 for details.
[5] The LEDs may start to glow when VCC_IO_B34 is less than 1.8 V.

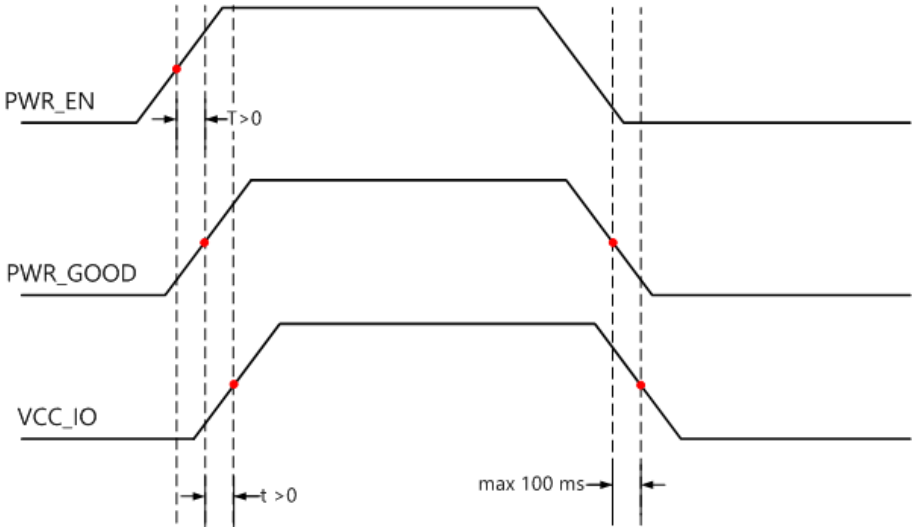

Figure 10: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.7 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mercury ZX1 SoC module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the SoC device's internal termination resistors.

FPGA bank 33 has two pins each equipped with a 100 Ω resistor, required for the implementation of internal termination (DCI - Digitally Controlled Impedance).

Internal differential termination is available only for certain VCCO voltages; please refer to Xilinx AR# 43989 for details.

Single-Ended Outputs

There are no series termination resistors on the Mercury ZX1 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.8 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq-7000 All Programmable SoC Technical Reference Manual [18].

Some of the MIO pins on the Mercury ZX1 SoC module are connected to on-board peripherals, while others are available as GPIOs; the suggested functions below are for reference only - always verify your MIO pinout with the Xilinx device handbook.

Table 11 gives an overview over the MIO pin connections on the Mercury ZX1 SoC module. Only the pins marked with "user functionality" are available on the module connector.

The MIO pins 52-53 have an external multiplexer that allows the pins to be switched either to the Ethernet MDIO interface, or to the on-board I2C bus; by default, MDIO is selected. In order to switch to I2C operation, MIO15 must be pulled low. Please refer to Table 10 for signal assignments.

It is recommended to use EMIO pins for I2C access. However, in situations where Ethernet is not used or when I2C access is needed before a bitstream is loaded into the FPGA, MIO pins 52-53 may be used for I2C.

MIO Pin	Function	
MIO15	MDIO select = 0	MDIO select = 1 (default)
MIO52	On-board I2C bus (I2C1.SCL)	Ethernet PHY MDC
MIO53	On-board I2C bus (I2C1.SDA)	Ethernet PHY MDIO

Table 10: Special MIO Pins

MIO Group	Function	Connection
0-14	QSPI and NAND flash	QSPI/NAND flash
15	MDIO select/LED3# signal	I2C/MDIO multiplexer selection, LED3#
16-27	Ethernet	Gigabit Ethernet PHY
28-39	USB	USB 2.0 OTG PHY
40-45	SD card/user functionality	Module connector
46 47	UART RX[6]/user functionality UART TX[6]/user functionality	Module connector
48-51	User functionality	Module connector
52-53	Ethernet MDIO/I2C	Gigabit Ethernet PHY/ On-board I2C bus and module connector via level shifter

Table 11: MIO Pins Connections Overview

2.10 Multi-Gigabit Transceiver (MGT)

On the Mercury ZX1 SoC modules equipped with bigger SoC devices, there are eight Multi-Gigabit transceivers and four reference input clock differential pairs available on the module connector B.

On the Mercury ZX1 SoC modules equipped with smaller SoC devices, there are only four Multi-Gigabit transceivers and two reference input clock differential pairs available. Instead, on these modules, there are additional regular I/Os routed to the module connector. Please refer to Section 2.9.2 for details on the MGT connections for different SoC devices.

Table 12 lists the available speeds for the MGT lines on the SoC device. Refer to Section 2.2 for details on the module configurations and equipped SoC devices.

[6]UART RX is an SoC input; UART TX is an SoC output.

MGT Speed	SoC Device
4 MGTs @ 6.6 Gbit/sec	Zynq-7030
8 MGTs @ 6.6 Gbit/sec	Zynq-7035
8 MGTs @ 10.3125 Gbit/sec	Zynq-7045

Table 12: MGT Switching Characteristics on the Mercury ZX1 SoC module

Warning!

The maximum data rate on the MGT lines on the Mercury ZX1 SoC module depends on the routing path for these signals. Adequate signal integrity over the full signal path must be ensured when using MGTs at high performance rates.

Warning!

No AC coupling capacitors are placed on the Mercury ZX1 SoC module on the MGT lines - make sure capacitors are mounted, if required, on the base board (close to the module pins), to prevent MGT lines from being damaged.

2.11 Power

2.11.1 Power Generation Overview

The Mercury ZX1 SoC module uses a 5 - 15 V DC power input for generating the on-board supply voltages (1.0 V, 1.2 V, 1.35 V/1.5 V, 1.55 V, 1.8 V, 2.0 V, 2.5 V, 2.9 V and 3.3 V). Some of these voltages (1.8 V, 2.5 V, 3.3 V) are accessible on the module connector.

Table 13 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V0	1.0 V	20 A	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	2 A	VCC_3V3	Yes	Yes
VCC_DDR3	1.35 V/1.5 V	2 A	VCC_3V3	Yes	Yes
VCC_1V8	1.8 V	2 A	VCC_3V3	Yes	Yes
VCC_1V55	1.55 V	2 A	VCC_1V8	Yes	No
VCC_2V0[7]	2.0 V	0.3 A	VCC_2V5	Yes	No
VCC_2V5	2.5 V	2 A	VCC_3V3	Yes	Yes
VCC_2V9	2.9 V	0.2 A	VCC_2V9	Yes	No
VCC_3V3	3.3 V	9 A	VCC_MOD	No	Yes

Table 13: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.11.2 Power Enable/Power Good

The Mercury ZX1 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.0 V, 1.2 V, 1.35 V/1.5 V, 1.8 V, and 2.5 V. The 3.3 V supply is always active.

The PWR_EN input is pulled to VCC_3V3 on the Mercury ZX1 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury ZX1 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.11.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	A-10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A-12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 14: Module Power Status and Control Pins

[7] The 2.0 V LDO is equipped only for SoC devices in FFG packages.

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mercury ZX1 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins (for example by connecting VCC_3V3 to VCC_IO directly) when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 10.

2.11.3 Voltage Supply Inputs

Table 15 describes the power supply inputs on the Mercury ZX1 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.6.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	A-1, 2, 3, 4, 5, 6, 7, 8, 9, 11	5 - 15 V ±5%	Supply for the 1.0 V and 3.3 V voltage regulators. All other supplies are generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A-168	2.0 - 3.6 V	Battery for the RTC and SoC encryption key storage

Table 15: Voltage Supply Inputs

2.11.4 Voltage Supply Outputs

Table 16 presents the supply voltages generated on the Mercury ZX1 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[8]	Comment
VCC_3V3	A-26, 29, 50, 86 B-55, 79, 115, 127, 152, 155	3.3 V ±5%	3 A (and max 0.3 A per pin)	Always active
VCC_2V5	A-53, 62, 65, 89	2.5 V ±5%	1.2 A (and max 0.3 A per pin)	Controlled by PWR_EN
VCC_1V8	B-52, 76, 108, 128	1.8 V ±5%	1.2 A (and max 0.3 A per pin)	Controlled by PWR_EN

Table 16: Voltage Supply Outputs

[8] The maximum available output current depends on your design. See sections 2.11.1 and 2.11.5 for details.

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mercury ZX1 SoC module.

2.11.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

2.11.6 Heat Dissipation

High performance devices like the Xilinx Zynq-7000 SoC need cooling in most applications; always make sure the SoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury ZX1 SoC module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the SoC device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

Table 17 lists the heat sink and thermal pad part numbers that are compatible with the Mercury ZX1 SoC module. Details on the Mercury heatsink kit can be found in the Mercury Heatsink Application Note [17].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury ZX1	FBG676,FFG676 [24]	ACC-HS3-Set	ATS-52270G-C1-R0	TG-A6200-28-28-1

Table 17: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

Warning!

Depending on the user application, the Mercury ZX1 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.11.7 Voltage Monitoring

Several pins on the module connector on the Mercury ZX1 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 18 presents the VMON pins on the Mercury ZX1 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V0	A-102	VCC_INT	PS and PL core voltages
VMON_1V2	B-167	VCC_1V2	1.2 V on-board voltage (default)/SoC battery voltage (assembly option)
VMON_2V9_DIV	B-168	VCC_2V9 on-board voltage divided by 2	NAND flash supply
VMON_DDR3	B-8	VCC_DDR3	DDR3 voltage

Table 18: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.12 Clock Generation

A 33.33 MHz oscillator is used for the Mercury ZX1 SoC module clock generation; the 33.33 MHz clock (CLK_33) is fed to the PS via PS_CLK pin. This clock is not connected directly to any clock pin of the FPGA fabric.

A 200 MHz LVDS oscillator is connected to FPGA bank 33 (pins L4 and L5). The signal is terminated with a 100 Ω parallel resistor close to the FPGA pins.

2.13 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the SoC device are available on the module connector.

Pulling PS_POR# low resets the SoC device, the Ethernet and the USB PHYs, and the flash devices. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the SoC device. For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq-7000 Technical Reference Manual [18].

Table 19 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 10 kΩ pull-up resistors to VCC_CFG_MIO_B12.

Signal Name	Module Connector Pin	FPGA Pin Type	Description
PS_POR#	A-132	PS_POR_B	Power-on reset
PS_SRST#	A-124	PS_SRST_B	System reset

Table 19: Reset Resources

Please note that PS_POR# is automatically asserted if PWR_GOOD is low.

2.14 LEDs

There are four active-low LEDs on the Mercury ZX1 SoC module. LEDs 0-2 are connected to the FPGA logic and LED3 is connected to the pin MIO15 of the PS.

Signal Name	FPGA/PS Pin	Remarks
FPGA_LED0#	H7	User function/active-low
FPGA_LED1#	H6	User function/active-low
FPGA_LED2#	H9	User function/active-low
MDIO_SEL_LED3#	MIO15	User function/active-low; shared with MDIO select signal

Table 20: LEDs

Note that MIO15 is a dual-function pin and by changing the value of this signal, the MDIO/I2C selection circuit is also affected - please refer to Section 2.9.8 for details on the usage of this pin.

2.15 DDR3 SDRAM (PS)

There are two DDR3 SDRAM channels on the Mercury ZX1 SoC module: one attached directly to the PS side (which is available only as a shared resource to the PL side) and one attached directly to the PL side.

The DDR3 SDRAM connected to the PS is operated at 1.35 V (low power mode) or at 1.5 V, depending on a selection signal. Two 16-bit memory chips are used to build a 32-bit wide memory.

The maximum memory bandwidth on the Mercury ZX1 SoC module for the DDR3 SDRAM (PS) is:
1066 Mbit/sec × 32 bit = 4264 MB/sec

2.15.1 DDR3 SDRAM Type

Table 21 describes the memory availability and configuration on the Mercury ZX1 SoC module.

Module	SDRAM Type	Density	Configuration	Manufacturer
ME-ZX1-D10 (commercial)	NT5CC256M16CP-DI	4 Gbit	256 M × 16 bit	Nanya
ME-ZX1-D10 (industrial)	NT5CC256M16CP-DII	4 Gbit	256 M × 16 bit	Nanya
ME-ZX1-D10 (industrial)	NT5CC256M16ER-EKI	4 Gbit	256 M × 16 bit	Nanya
ME-ZX1-D10 (industrial)	K4B4G1646D-BMK0	4 Gbit	256 M × 16 bit	Samsung
ME-ZX1-D10 (industrial)	K4B4G1646E-BMMA	4 Gbit	256 M × 16 bit	Samsung
ME-ZX1-D10 (industrial)	H5TC4G63CFR-RDI	4 Gbit	256 M × 16 bit	SK Hynix

Table 21: DDR3 SDRAM (PS) Types

Warning!

Other DDR3 memory devices may be equipped in future revisions of the Mercury ZX1 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

Please refer to the Mercury ZX1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3 SDRAM connections.

2.15.3 Termination

Warning!

No external termination is implemented on the Mercury ZX1 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.15.4 Parameters

Please refer to the Mercury ZX1 SoC module reference design [2] for DDR3 settings guidelines. The DDR3 SDRAM parameters and the DDR3 board timing information to be set in Vivado project are presented in Tables 22 and 23.

The values given in Table 22 are for reference only. Depending on the equipped memory device on the Mercury ZX1 SoC module and on the DDR3 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR3/DDR3L
DRAM bus width	32 bit
Operating frequency	200-533 MHz
DRAM chip bus width	16 bit
DRAM chip capacity	4096 Mbits
Speed bin	DDR3_1066F
Bank bits	3
Row bits	15
Column bits	10
CAS latency	7
CAS write latency	6
RAS to CAS delay	7
Precharge time	7
tRC	50.625 ns
tRASmin	37.5 ns
tFAW	40.0 ns

Table 22: DDR3 SDRAM (PS) Parameters

Parameter	Byte 3	Byte 2	Byte 1	Byte 0
DQS to clock delay (ns)	0.061	0.043	0.000	-0.032
Board delay (ns)	0.243	0.255	0.272	0.285

Table 23: DDR3 (PS) Board Timing

2.15.5 DDR3 Low Voltage Operation

The default voltage of the DDR3 is 1.5 V. In order to enable low voltage mode (1.35 V), DDR3_VSEL (pin AD10) must be driven logic 0, DDR3L memory type must be selected in the PS configuration parameters and a memory voltage of 1.35 V must be selected in the Memory Interface Generator (MIG) parameters in Vivado.

For 1.5 V operation, DDR3_VSEL must be set to high impedance (not driven logic 1).

Note that the configuration for the DDR3_VSEL pin affects both memory channels (DDR3 SDRAM PS and PL).

On Mercury ZX1 SoC modules revision 1 the Fast Ethernet ports are not enabled when DDR3 SDRAM is operated in low power mode. This is because the Ethernet ports are fed by the same supply as the DDR3 memory and require a voltage of 1.5 V to work properly. This issue has been fixed for modules from revision 2 and newer.

2.16 DDR3 SDRAM (PL)

The DDR3 SDRAM connected to the PL on the Mercury ZX1 SoC module is operated at 1.35 V (low power mode) or at 1.5 V, depending on a selection signal. The DDR bus width is 16-bit.

The DDR3 SDRAM memory connected to the PL supports different bandwidths depending on the equipped SoC device:

- FBG package, speedgrade 1: up to 800 Mbit/s (400 MHz)
- FBG package, speedgrade 2: up to 1066 Mbit/s (533 MHz)
- FFG package, speedgrade 1 and 2: up to 1600 Mbit/s (800 MHz)

Hence, the maximum memory bandwidth on the Mercury ZX1 SoC module for the DDR3 SDRAM (PL) is:

- FBG package, speedgrade 1: 800 Mbit/s × 16 bit = 1600 MB/sec
- FBG package, speedgrade 2: 1066 Mbit/s × 16 bit = 2133 MB/sec
- FFG package, speedgrade 1 and 2: 1600 Mbit/s × 16 bit = 3200 MB/sec

For DDR3 low power mode (DDR3L) the speed can be lower than mentioned above. Details are available in the Zynq DC and AC Switching Characteristics document [23].

2.16.1 DDR3 SDRAM Type

Table 24 describes the memory availability and configuration on the Mercury ZX1 SoC module.

Module	SDRAM Type	Density	Configuration	Manufacturer
ME-ZX1-D10 (commercial)	NT5CC256M16CP-DI	4 Gbit	256 M × 16 bit	Nanya
ME-ZX1-D10 (industrial)	NT5CC256M16CP-DII	4 Gbit	256 M × 16 bit	Nanya
ME-ZX1-D10 (industrial)	NT5CC256M16ER-EKI	4 Gbit	256 M × 16 bit	Nanya
ME-ZX1-D10 (industrial)	K4B4G1646D-BMK0	4 Gbit	256 M × 16 bit	Samsung
ME-ZX1-D10 (industrial)	K4B4G1646E-BMMA	4 Gbit	256 M × 16 bit	Samsung
ME-ZX1-D10 (industrial)	H5TC4G63CFR-RDI	4 Gbit	256 M × 16 bit	SK Hynix

Table 24: DDR3 SDRAM (PL) Types

Warning!

Other DDR3 memory devices may be equipped in future revisions of the Mercury ZX1 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

Please note that although 4 Gbit memories are used, only 2 Gbits (256 MB) are available, because the most significant address bit is not mapped to the FPGA pins (due to the limited number of FPGA I/Os).

2.16.2 Signal Description

Please refer to the Mercury ZX1 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3 SDRAM connections.

2.16.3 Termination

Warning!

No external termination is implemented on the Mercury ZX1 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.16.4 Parameters

Please refer to the Mercury ZX1 SoC module reference design [2] for DDR3 settings guidelines. The DDR3 SDRAM parameters to be set in Vivado project are presented in Table 25.

The values given in Table 25 are for reference only. Depending on the equipped memory device on the Mercury ZX1 SoC module and on the DDR3 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory voltage	1.5 V (for DDR3)/1.35 V (for DDR3L)
Data width	16 bit
Clock period	1250 - 3300 ps
Bank address bits	3
Row address bits	14
Column address bits	10
trefi	7.8 us
trfc	260 ns
tras	37.5 ns
trp	15 ns
trcd	15 ns

Table 25: DDR3 SDRAM (PL) Parameters

2.16.5 DDR3 Low Voltage Operation

Please refer to Section 2.15.5 for details on the DDR3 low power mode.

2.17 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.17.1 QSPI Flash Type

Table 26 describes the memory availability and configuration on the Mercury ZX1 SoC module.

As there is one QSPI flash chip equipped on the Mercury ZX1 SoC module, type "single" must be selected when programming the flash from Vivado tools.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 26: QSPI Flash Types

Warning!

Other flash memory devices may be equipped in future revisions of the Mercury ZX1 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.17.2 Signal Description

The QSPI flash is connected to the PS MIO pins 1-6. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Note that MIO pins 2-6 pins are shared between NAND flash and QSPI flash on the Mercury ZX1 SoC module, therefore only of the two memories may be used at once. However, it is possible to switch between them at runtime.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. These signals are shared with the NAND flash and have to be high impedance during normal operation.

Long traces or high capacitance may disturb the data communication between the SoC and the flash devices.

2.17.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, please refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO8 must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

24-bit Address Compatibility Mode

If the Zynq device boots from the QSPI flash and the 24-bit address compatibility mode of the QSPI flash is used to access the range above 16 MB, then the compatibility mode must be disabled before a system reset is executed. Otherwise, the Zynq device will not be able to boot from the QSPI flash again, as the address

register is not pointing to the lower addressed part of the memory, in which the boot image is located.

The reset of the QSPI flash is connected to the PS_POR# power-on reset signal in order to avoid this issue after a power-on reset. The PS_SRST# signal should not be used in this setup.

Please refer to Zynq-7000 Technical Reference Manual [18] for details on booting from the QSPI flash.

2.17.4 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [26], [27].

2.18 NAND Flash

The NAND flash can be used to boot the PS, to store the FPGA bitstream, ARM application code and other user data. Refer to Section 3.3 for details on available boot modes.

The NAND flash is disabled when VCC_CFG_MIO_B12 is 1.8 V. The NAND_ENABLE signal, which controls the CE# and WP# pins of the NAND flash, is set automatically to GND (if VCC_CFG_MIO_B12 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_MIO_B12 is 2.5 V or 3.3 V).

2.18.1 NAND Flash Type

Table 27 describes the memory availability and configuration on the Mercury ZX1 SoC module.

Flash Type	Size	Manufacturer
MT29F4G08ABADAWP	4 Gbit	Micron

Table 27: NAND Flash Type

2.18.2 Signal Description

The NAND flash is connected to the PS MIO pins 0, 2-14. The MIO pins 2-6 are shared between the QSPI and NAND flash.

2.18.3 Parameters

Please refer to the NAND flash memory device datasheet to extract the required parameter values. Reference values to be used in Vivado are given in Table 28.

The indicated parameter values may be used for booting from NAND flash memory on the Mercury ZX1 SoC module.

Nand Cycle Parameter	CS0	CS0 Cycles	Description
T_RC	30	4	Read cycle time
T_WC	30	4	Write cycle time
T_REA	0	1	RE assertion delay
T_WP	20	3	WE deassertion delay
T_CLR	20	3	Page cycle time
T_AR	20	3	ID read time
T_RR	30	4	Busy to RE

Table 28: NAND Flash Parameters

2.19 SD Card

An SD card can be connected to the PS MIO pins 40-45 or 46-51, or alternatively via EMIO pins to the PL.

The corresponding MIO pins are available on the module connector. Note that only MIO pins 40-45 allow the Mercury ZX1 SoC module to boot from the SD card. Information on this boot mode is available in Section 3.6.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_MIO_B12, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

2.20 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mercury ZX1 SoC module, connected to the PS on MIO pins 16-27.

Please note that Xilinx recommends operation at 1.8 V/2.5 V for the RGMII interface for the MIO pins [18]. Enclustra tests have shown that the RGMII is functional with a 3.3 V I/O voltage on the MIO pins, as long as the I/O voltage configured in Vivado matches the applied I/O voltage.

2.20.1 Ethernet PHY Type

Table 29 describes the equipped Ethernet PHY device type on the Mercury ZX1 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 29: Gigabit Ethernet PHY Type

2.20.2 Signal Description

The RGMII interface is connected to MIO pins 16-27 for use with the hard macro MAC. The interrupt output of the Ethernet PHY is connected to an FPGA pin (K11).

The Gigabit Ethernet connections are presented in Table 30. All listed pins are operated at VCC_CFG_MIO_B12 I/O voltage.

Signal Name	MIO Pin	PL Pin
ETH_RST#	PS_POR#	
ETH0_INT#	-	K11
ETH_MDC	MIO52[9]	-
ETH_MDIO	MIO53[9]	-
ETH_RXC	MIO22	-
ETH_RX_CTL	MIO27	-
ETH_RXD0	MIO23	-
ETH_RXD1	MIO24	-
ETH_RXD2	MIO25	-
ETH_RXD3	MIO26	-
ETH_TXC	MIO16	-
ETH_TX_CTL	MIO21	-
ETH_TXD0	MIO17	-
ETH_TXD1	MIO18	-
ETH_TXD2	MIO19	-
ETH_TXD3	MIO20	-

Table 30: Gigabit Ethernet Signal Description

2.20.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.20.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3.

The MDIO interface is connected by default to MIO pins 52-53. These pins can also be used to access the I2C bus - for details, please refer to Section 2.9.8.

2.20.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 31.

Please note that the RGMII delays in the Ethernet PHY need to be configured before the Ethernet interface can be used. This is done in the source files within the First Stage Boot Loader (FSBL) application provided in the Mercury ZX1 SoC module reference design [2].

[9] MIO52 and MIO53 can be used for either MDIO or I2C. Please refer to Section 2.9.8 for details.

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 31: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.21 Dual Fast Ethernet

There are two 10/100 Mbit Ethernet PHYs equipped on the Mercury ZX1 SoC module, connected to FPGA I/Os via MII interface.

On Mercury ZX1 SoC modules revision 1 the Fast Ethernet ports are not enabled when DDR3 SDRAM is operated in low power mode. This is because the Ethernet ports are fed by the same supply as the DDR3 memory and require a voltage of 1.5 V to work properly. This issue has been fixed for modules from revision 2 and newer.

2.21.1 Ethernet PHY Type

Table 32 describes the equipped Ethernet PHY device type on the Mercury ZX1 SoC module.

PHY Type	Manufacturer	Type
TLK105LRHBR	Texas Instruments	10/100 Mbit

Table 32: Fast Ethernet PHY Type

2.21.2 Signal Description

The MII interfaces are connected to the FPGA pins in banks 12 and 34 for use with soft Ethernet MAC IP cores. The signals connected to I/O bank 34 have 4.7 kΩ series resistors as protection if low I/O voltages are used. The two Fast Ethernet PHYs have a shared MDIO interface and a shared interrupt line. Details on connections are available in the Mercury ZX1 SoC Module User Schematics [5] and in the FPGA Pinout Excel Sheet [4].

The 25 MHz clock for the Fast Ethernet must be supplied via FPGA pin W14.

Some of the MII signals have pull-up or pull-down resistors for bootstrapping. Make sure all FPGA internal resistors are disabled.

The reset signal of the Fast Ethernet PHYs has a pull-down resistor and is connected to FPGA pin AF14. It needs to be driven high to release the PHYs from reset.

2.21.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.21.4 MDIO Address

The MDIO address assigned to the Fast Ethernet PHY A is 1, while the address assigned to PHY B is 2.

2.21.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the MII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 33.

Pin	Signal Value	Description
MII_MODE	0	MII mode
PHYAD[4-0]	00001 00010	PHY0: MDIO address 1 PHY1: MDIO address 2
LED_CFG	1	LED mode 1 (Link LED)
AMDIX_EN	1	Auto MDI-X enabled
AN_0	1	Auto-negotiation enabled

Table 33: Fast Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.22 USB 2.0

The Mercury ZX1 SoC module has an on-board USB 2.0 PHY connected to the SoC device. The USB interface can be configured for USB host, USB device and USB On-The-Go (host and device capable) operations.

2.22.1 USB PHY Type

Table 34 describes the equipped USB PHY device type on the Mercury ZX1 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 34: USB 2.0 PHY Type

2.22.2 Signal Description

The ULPI interface is connected to MIO pins 28-39 for use with the integrated USB controller.

2.23 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. The RTC features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus on the Mercury ZX1 SoC module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

Note that the frequency output mode of the RTC must be disabled when using I2C interrupt system. Otherwise, I2C_INT# is periodically pulled down by the RTC. The disabling of this function can be done by setting bits [3:0] of the RTC register 8 to logic low.

2.23.1 RTC Type

Table 35 describes the equipped RTC device type on the Mercury ZX1 SoC module.

Type	Manufacturer
ISL12020M	Intersil

Table 35: RTC Type

An example demonstrating how to use the RTC is included in the Mercury ZX1 SoC module reference design [2].

2.24 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.24.1 EEPROM Type

Table 36 describes the equipped EEPROM device type on the Mercury ZX1 SoC module.

Module	Type	Manufacturer
ME-ZX1 - R1	DS28CN01	Maxim
ME-ZX1 - R2 and newer	ATSHA204A-MAHDA-T (default)	Atmel
ME-ZX1 - R2 and newer	DS28CN01 (assembly option)	Maxim

Table 36: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mercury ZX1 SoC module reference design [2].

3 Device Configuration

3.1 Configuration Signals

The PS of the SoC needs to be configured before the FPGA logic can be used. Xilinx Zynq devices need special boot images to boot from QSPI flash or SD card. For more information, please refer to the Xilinx Zynq-7000: Concepts, Tools, and Techniques document [20].

Table 37 describes the most important configuration pins and their location on the module connector. These signals allow the SoC to boot from QSPI flash or SD card, and can be used to program the QSPI flash from an external master. Please refer to Section 3.9 for details.

Signal Name	SoC Pin Type	Mod. Conn. Pin	Description	Comments
FLASH_CLK	MIO6	A-118	SPI CLK	20 kΩ pull-down
FLASH_DO	MIO3	A-122	SPI MISO	20 kΩ pull-down
FLASH_DI	MIO2	A-114	SPI MOSI	20 kΩ pull-down
FLASH_CS#	MIO1	A-116	SPI CS#	10 kΩ pull-up to VCC_CFG_MIO_B12
FPGA_DONE	DONE_0	A-130	FPGA configuration done	1 kΩ pull-up to VCC_CFG_MIO_B12
FPGA_CFGBVS	CFGBVS_0	-	Configuration bank voltage select[10]	10 kΩ pull-up to VCC_CFG_MIO_B12
PS_POR#	PS_POR_B	A-132	Must be pulled to GND for a short period before QSPI flash programming. PS_SRST# must be low when PS_POR# is released.	10 kΩ pull-up to VCC_CFG_MIO_B12
PS_SRST#	PS_SRST_B	A-124	Must be pulled to GND during QSPI flash programming. When released, all other pins of the SPI interface must be high impedance.	10 kΩ pull-up to VCC_CFG_MIO_B12
BOOT_MODE0	-	A-126	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO_B12

Continued on next page...

[10] The CFGBVS_0 pin is set automatically to GND (if VCC_CFG_MIO_B12 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_MIO_B12 is 2.5 V or 3.3 V).

Signal Name	SoC Pin Type	Mod. Conn. Pin	Description	Comments
BOOT_MODE1	-	A-112	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO_B12

Table 37: SoC Configuration Pins

Warning!

All configuration signals except for BOOT_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped SoC device, as well as other devices on the Mercury ZX1 SoC module.

3.2 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to ground via a 1 kΩ resistor during FPGA configuration, and connected to an FPGA signal after this process is done.

As PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires that all FPGA I/Os have the internal pull-up resistors disabled during device configuration, this can be achieved by removing R202 component and by mounting R203 - in this configuration the PUDC pin is connected to VCC_IO_B34.

Figure 11 illustrates the configuration of the I/O signals during power-up. Figure 12 indicates the location of the pull-up/pull-down resistors on the module PCB - upper right part on the top view drawing and upper left part on the bottom view drawing.

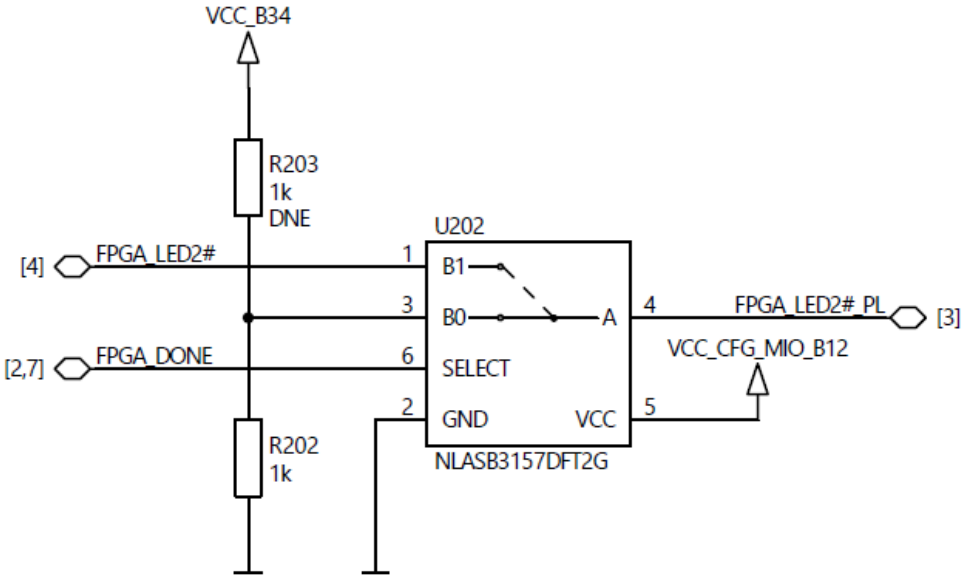

Figure 11: Pull-Up During Configuration (PUDC)

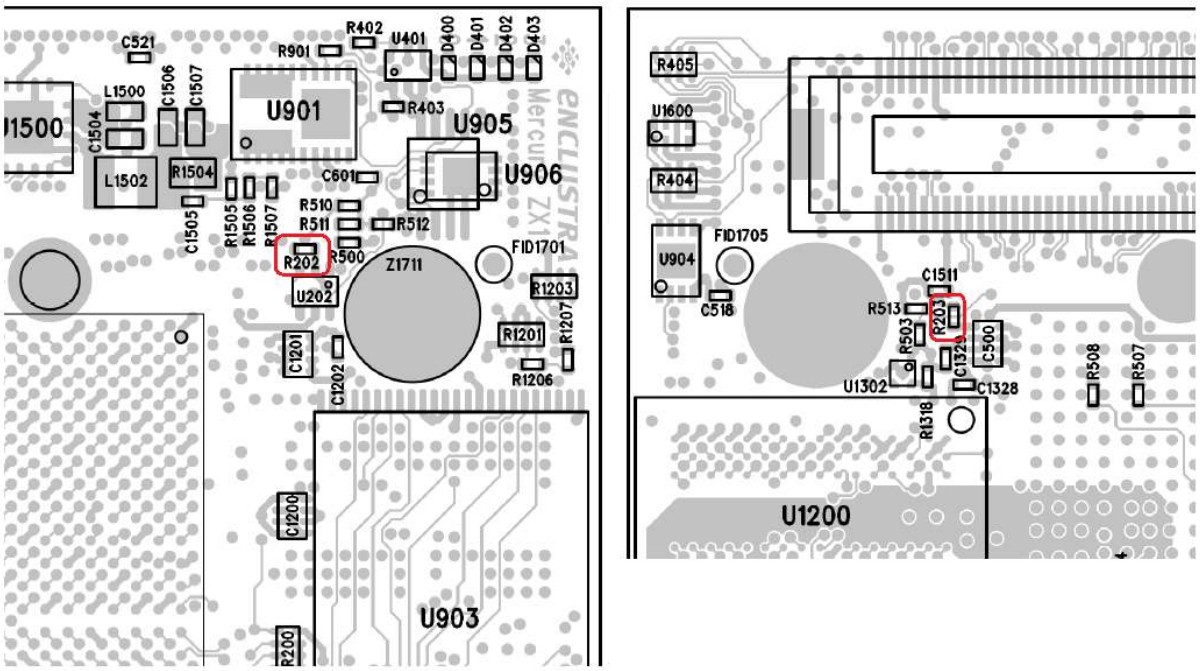

Figure 12: Pull-Up During Configuration (PUDC) Resistors - Assembly Drawing Top and Bottom View (upper right and upper left corners) for Revision 2 Modules

For details on the PUDC signal please refer to the Zynq-7000 All Programmable SoC Technical Reference Manual [18].

3.3 Boot Mode

The boot mode can be selected via two signals available on the module connector.

Table 38 describes the available boot modes on the Mercury ZX1 SoC module.

BOOT_MODE1	BOOT_MODE0	Description
0	0	JTAG boot mode
0	1	Boot from NAND flash
1	0	Boot from QSPI flash
1	1	Boot from SD card

Table 38: Boot Modes

3.4 JTAG

The FPGA and the PS JTAG interfaces are connected into one single chain available on the module connector. The SoC device, the QSPI flash, and the NAND flash can be configured via JTAG from Xilinx SDK or Xilinx Vivado Hardware Manager.

3.4.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	A-123	10 kΩ pull-up to VCC_CFG_MIO_B12
JTAG_TMS	A-119	SoC internal pull-up
JTAG_TDI	A-117	SoC internal pull-up
JTAG_TDO	A-121	-

Table 39: JTAG Interface

3.4.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_MIO_B12.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.5 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 1-6.

In order to boot from the QSPI flash, the user must enable the QSPI flash controller in the Vivado block design and generate a new FSBL to be used for the Zynq boot image creation.

3.6 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board.

For this operation, the following requirements must be met:

- The SD card must be connected to MIO pins 40-45
- A Zynq boot image must be generated from an SoC design having the SDIO controller enabled
- The boot image must be named "boot.bin" and then copied to the SD card
- In software versions older than Vivado 2014.4, the card detect check in the Xilinx FSBL must be disabled. For details, please contact Enclustra Support team.
- The SDIO controller must be fed with a reasonable clock frequency. Please refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, please refer to the Xilinx Zynq documentation [18] [20].

3.7 NAND Boot Mode

In the NAND boot mode, the PS boots from the NAND flash located on the module. The flash device is connected to the PS MIO pins 0 and 2-14.

In order to boot from the NAND flash, the user must enable the NAND controller in the Vivado block design and set the timing parameters as described in Section 2.18.3. After these changes, a new FSBL must be generated and used for the Zynq boot image creation.

3.8 QSPI Flash Programming via JTAG

The Xilinx Vivado and SDK software offer QSPI flash programming support via JTAG. For more information, please refer to the Xilinx documentation [22].

3.9 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the PS_SRST# signal to GND followed by a pulse on PS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Figure 13 shows the signal diagrams corresponding to flash programming from an external master.

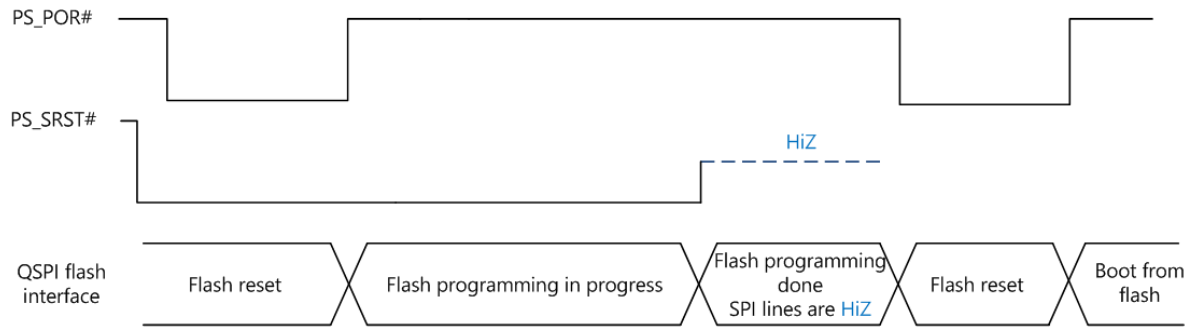

Figure 13: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mercury ZX1 SoC module.

3.10 NAND Flash Programming

The Xilinx SDK software offers NAND flash programming support via JTAG. For the programming operation, type "nand_8" must be selected. Please note that Vivado Hardware Manager does not support the NAND flash type equipped on the Mercury ZX1 SoC module.

When programming the NAND flash in u-boot, the user must make sure that the NAND controller is enabled; the u-boot available in the Enclustra Linux build environment includes a built-in command to switch the current configuration to use NAND flash as storage:

```
zx_set_storage NAND
```

Note that for a successful programming the flash image must be written avoiding the bad sectors of the flash (by using nand.jffs2 command).

3.11 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using the Enclustra Module Configuration Tool (MCT) [16].

Please note that the Xilinx Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mercury ZX1 SoC module.

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury ZX1 SoC module is connected to the SoC device, EEPROM and RTC, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

Please note that the RTC must be configured correctly to use I2C interrupts - for details, refer to Section 2.23.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 40 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the SoC and must not be driven from the SoC device.

Level shifters are used between the I2C bus and the PS/PL pins, to allow I/O voltages lower than 3.3 V. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Pin	Connector Pin	Resistor
I2C_SDA	MIO53[11]	Y13	A-113	2.2 kΩ pull-up
I2C_SCL	MIO52[11]	W13	A-111	2.2 kΩ pull-up
I2C_INT#	-	K10	A-115	10 kΩ pull-up

Table 40: I2C Signal Description

4.3 I2C Address Map

Table 41 describes the addresses for several devices connected on I2C bus.

[11] MIO52 and MIO53 are used for MDIO by default. Please refer to Section 2.9.8 for details.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.24)
0x57	RTC user SRAM
0x6F	RTC registers

Table 41: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury ZX1 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 42: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mercury ZX1 SoC module	0x0327	0x[XX]	0x[YY]	0x0327 [XX][YY]

Table 43: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC type	0	2	See SoC type table (Table 45)
	3-0	SoC device speed grade	1	3	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low power)	
	5-4	Gigabit Ethernet port count	0	1	
	3-2	Fast Ethernet port count	0	2	
	1	RTC equipped	0	1	
	0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR3 RAM (PS) size (MB)	0 (0 MB)	8 (1 GB)	Resolution = 8 MB
	3-0	DDR3 RAM (PL) size (MB)	0 (0 MB)	6 (256 MB)	Resolution = 8 MB
0x0C	7-4	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
	3-0	NAND flash memory size (MB)	0 (0 MB)	7 (512 MB)	Resolution = 8 MB

Table 44: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 45 shows the available SoC types.

Value	SoC Device Type
0	XC7Z030, FBG package
1	XC7Z035, FBG package
2	XC7Z045, FFG package

Table 45: SoC Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

If all three Ethernet interfaces shall be used, the user must provide the third MAC address; the first two addresses are already provided by Enclustra.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 46 indicates the absolute maximum ratings for Mercury ZX1 SoC module. The values given are for reference only; for details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [23].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 16	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_B13 VCC_CFG_MIO_B12	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
VCC_IO_B33/34	Output drivers supply voltage relative to GND	-0.5 to 2.0	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 46: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 47 indicates the recommended operating conditions for Mercury ZX1 SoC module. The values given are for reference only; for details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [23].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	4.75 to 15.75	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.6	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 47: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

List of Tables

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