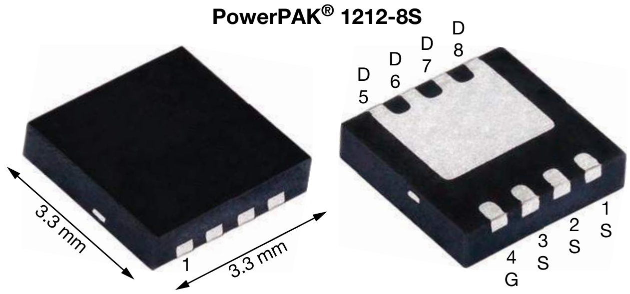
N-Channel 20 V (D-S) MOSFET

PowerPAK® 1212-8S



Top View   Bottom View

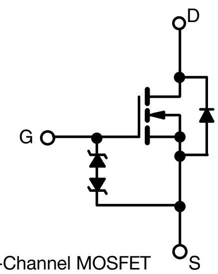
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Low thermal resistance PowerPAK package with small size and 0.75 mm profile
- Typical ESD performance 3400 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Battery switch / load switch
- Power management for tablet PCs and mobile computing



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0039
$R_{DS(on)}$ max. (Ω) at V_{GS} = 3.7 V	0.0042
$R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.0058
Q_g typ. (nC)	22.5
I_D (A)	50 [f, g]
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiS612EDNT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	50 [g]	A
	T_C = 70 °C		50 [g]	
	T_A = 25 °C		24.6 [a, b]	
	T_A = 70 °C		19.7 [a, b]	
Pulsed drain current (t = 100 μs)		I_{DM}	200	
Continuous source-drain diode current	T_C = 25 °C	I_S	43.3	
	T_A = 25 °C		3.1 [a, b]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	20	
Single pulse avalanche energy		E_{AS}	20	mJ
Maximum power dissipation	T_C = 25 °C	P_D	52	W
	T_C = 70 °C		33	
	T_A = 25 °C		3.7 [a, b]	
	T_A = 70 °C		2.4 [a, b]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c, d]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a, e]	t ≤ 10 s	R_{thJA}	24	33	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.9	2.4	

Notes

a. Surface mounted on 1" x 1" FR4 board
b. t = 10 s
c. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
e. Maximum under steady state conditions is 81 °C/W
f. Based on T_C = 25 °C
g. Package limited

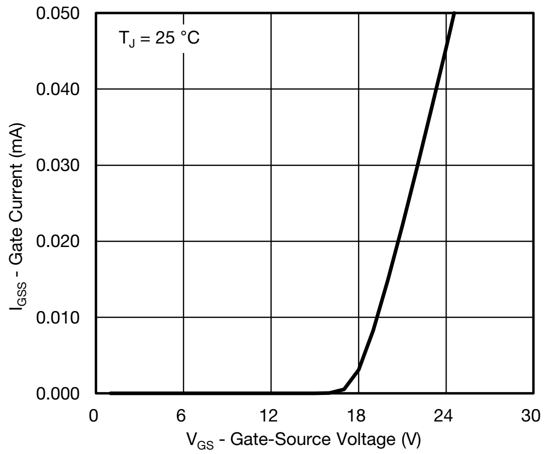
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	20	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	-	18	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-3.5	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	0.5	-	1.2	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 10	μA
		V_{DS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 1	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	-	-	1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 14 A	-	0.0032	0.0039	Ω
		V_{GS} = 3.7 V, I_D = 14 A	-	0.0035	0.0042	
		V_{GS} = 2.5 V, I_D = 13 A	-	0.0041	0.0058	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 14 A	-	50	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	-	2060	-	pF
Output capacitance	C_{oss}		-	558	-	
Reverse transfer capacitance	C_{rss}		-	365	-	
Total gate charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 20 A	-	46	70	nC
		V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 20 A	-	22.5	34	
Gate-source charge	Q_{gs}		-	4.1	-	
Gate-drain charge	Q_{gd}		-	5.3	-	
Gate resistance	R_g	f = 1 MHz	0.2	1	2	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1 Ω I_D ≅ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	16	24	ns
Rise time	t_r		-	65	98	
Turn-off delay time	$t_{d(off)}$		-	40	60	
Fall time	t_f		-	12	20	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 1 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	-	9	18	
Rise time	t_r		-	5	10	
Turn-off delay time	$t_{d(off)}$		-	34	51	
Fall time	t_f		-	4	8	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	50	A
Pulse diode forward current (t = 100 μs)	I_{SM}		-	-	200	
Body diode voltage	V_{SD}	I_S = 10 A, V_{GS} = 0 V	-	0.75	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 10 A, di/dt = 100 A/μs, T_J = 25 °C	-	22	44	ns
Body diode reverse recovery charge	Q_{rr}		-	10	20	nC
Reverse recovery fall time	t_a		-	11	-	ns
Reverse recovery rise time	t_b		-	11	-	

Notes

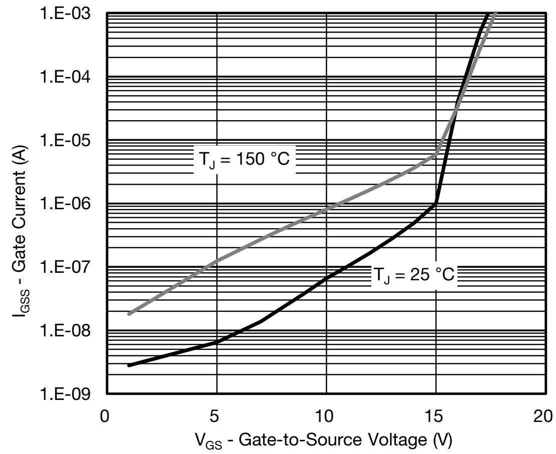
a. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

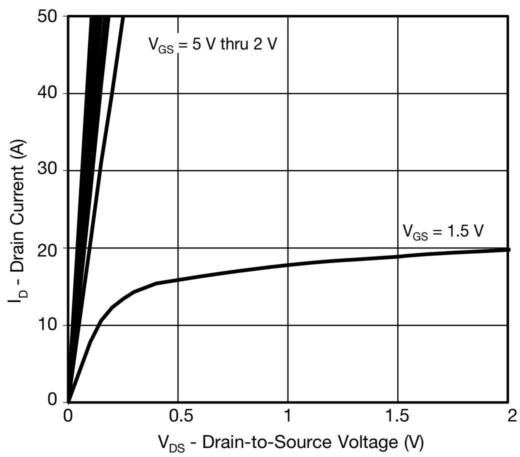
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



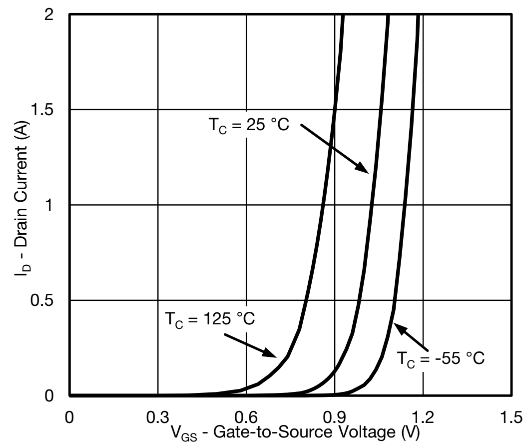
Gate Current vs. Gate-to-Source Voltage



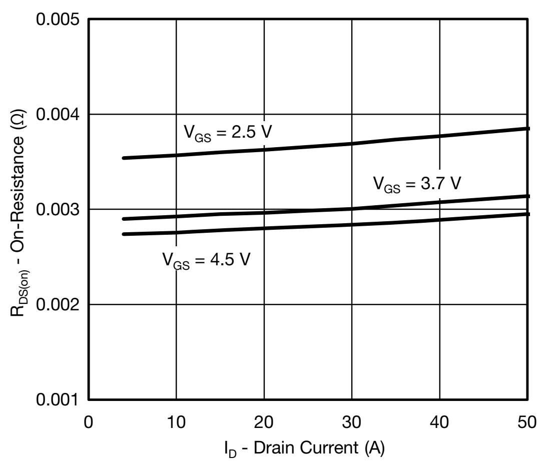
Gate Current vs. Gate-to-Source Voltage



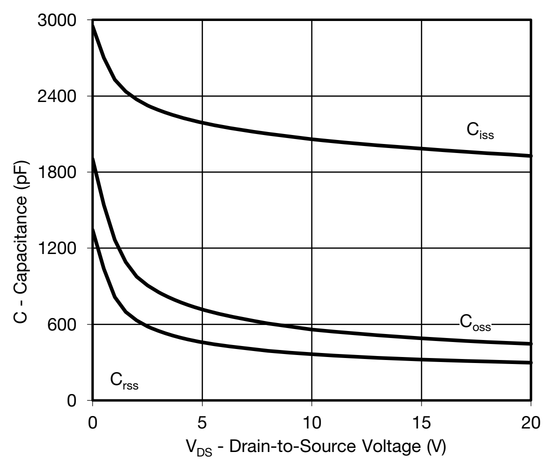
Output Characteristics



Transfer Characteristics

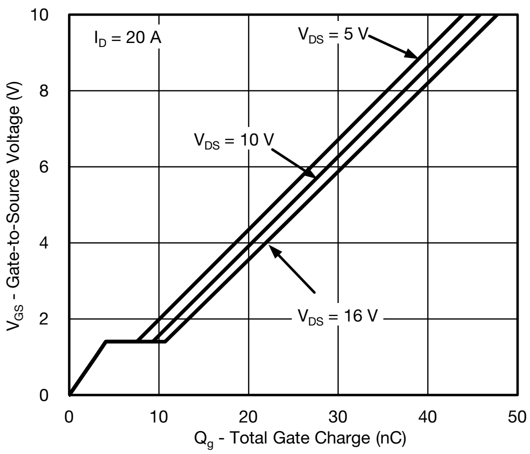


On-Resistance vs. Drain Current and Gate Voltage

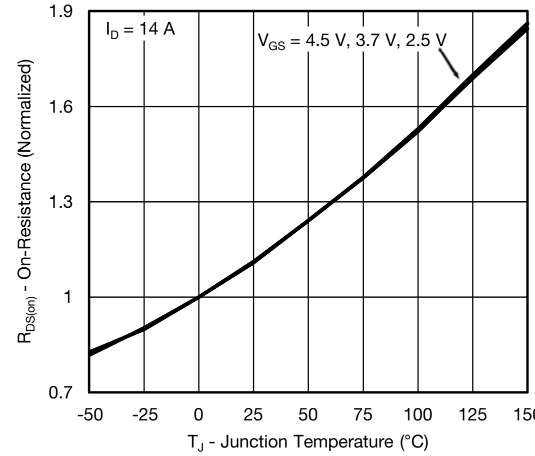


Capacitance

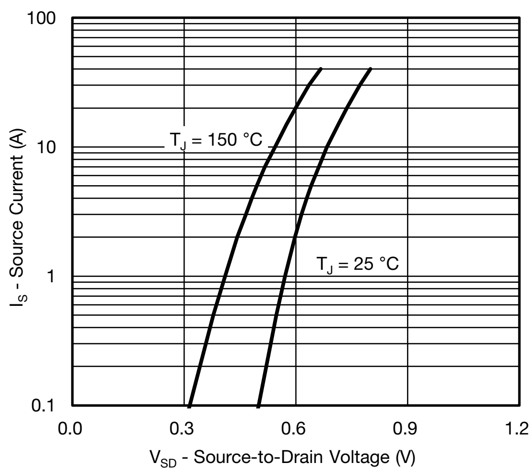
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



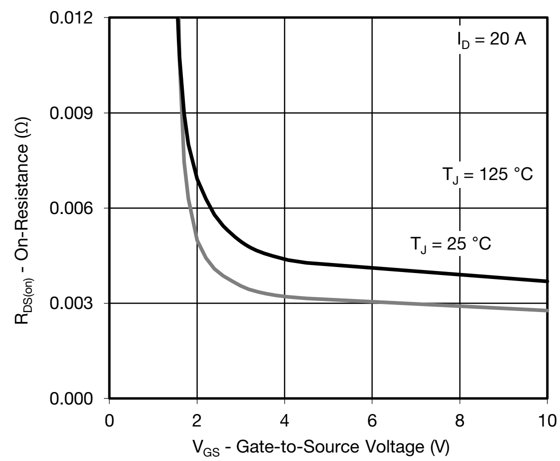
Gate Charge



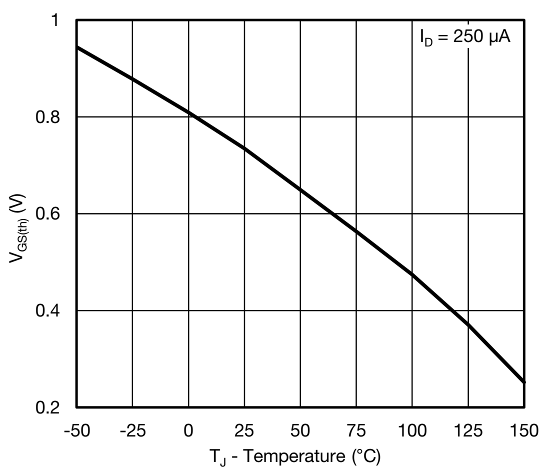
On-Resistance vs. Junction Temperature



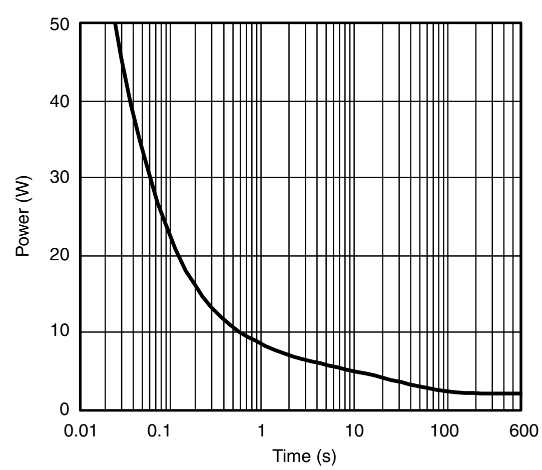
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

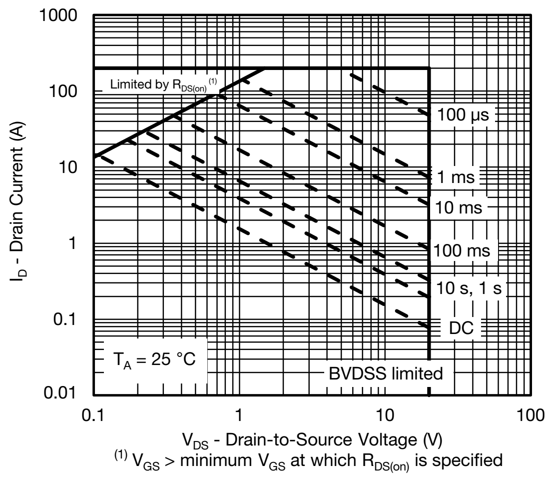


Threshold Voltage

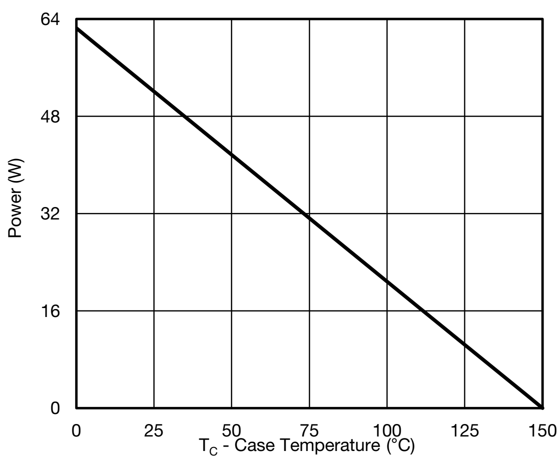


Single Pulse Power, Junction-to-Ambient

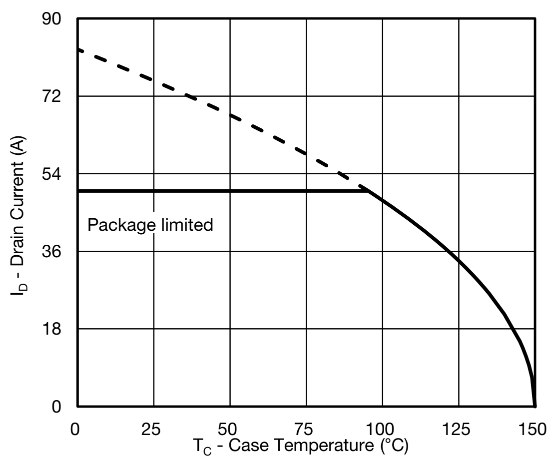
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area



Power, Junction-to-Case

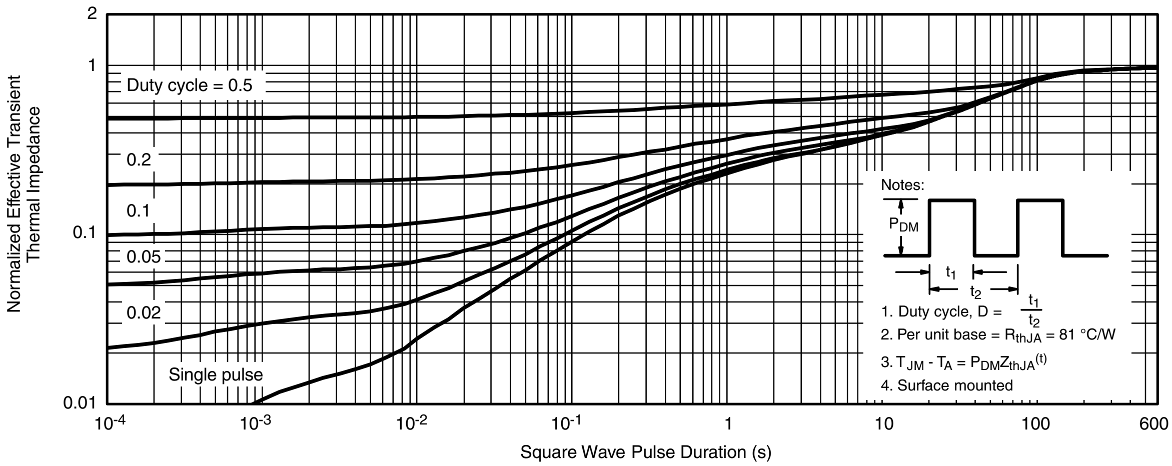


Current Derating [a]

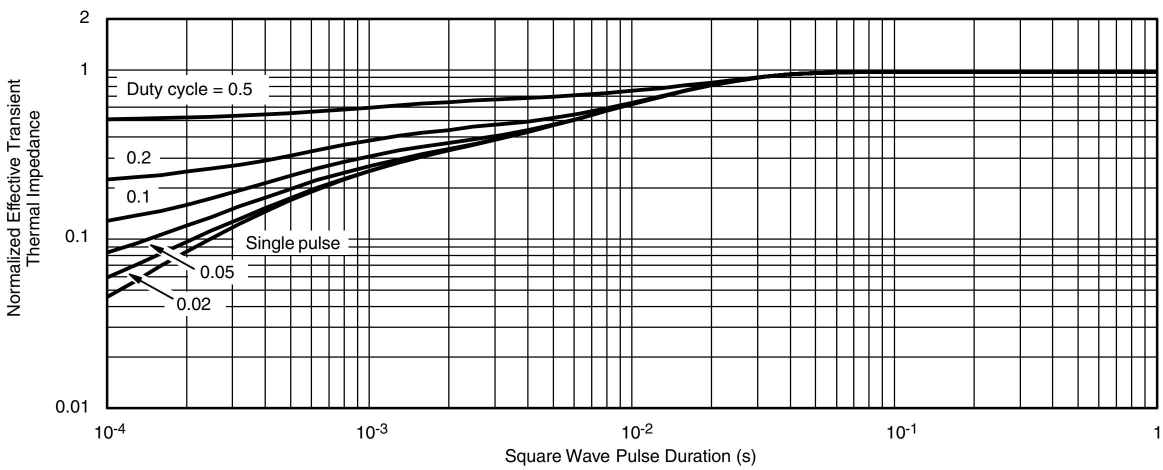
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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