# MOSFET – Power, N-Channel, DPAK

### 24 V, 110 A

#### **Features**

- Planar HD3e Process for Fast Switching Performance
- Low R<sub>DS(on)</sub> to Minimize Conduction Loss
- Low C<sub>iss</sub> to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	24	V
Gate-to-Source Voltage - Continuous	V <sub>GS</sub>	±20	V
Thermal Resistance – Junction–to–Case Total Power Dissipation @ T <sub>C</sub> = 25°C	R <sub>0JC</sub> P <sub>D</sub>	1.35 110	°C/W W
Drain Current  - Continuous @ T <sub>C</sub> = 25°C, Chip  - Continuous @ T <sub>C</sub> = 25°C	I <sub>D</sub> I <sub>D</sub>	110 110	A A
Limited by Package  - Continuous @ T <sub>A</sub> = 25°C	I <sub>D</sub>	32	Α
Limited by Wires - Single Pulse (t <sub>p</sub> = 10 μs)	I <sub>D</sub>	110	Α
Thermal Resistance  - Junction-to-Ambient (Note 1)  - Total Power Dissipation @ T <sub>A</sub> = 25°C  - Drain Current - Continuous @ T <sub>A</sub> = 25°C	R <sub>θJA</sub> P <sub>D</sub> I <sub>D</sub>	52 2.88 17.5	°C/W W A
Thermal Resistance  - Junction-to-Ambient (Note 2)  - Total Power Dissipation @ T <sub>A</sub> = 25°C  - Drain Current - Continuous @ T <sub>A</sub> = 25°C	R <sub>θJA</sub> P <sub>D</sub> I <sub>D</sub>	100 1.5 12.5	°C/W W A
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^{\circ}C$ ( $V_{DD} = 50$ Vdc, $V_{GS} = 10$ Vdc, $I_L = 15.5$ Apk, $L = 1.0$ mH, $R_G = 25 \Omega$ )	E <sub>AS</sub>	120	mJ
Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s)	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

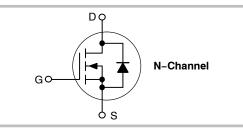
- 1. When surface mounted to an FR4 board using 0.5 sq in drain pad size.
- When surface mounted to an FR4 board using the minimum recommended pad size.



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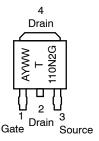
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
24 V	4.1 mΩ @ 10 V	110 A





DPAK CASE 369AA (Surface Mount) STYLE 2

# MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location\*

Y = Year

WW = Work Week

T110N2 = Device Code

G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

#### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

ELECTRICAL CHARACTER	Symbol	Min	Тур	Max	Unit		
OFF CHARACTERISTICS	Cymbol	IVIIII	Typ	Max	Onit		
Drain-to-Source Breakdown Vol (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA) Positive Temperature Coefficient	V <sub>(BR)DSS</sub>	24	28 15		V mV/°C		
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V) (V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> =	I <sub>DSS</sub>			1.5 10	μΑ		
Gate-Body Leakage Current (Vo	$_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V})$	I <sub>GSS</sub>			±100	nA	
ON CHARACTERISTICS (Note 3	3)						
Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 250 \mu A)$ Negative Threshold Temperature	V <sub>GS(th)</sub>	1.0	1.5 5.0	2.0	V mV/°C		
$ \begin{array}{c} \text{Static Drain-to-Source On-Resi} \\ \text{(V}_{\text{GS}} = 10 \text{ V, I}_{\text{D}} = 110 \text{ A)} \\ \text{(V}_{\text{GS}} = 4.5 \text{ V, I}_{\text{D}} = 55 \text{ A)} \\ \text{(V}_{\text{GS}} = 10 \text{ V, I}_{\text{D}} = 20 \text{ A)} \\ \text{(V}_{\text{GS}} = 4.5 \text{ V, I}_{\text{D}} = 20 \text{ A)} \end{array} $	R <sub>DS(on)</sub>		4.1 5.5 3.9 5.5	4.6 6.2	mΩ		
Forward Transconductance (V <sub>DS</sub>	9FS		44		Mhos		
DYNAMIC CHARACTERISTICS							
Input Capacitance		C <sub>iss</sub>		2710	3440	pF	
Output Capacitance	$(V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz})$	C <sub>oss</sub>		1105	1670		
Transfer Capacitance		C <sub>rss</sub>		450	640		
SWITCHING CHARACTERISTIC	CS (Note 4)						
Turn-On Delay Time		t <sub>d(on)</sub>		11	22	ns	
Rise Time	(V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 10 V,	t <sub>r</sub>		39	80		
Turn-Off Delay Time	$I_D = 40 \text{ A}, R_G = 3.0 \Omega$	t <sub>d(off)</sub>		27	40		
Fall Time		t <sub>f</sub>		21	40		
Gate Charge		Q <sub>T</sub>		23.6	28	nC	
	(V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 40 A, V <sub>DS</sub> = 10 V) (Note 3)	(V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 40 A, V <sub>DS</sub> = 10 V) (Note 3) Q <sub>GS</sub> 5.1					
	26 , , ,	$Q_{GD}$		11			
SOURCE-DRAIN DIODE CHAR	ACTERISTICS						
Forward On-Voltage	$(I_S = 20 \text{ A}, V_{GS} = 0 \text{ V}) \text{ (Note 3)}$ $(I_S = 55 \text{ A}, V_{GS} = 0 \text{ V})$ $(I_S = 20 \text{ A}, V_{GS} = 0 \text{ V}, T_J = 125^{\circ}\text{C})$	V <sub>SD</sub>		0.82 0.99 0.65	1.2	V	
Reverse Recovery Time		t <sub>rr</sub>		36.5		ns	
	(I <sub>S</sub> = 30 A, V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>a</sub>		30			
	G 1771-7 (	t <sub>b</sub>		25			
Reverse Recovery Stored Charge		Q <sub>rr</sub>		0.048		μС	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 3. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2%.

<sup>4.</sup> Switching characteristics are independent of operating junction temperatures.

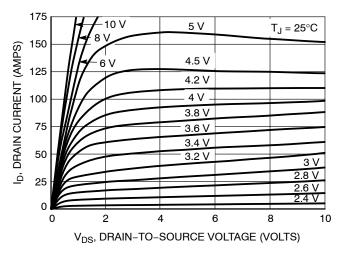
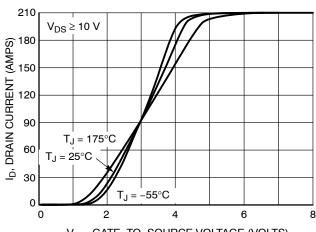


Figure 1. On-Region Characteristics



V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (VOLTS) Figure 2. Transfer Characteristics

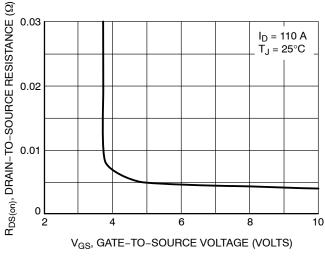


Figure 3. On-Resistance versus Gate-to-Source Voltage

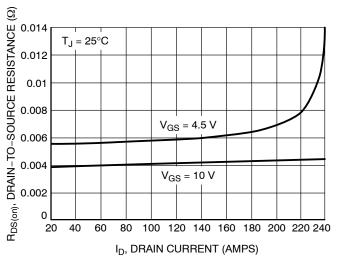


Figure 4. On-Resistance versus Drain Current and Gate Voltage

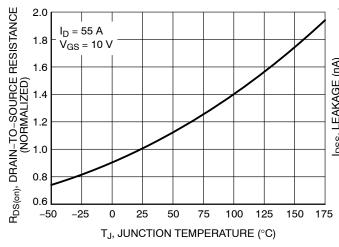


Figure 5. On–Resistance Variation with Temperature

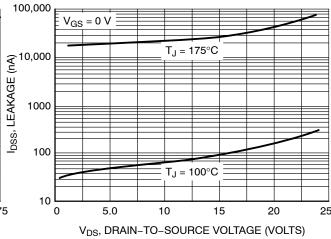


Figure 6. Drain-to-Source Leakage Current versus Voltage

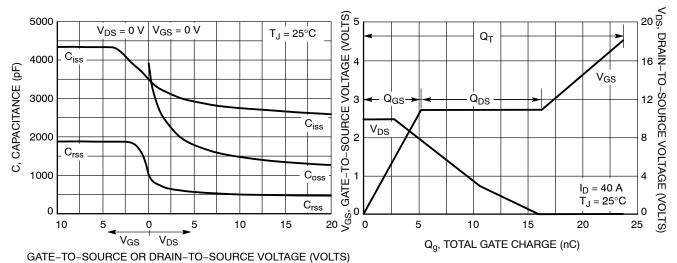


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

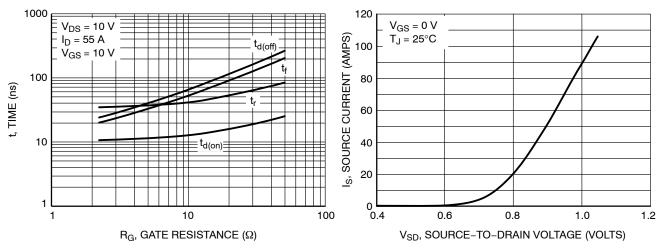


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Diode Forward Voltage versus Current

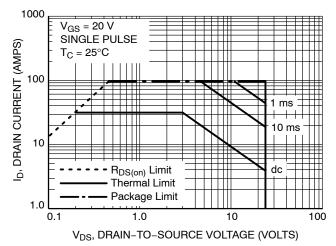


Figure 11. Maximum Rated Forward Biased Safe Operating Area

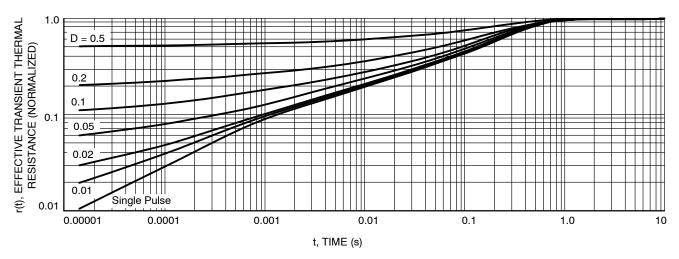


Figure 12. Thermal Response

#### **ORDERING INFORMATION**

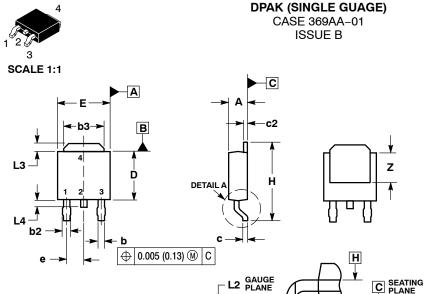
Device	Package	Shipping <sup>†</sup>
NTD110N02RT4G	DPAK (Pb-Free)	2500 / Tape & Reel
STD110N02RT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP

Capable.

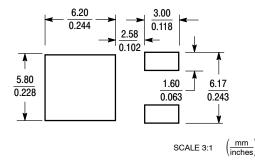
4. ANODE



**DETAIL A** ROTATED 90° CW STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE STYLE 1: PIN 1. BASE STYLE 2: PIN 1. GATE STYLE 3: PIN 1. ANODE 2. COLLECTOR 3. EMITTER 2. CATHODE 3. ANODE 2. DRAIN 3. SOURCE 4. COLLECTOR 4. DRAIN CATHODE STYLE 5: STYLE 6: STYLE 7: PIN 1. GATE 2. ANODE 3. CATHODE PIN 1. GATE 2. COLLECTOR PIN 1. MT1 2. MT2 3. GATE 3. EMITTER

COLLECTOR

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

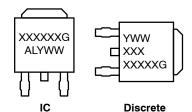
**DATE 03 JUN 2010** 

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: INCHES.
  3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-
- MENSIONS b3, L3 and Z.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H

	INCHES		S MILLIMET		
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.030	0.045	0.76	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
E	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29	BSC	
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.108 REF		2.74	REF	
L2	0.020 BSC		0.51	BSC	
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

#### **GENERIC** MARKING DIAGRAM\*



XXXXXX = Device Code Α = Assembly Location L = Wafer Lot ٧ = Year = Work Week WW = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

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