- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Separate Negative-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Typical Clock Input Frequency . . . 50 MHz
- Fully Buffered Outputs

#### description

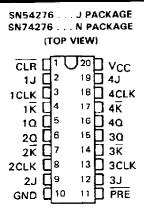
These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by up to 50%. They feature hysteresis at each clock input, fully buffered outputs, and direct clear capability, and are presettable through a buffer that also features an input hysteresis loop. The negative-edge-triggering clocks are directly compatible with earlier Series 54/74 single and dual pulse-triggered flip-flops. These circuits can be used to emulate D- or T-type flip-flops by hard-wiring the inputs, or to implement asychronous sequential functions.

The SN54276 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C; the SN74726 is characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C.

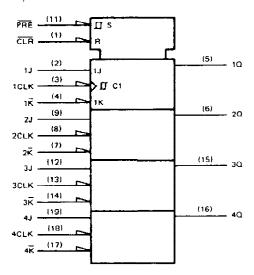
FUNCTION TABLE (EACH FLIP-FLOP)

COMMON	INPUTS	LNP	INPUTS (		
PRE	CLR	CLK	J	ĸ	a
L	Н	х	Х	Х	H
н	L	×	X	X	L
L	L	×	х	Х	H <sup>†</sup>
н	Н	1	L	Н	$\alpha_0$
Н	Н	1	н	Н	н
н	н	ļ ,	L	L	L
H	H	1	Н	L	TOGGLE
Н	Н	н	×	×	<i>G</i> 0

<sup>†</sup> This configuration is nonstable; that is, it may not persist when preset and clear return to their inactive (high) level.

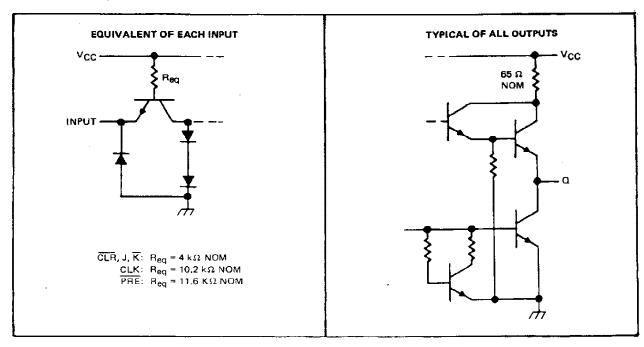


## logic symbol‡



\*This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V	
	SN54276	
	\$N74276	0° C to 70° C
Storage temperature range		65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			SN54276	•		SN74276		UNIT
	_	MIN	NOM	MAX	MIN	NOM	MAX	JUNIT
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4,75	5	5.25	V
High-level output current, IOH				-800			-800	μА
Low-level output curi	rent, IOL			16			16	mA
Clock frequency		0		35	0		35	MHz
	Clock high	13.5			13,5			ns
Pulse width, tw	Clock low	15			15			
	Preset or clear low	12			12			
_	J, K inputs	31			34			ns
Setup time, t <sub>su</sub>	Clear and preset inactive state	10↓			104			'''
Input hold time, th		101			104			ns
Operating free-air temperature, TA		-55		125	0		70	°C

<sup>1</sup> The arrow indicates that the falling edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CO	MIN	TYP‡	MAX	UNIT	
VIH	High-level input voltage			2			V
VIL	Low-level input voltage				-	8.0	V
VIK	Input clamp voltage	V <sub>CC</sub> = MIN,	1 <sub>1</sub> = -12 mA			-1.5	٧
Voн	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V,	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = –800 µA	2.4	3.4		V
v <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>1L</sub> = 0.8 V,	V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4	V
t <sub>1</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub> </sub> = 5.5 V		-	1	пΑ
<del>П</del> Н	High-level input current	VCC = MAX,	V <sub>1</sub> = 2.4 V			40	μА
11L	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V			-1,6	mA
los	Short-circuit autput current§	V <sub>CC</sub> = MAX		-30		85	mΑ
Icc	Supply current	V <sub>CC</sub> = MAX			60	81	mA

<sup>&</sup>lt;sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25 °C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Maximum clock frequency		35	50		MHz
<sup>I</sup> max <sup>t</sup> PLH	Propagation delay time, low-to-high-level output from preset	C <sub>L</sub> = 15 pF.		15	25	ns
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output from clear	R <sub>L</sub> = 400 Ω,		18	30	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high level output from clock	See Note 2		17	30	ns
tPHL	Propagation delay time, high-to-low level output from clock			20	30	กร

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

<sup>‡</sup>All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C.

 $<sup>\</sup>S Not \, more \, than \, one \, output should be shorted at a time.$ 





11-Apr-2013

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
SN74276DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74276DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74276DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74276N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74276N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74276N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74276N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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<sup>(3)</sup> MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.





11-Apr-2013

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



#### NOTES:

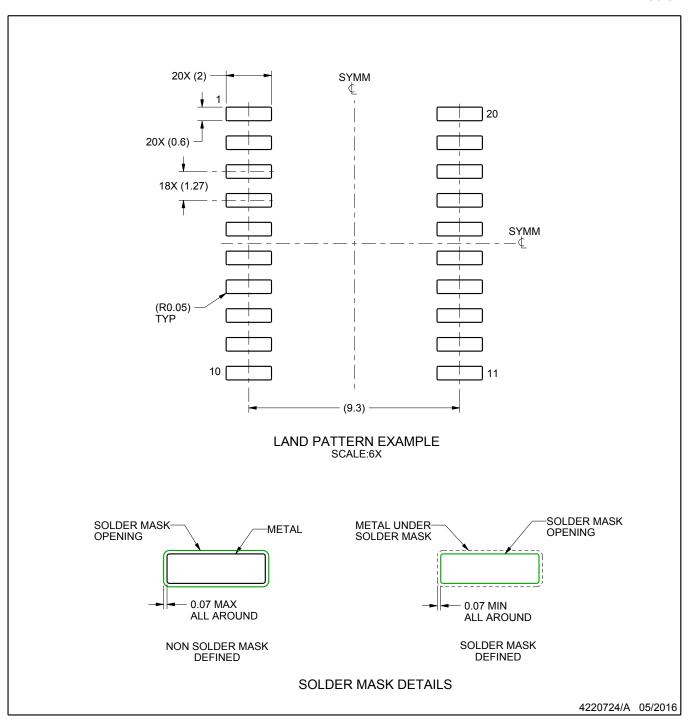
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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