

RoHS Compliant

CFast 2.0

SV170-CFast 2.0 Product Specifications



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Version 1.4



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Specifications Overview:

- **Compliance with SATA Interface**
 - Serial ATA Revision 3.2
 - SATA 6 Gb/s
 - ATA-8 command set
 - Backward compatible with SATA 1.5/3 Gb/s
- **Capacity**
 - 30, 60, 120, 240, 480 GB
- **Performance* (Est.)**
 - Burst read/write: 600 MB/sec
 - Sequential read: Up to 560 MB/sec
 - Sequential write: Up to 495 MB/sec
 - Random read (4K): Up to 79,000 IOPS
 - Random write (4K): Up to 84,000 IOPS
- **Flash Management**
 - Low-Density Parity-Check (LDPC) Code
 - Global Wear Leveling
 - Flash bad-block management
 - Flash Translation Layer: Page Mapping
 - Power Failure Management
 - S.M.A.R.T.
 - Device Sleep
 - ATA Secure Erase
 - TRIM
 - Hyper Cache Technology
 - Over-Provisioning
 - DataRAID™
 - SMART Read Refresh™
- **NAND Flash Type:** 3D TLC (BiCS3)
- **MTBF:** >3,000,000 hours
- **Temperature Range**
 - Operating:
 - Standard: 0°C to 70°C
 - Wide: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Power Consumption***
 - Supply voltage: 3.3V
 - Active mode: 500 mA
 - Idle mode: 105 mA
- **Form Factor**
 - CFast
 - Dimensions: 42.80 x 36.45 x 3.60, unit: mm
 - Net Weight: 9.33 g ± 5%
- **Connector Type**
 - 7 + 17 pin female connector
- **Endurance (in drive writes per day: DWPD)**
 - 30 GB: 1.74 DWPD
 - 60 GB: 2.09 DWPD
 - 120 GB: 2.48 DWPD
 - 240 GB: 2.74 DWPD
 - 480 GB: 2.71 DWPD
- **Reliability**
 - Thermal Sensor
 - End-to-End Data Protection
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

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1. General Descriptions

Apacer SV170-CFast 2.0 is the latest enhancement of conventional CFast form factor that delivers various technological advantages. It utilizes 3D NAND for higher capacity up to 480 GB and provides more power efficiency than 2D NAND. This new flash memory card comes with SATA 6 Gb/s interface for higher performance and consists of SATA-based 7-pin signal segment and 17-pin for power and control purposes. Designed without DRAM on the internal controlling unit, SV170-CFast ensures data integrity by preventing data loss during a sudden power outage.

For data efficiency, SV170-CFast 2.0 delivers data transfer rates up to 560 MB/s in sequential access and 79,000 IOPS in 4KB random access. In addition, Apacer CFast cards come with S.M.A.R.T. for lifetime monitoring. Apacer SV170-CFast 2.0 guarantees reliability of applications in harsh environments by implementing intelligent Flash Management algorithms and LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability.

2. Functional Block

Apacer SV170-CFast 2.0 includes a single-chip SATA 6 Gb/s and the flash media. The controller integrates the flash management unit to support multi-channel, multi-bank flash arrays. Figure 2-1 shows the functional block diagram.

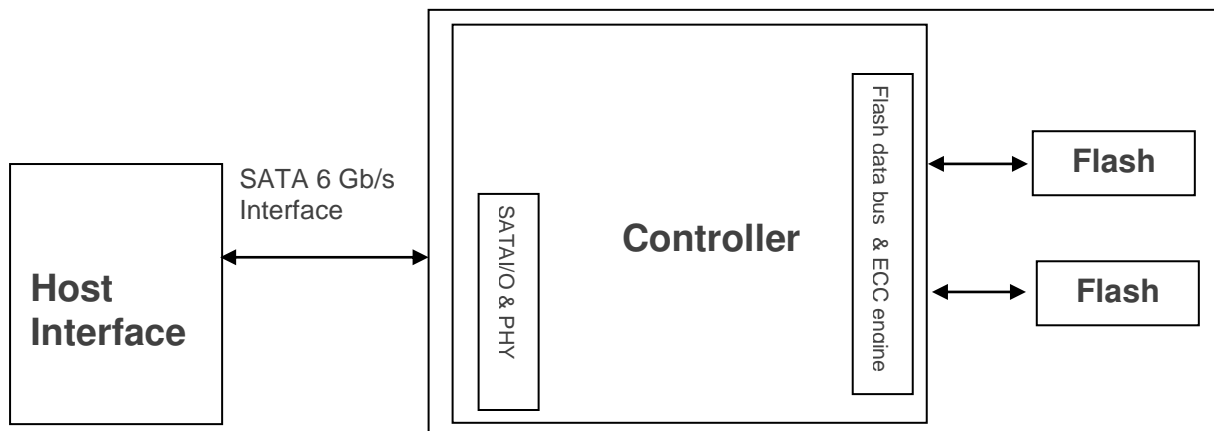


Figure 2-1 Functional Block Diagram

3. Pin Assignments

Table 3-1 describes SV170-CFast 2.0 signal segment, and Table 3-2, its power segment.

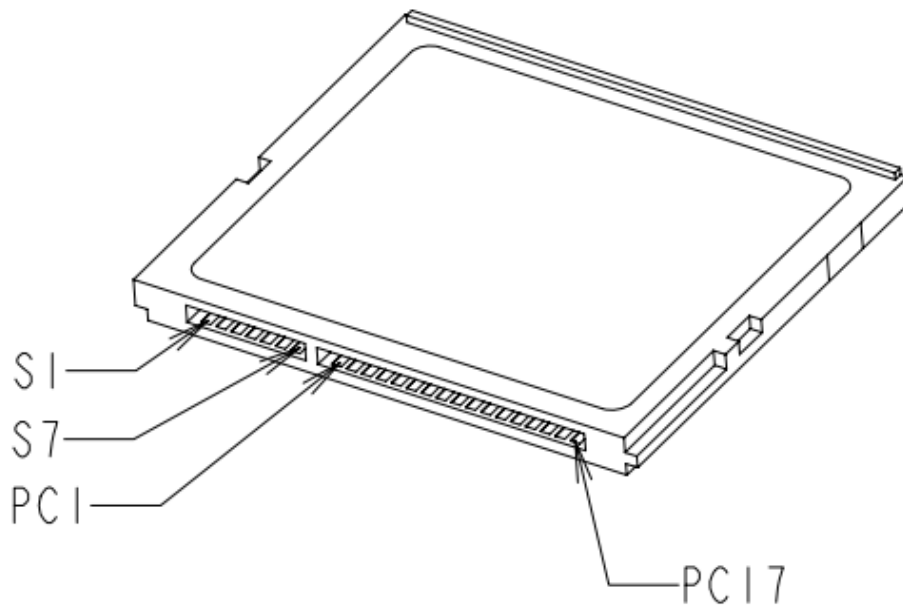


Figure 3-1 Pin Assignment

Table 3-1 Signal Segment

Pin	Definition	Description
S1	GND	Ground
S2	A+	SATA Differential Signal Pair A
S3	A-	
S4	GND	Ground
S5	B-	SATA Differential Signal Pair B
S6	B+	
S7	GND	Ground

Table 3-2 Power Segment

Pin	Definition	Type	Description
PC1	CDI	Input	Card Detect In
PC2	PGND	Device GND	Device GND
PC3	DEVSLP*	DEVSLP card input	DEVSLP enable
PC4			Reserved
PC5			Reserved
PC6			Reserved
PC7	PGND	Device GND	Device GND
PC8	LED1	LED Output	Power indicator
PC9	LED2	LED Output	Access indicator
PC10			Reserved
PC11			Reserved
PC12	IFDet	GND	Card output, connect to PGND on card
PC13	PWR	3.3V	Device power (3.3V)
PC14	PWR	3.3V	Device power (3.3V)
PC15	PGND	Device GND	Device GND
PC16	PGND	Device GND	Device GND
PC17	CDO	Output	Card Detect Out

*Optional

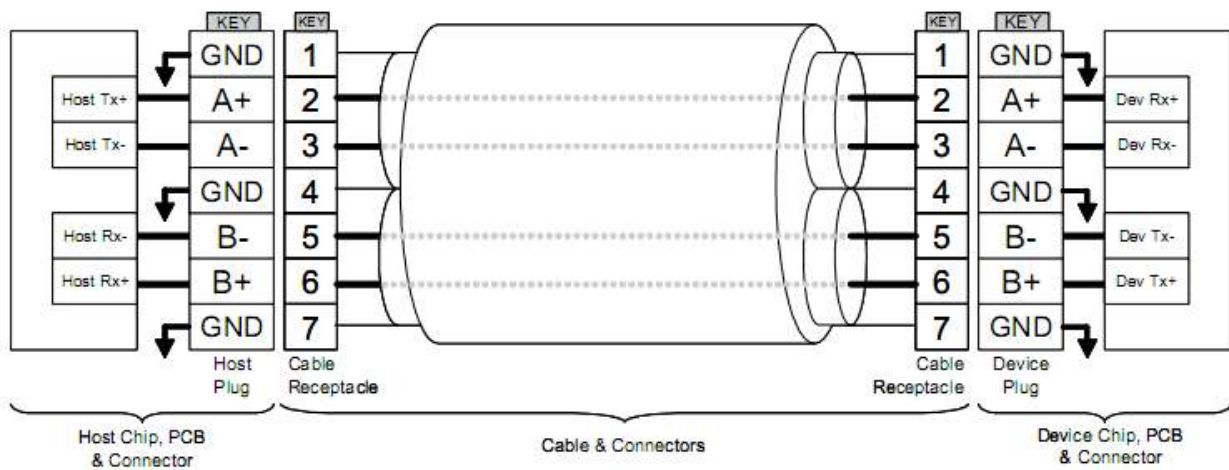


Figure 3-2 SATA Cable / Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable while the connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

4. Product Specifications

4.1 Capacity

Capacity specifications of the SV170-CFast 2.0 are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Total LBA
30 GB	30,016,659,456	16,383	16	63	58,626,288
60 GB	60,022,480,896	16,383	16	63	117,231,408
120 GB	120,034,123,776	16,383	16	63	234,441,648
240 GB	240,057,409,536	16,383	16	63	468,862,128
480 GB	480,103,981,056	16,383	16	63	937,703,088

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of SV170-CFast 2.0 product family is available as shown in Table 4-2.

Table 4-2 Performance Specifications

Performance	Capacity	30 GB	60 GB	120 GB	240 GB	480 GB
	Sequential Read* (MB/s)		295	550	560	560
Sequential Write* (MB/s)		130	255	450	490	495
Random Read IOPS** (4K)		19,000	38,000	63,000	79,000	78,000
Random Write IOPS** (4K)		29,000	60,000	77,000	82,000	84,000

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

**Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of SV170-CFast 2.0 are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C (Standard); -40°C to 85°C (Wide)
Non-operating temp.	-40°C to 100°C
Operating vibration	7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G)
Non-operating vibration	4.02 GRMS, 15~2000 Hz/random (compliant with MIL-STD-810G)
Operating shock	50G, 11ms
Non-operating shock	1500G, 0.5ms (compliant with MIL-STD-883K)

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SV170-CFast 2.0. Serving as statistical reference, the prediction result for SV170-CFast is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

SV170-CFast 2.0 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810G

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Drive Writes Per Day

Capacity	Drive Writes Per Day
30 GB	1.74
60 GB	2.09
120 GB	2.48
240 GB	2.74
480 GB	2.71

Note:

- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)

5. Flash Management

5.1 Error Correction/Detection

SV170-CFast implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

5.6 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.7 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

5.8 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.9 Over-Provisioning

Over-Provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.10 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

5.11 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

5.12 Device Sleep (DevSleep or DEVSLP) Mode

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating a particular pin as DEVSLP signal with an aim to reducing power consumption.



5.13 SATA Power Management

By complying with SATA 6 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 μ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption \leq 5 mW; host assertion time \leq 10 ms; exit timeout from this state \leq 20 ms (unless specified otherwise in SATA Identify Device Log).

Note: The behaviors of power management features would depend on host/device settings.

6. Reliability Features

6.1 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and ensure data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

6.2 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

7. Software Interface

7.1 Command Set

This section defines the software requirements and the format of the commands the host sends to SV170-CFast. Commands are issued to SV170-CFast by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 7-1 Command Set

Code	Command	Code	Command		
00h	NOP	C9h	READ DMA WITHOUT RETRY		
06h	DATA SET MANAGEMENT	CAh	WRITE DMA		
10h-1Fh	RECALIBRATE	CBh	WRITE DMA WITHOUT RETRY		
20h	READ SECTORS	CEh	WRITE MULTIPLE FUA EXT		
21	READ SECTORS WITHOUT RETRY	E0h	STANDBY IMMEDIATE		
24h	READ SECTORS EXT	E1h	IDLE IMMEDIATE		
25h	READ DMA EXT	E2h	STANDBY		
27h	READ NATIVE MAX ADDRESS EXT	E3h	IDLE		
29h	READ MULTIPLE EXT	E4h	READ BUFFER		
2Fh	READ LOG EXT	E5h	CHECK POWER MODE		
30h	WRITE SECTORS	E6h	SLEEP		
31h	WRITE SECTORS WITHOUT RETRY	E7h	FLUSH CACHE		
34h	WRITE SECTORS EXT	E8h	WRITE BUFFER		
35h	WRITE DMA EXT	E9h	READ BUFFER DMA		
37h	SET NATIVE MAX ADDRESS EXT	EAh	FLUSH CACHE EXT		
38h	CFA WRITE SECTORS WITHOUT	EBh	WRITE BUFFER DMA		
39h	WRITE MULTIPLE EXT	ECh	IDENTIFY DEVICE		
3Dh	WRITE DMA FUA EXT	EFh	SET FEATURES		
3Fh	WRITE LONG EXT	EFh	02h	ENABLE VOLATILE WRITE	
40h	READ VERIFY SECTORS	EFh	03h	SET TRANSFER MODE	
41h	READ VERIFY SECTORS WITHOUT	EFh	05h	ENABLE THE APM FEATURE	
42h	READ VERIFY SECTORS EXT	EFh	10h	ENABLE USE OF SATA	
44h	ZERO EXT	EFh	10h	02h	ENABLE DMA SETUP FIS AUTO-ACTIVATE
45h	WRITE UNCORRECTABLE EXT	EFh	10h	03h	ENABLE DEVICE-INITIATED INTERFACE POWER STATE
47h	READ LOG DMA EXT	EFh	10h	06h	ENABLE SOFTWARE SETTINGS PRESERVATION
57h	WRITE LOG DMA EXT	EFh	10h	07h	ENABLE DEVICE AUTOMATIC PARTIAL TO SLUMBER
60h	READ FPDMA QUEUED	EFh	10h	09h	ENABLE DEVICE SLEEP

Code		Command	Code		Command
61h		WRITE FPDMA QUEUED	EFh	55h	DISABLE READ LOOK-AHEAD
70h-7Fh		SEEK	EFh	66h	DISABLE REVERTING TO POWER-ON DEFAULTS
90h		EXECUTE DEVICE DIAGNOSTIC	EFh	82h	DISABLE VOLATILE WRITE
91h		INITIALIZE DEVICE PARAMETERS	EFh	85h	DISABLE THE APM FEATURE
92h		DOWNLOAD MICROCODE	EFh	90h	DISABLE USE OF SATA
93h		DOWNLOAD MICROCODE DMA	EFh	90h 02h	DISABLE DMA SETUP FIS AUTO-ACTIVATE
B0h		SMART	EFh	90h 03h	DISABLE DEVICE-INITIATED INTERFACE POWER STATE
B0h	D0h	SMART READ DATA	EFh	90h 06h	DISABLE SOFTWARE SETTINGS PRESERVATION
B0h	D1h	SMART READ ATTRIBUTE THRESHOLDS	EFh	90h 07h	DISABLE DEVICE AUTOMATIC PARTIAL TO SLUMBER
B0h	D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	EFh	90h 09h	DISABLE DEVICE SLEEP
B0h	D3h	SMART SAVE ATTRIBUTE VALUES	EFh	AAh	ENABLE READ LOOK-AHEAD
B0h	D4h	SMART EXECUTE OFF-LINE IMMEDIATE	EFh	CCh	ENABLE REVERTING TO POWER-ON DEFAULTS
B0h	D5h	SMART READ LOG	F1h		SECURITY SET PASSWORD
B0h	D6h	SMART WRITE LOG	F2h		SECURITY UNLOCK
B0h	D8h	SMART ENABLE OPERATIONS	F3h		SECURITY ERASE PREPARE
B0h	D9h	SMART DISABLE OPERATIONS	F4h		SECURITY ERASE UNIT
B0h	DAh	SMART RETURN STATUS	F5h		SECURITY FREEZE LOCK
B0h	DBh	SMART ENABLE/DISABLE AUTOMATIC OFF-LINE	F6h		SECURITY DISABLE PASSWORD
B1h		DEVICE CONFIGURATION	F8h		READ NATIVE MAX ADDRESS
B4h		SANITIZE	F9h		SET MAX ADDRESS
C4h		READ MULTIPLE	F9h	01h	SET MAX SET PASSWORD
C5h		WRITE MULTIPLE	F9h	02h	SET MAXLOCK
C6h		SET MULTIPLE MODE	F9h	03h	SET MAX UNLOCK
C8h		READ DMA	F9h	04h	SET MAX FREEZE LOCK

7.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D4h	EXECUTE OFF-LINE IMMEDIATE
D5h	SMART READ LOG
D6h	SMART WRITE LOG
D8h	ENABLE OPERATIONS
D9h	DISABLE OPERATIONS
DAh	RETURN STATUS

General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status Flag
3	Value
4	Worst
5*-11	Raw Data

*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on Hours
12 (0x0C)	Power Cycle Count
163 (0xA3)	Max. Erase Count
164 (0xA4)	Avg. Erase Count
166 (0xA6)	Total Later Bad Block Count
167 (0xA7)	SSD Protect Mode (Vendor Specific)
168 (0xA8)	SATA PHY Error Count
171 (0xAB)	Program Fail Count
172 (0xAC)	Erase Fail Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
231 (0xE7)	Lifetime Left
241 (0xF1)	Total Sectors of Write

8. Electrical Specifications

8.1 Operating Voltage

Table 8-1 lists the supply voltage for SV170-CFast 2.0.

Table 8-1 Operating Range

Parameter	Symbol	Min	Type	Max	Units
Power Supply	Vcc	3.135	3.3	3.465	V

8.2 Power Consumption

Table 8-2 lists the power consumption for SV170-CFast 2.0.

Table 8-2 Power Consumption

Capacity	30 GB	60 GB	120 GB	240 GB	480 GB
Mode					
Active (mA)	310	390	400	460	500
Idle (mA)	105	100	105	100	105

Note:

*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

9. Physical Characteristics

9.1 Dimensions

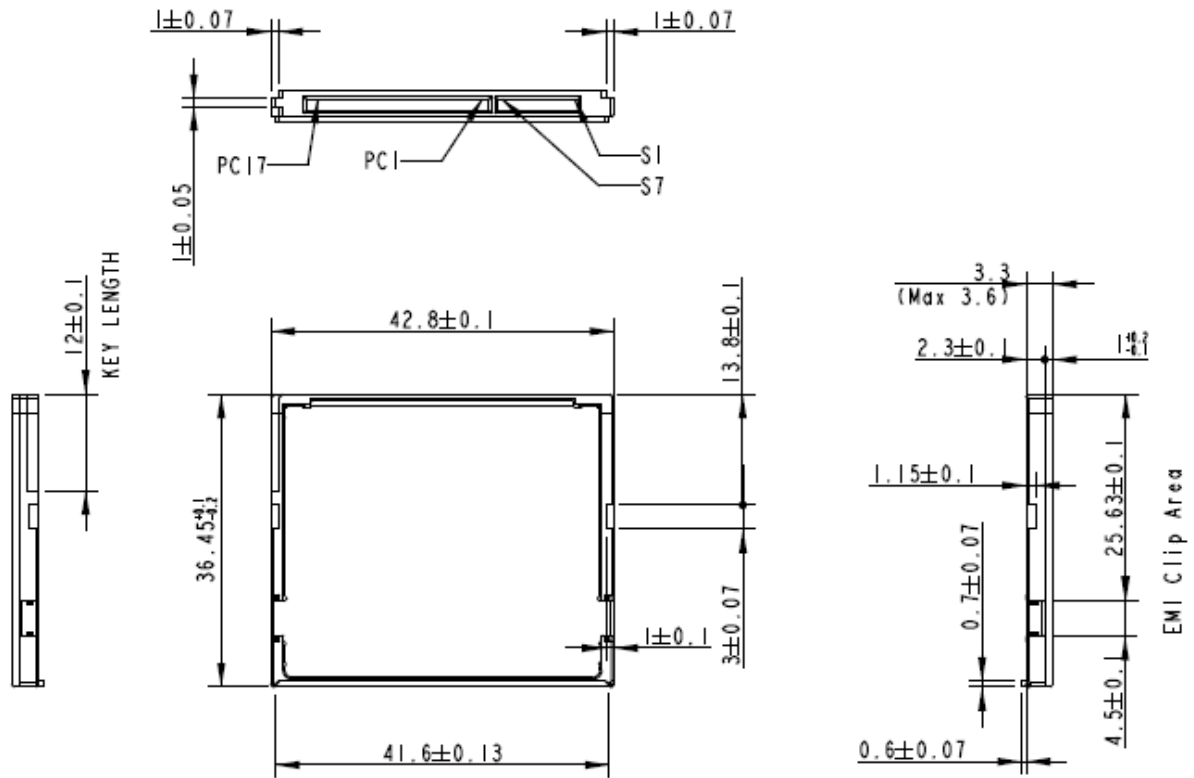


Figure 9-1 Physical Dimensions

Unit: mm

9.2 Net Weight

Capacity	Net Weight (g \pm 5%)
30GB	7.72
60GB	8.23
120GB	9.32
240GB	9.33
480GB	9.32

10. Product Ordering Information

10.1 Product Code Designations

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	A	2	.	1	7	5	X	X	A	.	X	X	X	1	1

Code 1-3 (Product Line & form factor)	MDC CFAST
Code 5-6 (Model/Solution)	SV170-CFAST
Code 7-8 (Product Capacity)	5F: 30GB 5G: 60GB 5H: 120GB 5J: 240GB 5K: 480GB
Code 9 (Flash Type & Product Temp)	G: 3D TLC Standard temperature H: 3D TLC Wide temperature
Code 10 (Product Spec)	A: STD without Write Protect Switch
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	11: DEVSLP + Thermal + OP

10.2 Valid Combinations

Capacity	Standard Temperature	Wide Temperature
30GB	AA2.175FGA.00111	AA2.175FHA.00111
60GB	AA2.175GGA.00111	AA2.175GHA.00111
120GB	AA2.175HGA.00111	AA2.175HHA.00111
240GB	AA2.175JGA.00111	AA2.175JHA.00111
480GB	AA2.175KGA.00111	AA2.175KHA.00111

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
0.1	Preliminary release	6/3/2019
1.0	<ul style="list-style-type: none"> - Updated Performance on Specifications Overview page and 4.2 Performance - Updated Power Consumption on Specifications Overview page and 8.2 Power Consumption - Completed endurance rating at Endurance on Specifications Overview page and 4.6 Endurance 	6/21/2019
1.1	Modified total bytes at Table 4-1 Capacity Specifications	2/10/2020
1.2	<ul style="list-style-type: none"> - Changed SATA 6.0 Gbps to SATA 6 Gb/s in accordance with SATA naming guidelines - Updated operating/non-operating vibration spec at Table 4-3 Environmental Specifications - Added MIL-STD-810G to 4.5 Certification and Compliance - Updated the description for 5.12 DEVSLP (DevSleep or DEVSLP) Mode - Capitalized every letter for commands at 7.1 Command Set and SMART subcommand at 7.2 S.M.A.R.T. 	3/19/2020
1.3	<ul style="list-style-type: none"> - Updated compliance version with SATA Interface from 3.1 to 3.2 on Specifications Overview page - Updated Table 4-1 by changing max LBA to total LBA - Modified the issue version for the note at 4.4 Mean Time Between Failures (MTBF) - Updated technology description for 5.4 Power Failure Management - Updated 7.1 Command Set 	5/29/2020
1.4	<ul style="list-style-type: none"> - Updated MTBF on Specifications Overview page and 4.4 Mean Time Between Failures (MTBF) by changing it from >1,000,000 hours to >3,000,000 hours - Updated the description of 5.2 Bad Block Management 	8/4/2020

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