# LOW SKEW CLOCK DRIVER/ BUFFER FOR MOBILE PC WITH THREE DIMMS

**QS5813**

## FEATURES:

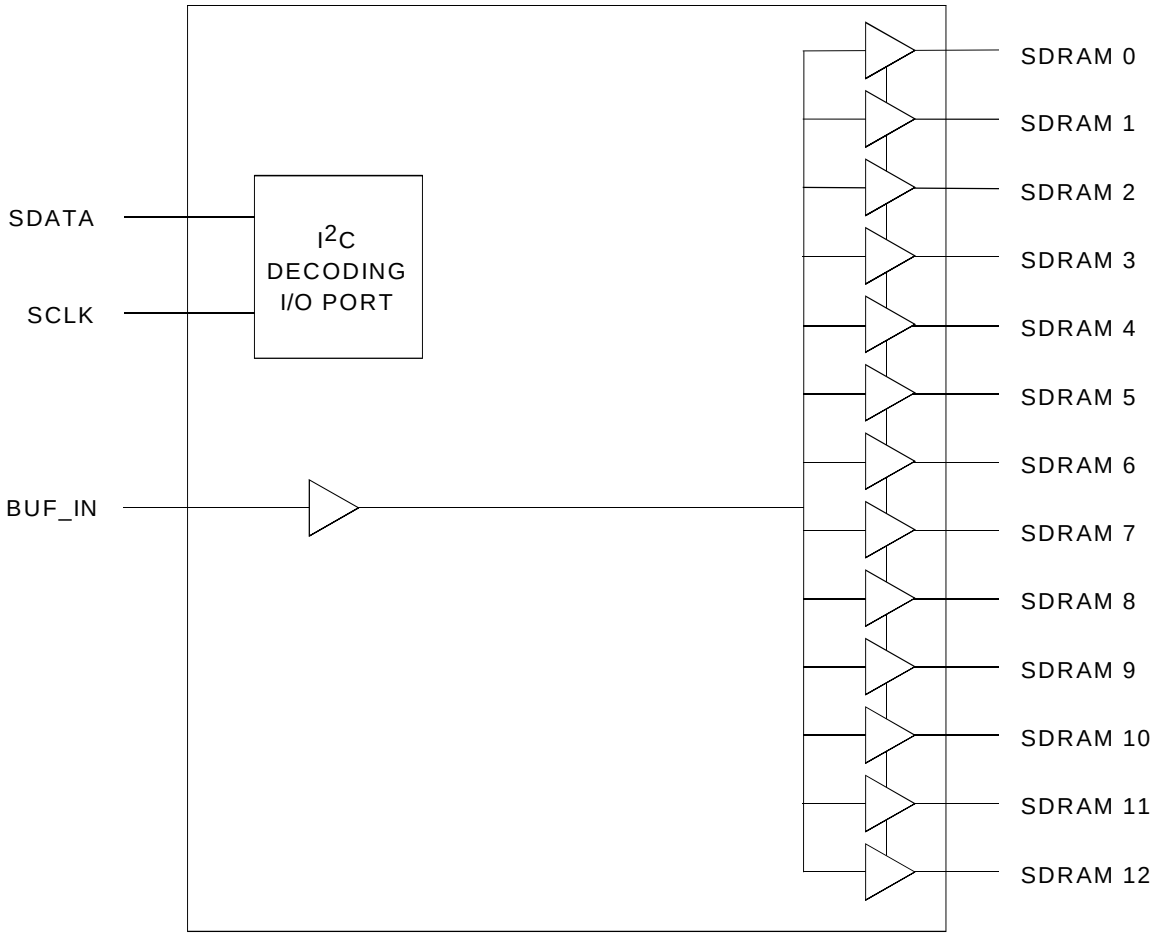
- 1 to 13 output buffer/driver
- $I^2C$ programming capability
- Power Supply Voltage 3.3V ±5%
- Low Skew Outputs (<200ps)
- Multiple $V_{DD}$ and GND for noise reduction
- 28 Pin SSOP package

## DESCRIPTION

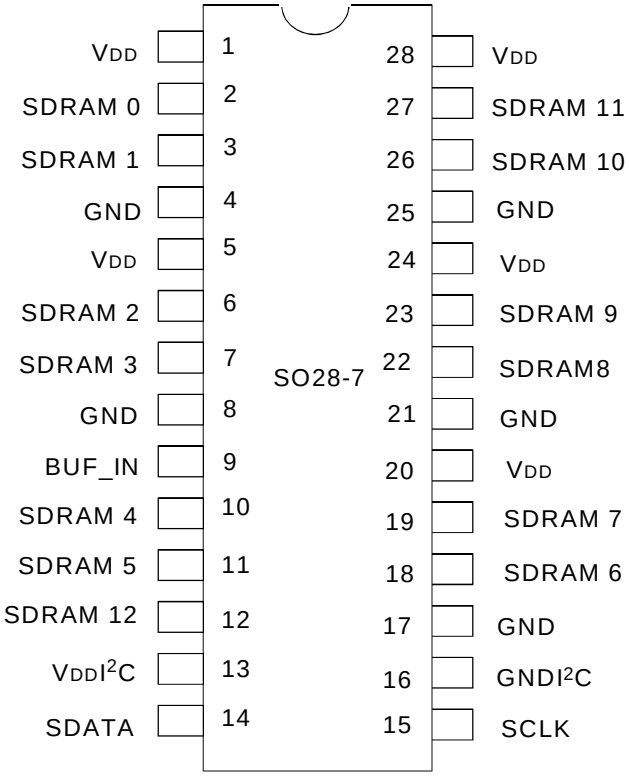
The QS5813 is a high speed, low noise 1-13 non-inverting buffer designed for SDRAM clock buffer applications. Out of the 13 outputs,12 could be used to drive up to three SDRAM DIMMS, and the remaining output is used for external feedback to a PLL stage for synchronization to master clock.

The QS5813 also includes an $I^2C$ interface, which can enable or disable each output clock when the lines are not used. By turning the outputs on and off, $I^2C$ will aid in reducing the Electro Magnetic Interference (EMI).

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| | Supply Voltage to Ground | – 0.5 to + 4.6 | V |
| | DC Output Voltage $V_{OUT}$ | – 0.5 to + 4.6 | V |
| | DC Output Voltage $V_{IN}$ | – 0.5 to + 4.6 | V |
| | DC Input Diode Current with $V_I < 0$ | – 20 | mA |
| | Maximum Power Dissipation at $T_A = 85°C$ | 600 | mW |
| | $T_{STG}$ Storage Temperature | –65 to 150 | °C |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN DESCRIPTION

| Pin Name | Description |
|---|---|
| SDRAM (0:5) | SDRAM Byte 0 Clock Outputs. |
| SDRAM (6:11) | SDRAM Byte 1 Clock Outputs. |
| SDRAM (12) | SDRAM Byte 2 Clock Outputs. |
| BUF_IN | Input for Buffers. |
| SDATA | I²C Data Input. It has 100kΩ internal pull up to $V_{DD}$. |
| SCLK | I²C Data Input. It has 100kΩ internal pull up to $V_{DD}$. |
| $V_{DD}$ | 3.3V power supply for output buffers. |
| GND | Ground for output buffers. |
| GNDI²C | Ground for I²C circuitry. |
| $V_{DD}$I²C | 3.3V Power Supply for I²C circuitry. |

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Operating Condition: $T_A$ = – 40°C to +85°C**

| Symbol | Parameter | Test Conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | For all Inputs | 2 | — | — | V |
| $V_{IL}$ | Input LOW Voltage Level | For all inputs except I²C inputs | — | — | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{IN} = V_{DD}$ | – 5 | — | 5 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = 0V | – 5 | — | 5 | µA |
| | | $V_{IN}$ = 0V; Inputs with 100k pull up | – 100 | — | — | |
| $I_{DD}$ | Supply Current | $C_L$ = 0pF; $f_{IN}$@66.66MHz(1) | — | 50 | 70 | mA |
| | | $C_L$ = 30pF; $f_{IN}$@66.66MHz(1) | — | 130 | 150 | |
| | | $C_L$ = 0pF; $f_{IN}$@100MHz(1) | — | 75 | 105 | |
| | | $C_L$ = 30pF; $f_{IN}$@100MHz(1) | — | 195 | 225 | |
| | | BUF_IN = GND or $V_{DD}$, all other inputs to $V_{DD}$ | — | — | 500 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –36mA | 2.4 | — | — | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 25mA | — | — | 0.4 | V |
| $V_{OL}I^2C$ | Output Low Voltage | SDATA $I_{OL}I^2C$ = 3mA | — | — | 0.4 | V |

**NOTE:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

# AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Rise Time | 0.4V to 2.4V; $C_L$ = 30pF | — | — | 2.2 | ns |
| $t_F$ | Fall Time | 2.4V to 0.4V; $C_L$ = 30pF | — | — | 2.2 | ns |
| DT | Duty Cycle | $V_T$ = 1.5V; $C_L$ = 30pF | 45 | 50 | 55 | % |
| $t_{SK}$ | Skew (output-output) | $V_T$ = 1.5V; $C_L$ = 30pF for all outputs | — | — | 200 | ps |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay | $V_T$ = 1.5V | — | — | 6 | ns |

# OPERATING CHARACTERISTICS , $T_A$ = 25ºC

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 3.135 | 3.3 | 3.465 | V |
| $T_A$ | Operating Temperature | -40 | 25 | 85 | °C |
| $C_L$ | Load Capacitance | — | — | 30 | pF |
| $C_{IN}$ | Input Capacitance | — | — | 15 | pF |

# I²C SERIAL INTERFACE CONTROL

The I²C interface permits individual enable/disable of each clock output: any unused outputs may be disabled to reduce the EMI. The QS5813 is a slave receiver device. It can read back the data stored in the latches for verification.

The data transfer rate supported by the I²C interface is 100k bits/sec. Data is transferred in bytes (with the addition of start, stop, acknowledge bits) in sequential order from the lowest to highest byte with the ability to stop after any complete byte has been transferred. The first two bytes transferred must be a Command Code followed by a Byte Count. Both of these bytes are ignored by the device.

The I²C address of the QS5813 is:

| A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |

Address A0 is the read/write bit and is set to 0 for writes and 1 for reads. During read back, the first byte read is a Byte Count representing the number of bytes following (fixed at 3).

# SERIAL CONFIGURATION COMMAND BITMAPS

Byte 0: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable, outputs held LOW), Default = Enable

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 11 | SDRAM 5 (Active/Inactive) |
| Bit 6 | 10 | SDRAM 4 (Active/Inactive) |
| Bit 5 | — | Initialize to 0 |
| Bit 4 | — | Initialize to 0 |
| Bit 3 | 7 | SDRAM 3 (Active/Inactive) |
| Bit 2 | 6 | SDRAM 2 (Active/Inactive) |
| Bit 1 | 3 | SDRAM 1 (Active/Inactive) |
| Bit 0 | 2 | SDRAM 0 (Active/Inactive) |

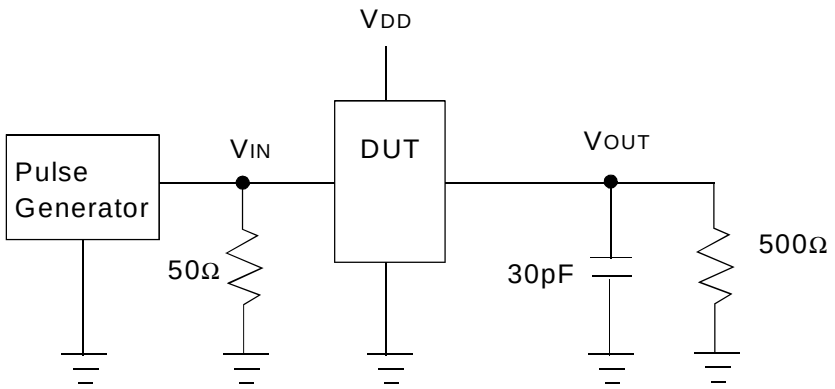
Byte 1: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable, outputs held LOW), Default = Enable

| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | 27 | SDRAM 11 (Active/Inactive) |
| Bit 6 | 26 | SDRAM 10 (Active/Inactive) |
| Bit 5 | 23 | SDRAM 9 (Active/Inactive) |
| Bit 4 | 22 | SDRAM 8 (Active/Inactive) |
| Bit 3 | — | Initialize to 0 |
| Bit 2 | — | Initialize to 0 |
| Bit 1 | 19 | SDRAM 7 (Active/Inactive) |
| Bit 0 | 18 | SDRAM 6 (Active/Inactive) |

Byte 2: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable, outputs held LOW), Default = Enable

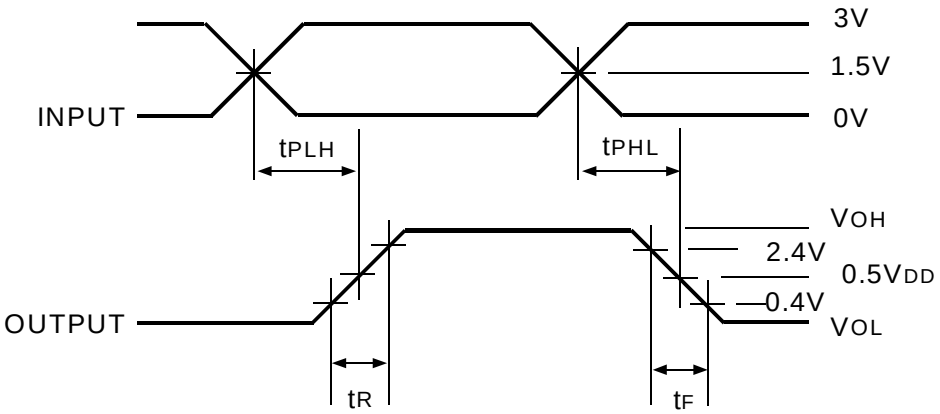
| Bit | Pin # | Description |
|---|---|---|
| Bit 7 | — | Initialize to 0 |
| Bit 6 | 12 | SDRAM 12 (Active/Inactive) |
| Bit 5 | — | Reserved, 1 at power up, set to 0 |
| Bit 4 | — | Reserved, 1 at power up, set to 0 |
| Bit 3 | — | Reserved, 1 at power up, set to 0 |
| Bit 2 | — | Reserved, 1 at power up, set to 0 |
| Bit 1 | — | Reserved, 1 at power up, set to 0 |
| Bit 0 | — | Reserved, 1 at power up, set to 0 |

## TEST CIRCUIT

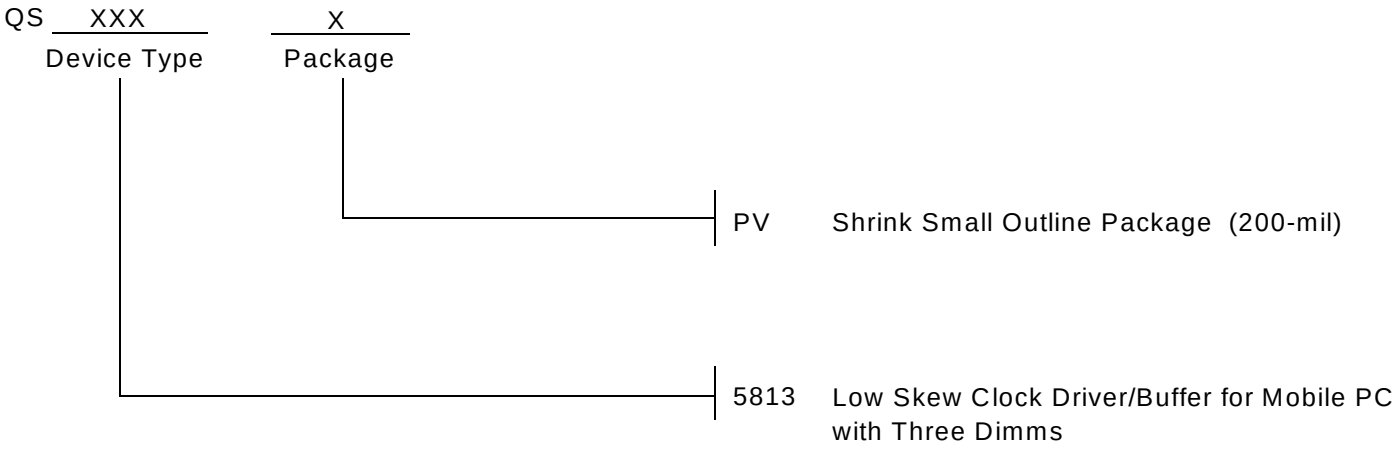



## AC TIMING DIAGRAM

## PROPAGATION DELAY



## ORDERING INFORMATION

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