

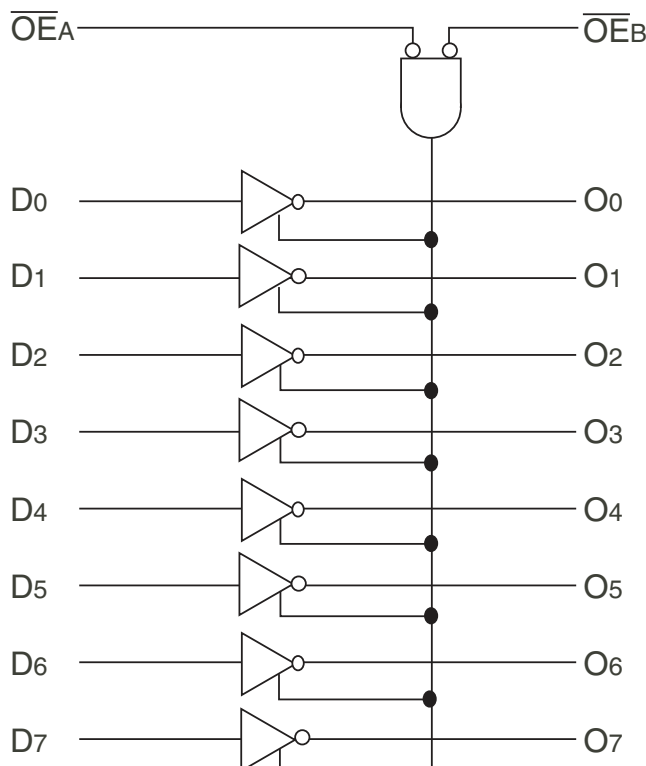
**FEATURES:**

- A and C grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - $V_{OH} = 3.3V$  (typ.)
  - $V_{OL} = 0.3V$  (typ.)
- High Drive outputs (-15mA IOH, 64mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

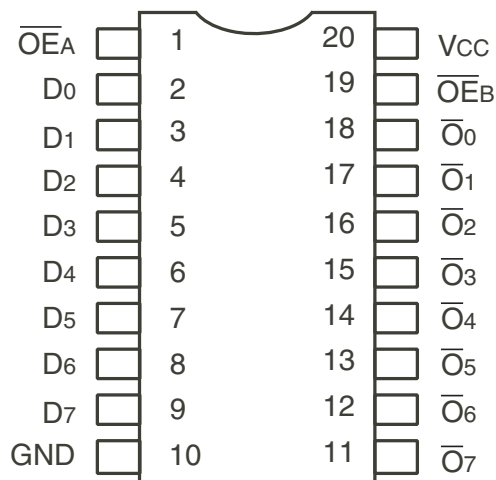
**DESCRIPTION:**

The IDT octal buffer/line driver is built using an advanced dual metal CMOS technology. The FCT540T is similar in function to the FCT240T, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

**FUNCTIONAL BLOCK DIAGRAM**



## PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
QSOP	PCG20	QG
SOIC	PSG20	SOG

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Output and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
OĒA, OĒB	3-State Output Enable Inputs (Active LOW)
D <sub>x</sub>	Inputs
Ō <sub>x</sub>	Outputs

## FUNCTION TABLE<sup>(1)</sup>

Inputs			Outputs
OĒA	OĒB	D	
L	L	L	H
L	L	H	L
H	H	X	Z

### NOTE:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current <sup>(4)</sup> (3-State Output pins) <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_I = 0.5\text{V}$	—	—	$\pm 1$	
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.3	0.55	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B = \text{GND}$ One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 10MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	1.5	3.5	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	1.8	4.5	
		V <sub>CC</sub> = Max. Outputs Open f <sub>i</sub> = 2.5MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = \text{GND}$ Four Bits Toggling	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	3	6 <sup>(5)</sup>	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	5	14 <sup>(5)</sup>	

## NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V). All other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of  $\Delta I_{CC}$  formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
I<sub>C</sub> = I<sub>CC</sub> +  $\Delta I_{CC} \text{ DH}_{NT}$  + I<sub>CCD</sub> (f<sub>i</sub>N<sub>i</sub>)  
I<sub>CC</sub> = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
DH = Duty Cycle for TTL Inputs High  
N<sub>T</sub> = Number of TTL Inputs at DH  
I<sub>CCD</sub> = Dynamic Current caused by an Input Transition Pair (HLH or LHL)  
f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
f<sub>i</sub> = Output Frequency  
N<sub>i</sub> = Number of Outputs at f<sub>o</sub>

All currents are in milliamps and all frequencies are in megahertz.

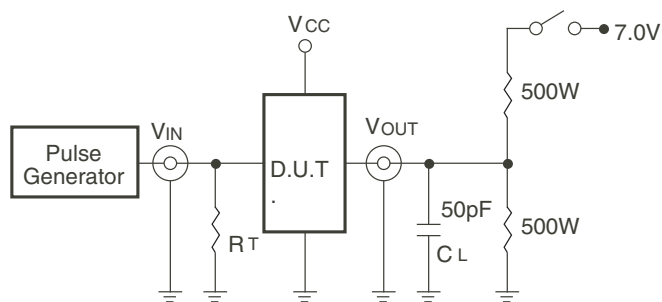
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT540AT		FCT540CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	4.8	1.5	4.3	ns
t <sub>PHL</sub>	Dx to $\overline{O}_x$						
t <sub>PZH</sub>	Output Enable Time		1.5	6.2	1.5	5.8	
t <sub>PZL</sub>	Output Disable Time		1.5	5.6	1.5	5.2	

## NOTES:

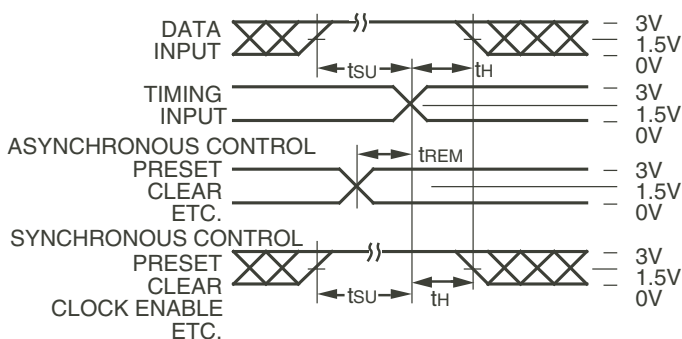
- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

## TEST CIRCUITS AND WAVEFORMS



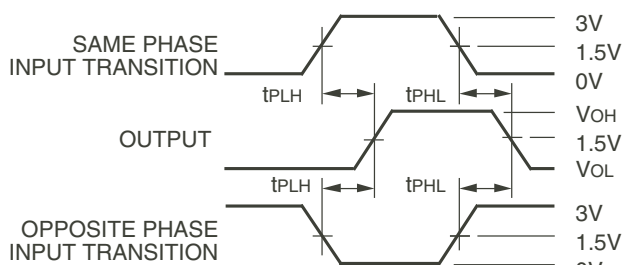
Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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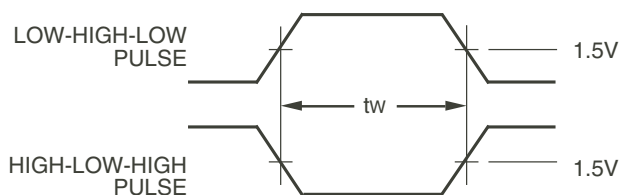
Propagation Delay

## SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

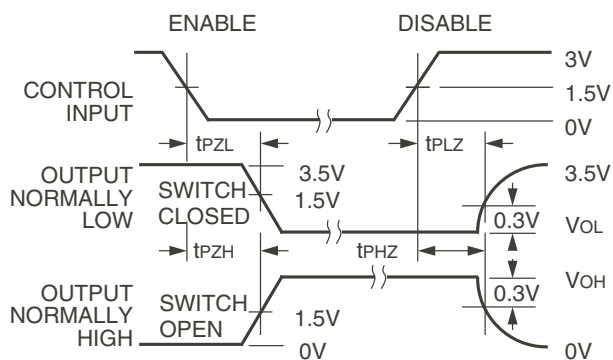
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

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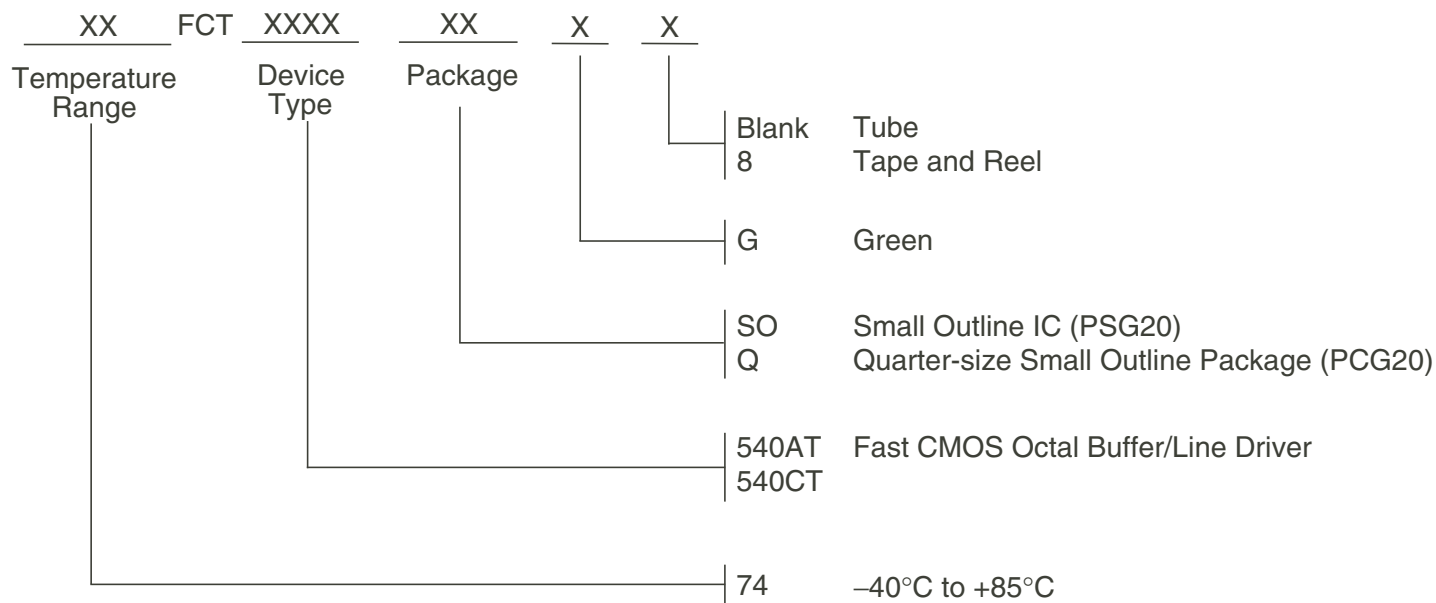
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Enable and Disable Times

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



## Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT540ATQG	PCG20	QSOP	I
	74FCT540ATQG8	PCG20	QSOP	I
	74FCT540ATSOG	PSG20	SOIC	I
	74FCT540ATSOG8	PSG20	SOIC	I
C	74FCT540CTQG	PCG20	QSOP	I
	74FCT540CTQG8	PCG20	QSOP	I
	74FCT540CTSOG	PSG20	SOIC	I
	74FCT540CTSOG8	PSG20	SOIC	I

## Datasheet Document History

10/10/2009	Pg. 6	Updated the ordering information by removing the "IDT" notation and non RoHS part.
11/28/2016	Pgs. 1,2,6	Updated datasheet obsolete SSOP package and added Tube, Tape and Reel.
05/06/2019	Pgs. 2,6	Added table under pin configuration diagram with detailed package information and orderable part information table.
02/11/2020	Pgs. 1-7	Rebranded as Renesas datasheet.

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