NBA3N011S

3.3 V Automotive Grade LVDS Driver

ON Semiconductor®

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Description

The NBA3N011S is a Low Voltage Differential Signaling (LVDS) driver for low power and high data rate applications. The device accepts LVCMOS/TTL input and translates it to LVDS and is designed to support data rates higher than 400 Mbps (200 MHz).

The driver provides low EMI with a typical output swing of 350 mV. The device can be paired with its companion single line receiver NBA3N012C or with any other LVDS receiver for high speed LVDS interface.

The LVDS output is designed as a 3.5 mA (typical) current mode driver allowing low power dissipation even at the high frequency.

NBA3N011S is offered in a 5 lead SOT23 package, shipping in 3000 pcs tape & reel.

Features

- Compatible with TIA/EIA−644A Standard
- Automotive Grade AECQ−100 Grade 1
- > 400 Mbps (200 MHz) Data Rate
- Operating Range: V_{DD} = 3.3 V ± 0.3 V
- Maximum 700 ps Differential Skew
- Maximum Propagation Delay of 1.5 ns
- Low Power Dissipation (Typical 23 mW @ 3.3 V)
- SOT23−5 Lead Package with Pinout optimized for easy PCB Layout
- ±350 mV Differential Signaling
- Power Off Protection (Outputs in Tri−state)
- Temperature Operating Range −40°C to +125°C
- These are Pb−Free Devices

Typical Applications:

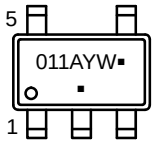
- Automotive: Head Lamp Lighting for Cars
- Telecom: Wireless, Microwave and Optical

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	I/O Type	Description
1	V_{DD}		Power Supply Pin
2	GND		Ground Pin
3	$\overline{Q}$	Output	Inverting Output Pin
4	Q	Output	Non−Inverting Output
5	IN	Input	Input Pin

SOT23−5
DT SUFFIX
CASE 527AH

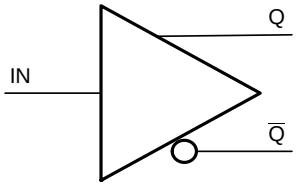
MARKING DIAGRAM



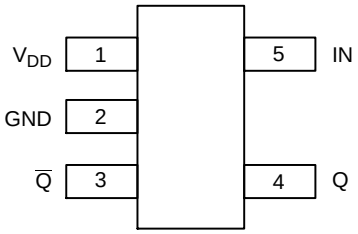
011	= Specific Device Code
A	= Assembly Code
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

LOGIC DIAGRAM



PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NBA3N011SSNT1G	SOT23−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 2. ATTRIBUTES (Note 1)

Characteristics			Value
ESD Protection	Human Body Model (JEDEC Standard 22, Method A114−E)	All Pins	≥ 8 kV
	Charge Device Model (JEDEC Standard 22, Method C101D)	All Pins	≥ 1.25 kV
Moisture Sensitivity (Note 1)			Level 1
Flammability Rating	Oxygen Index: 28 to 34		UL 94 Code V−0 A 0.125 in 28 to 34

1. For additional information, see Application Note AND8003/D

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	Supply voltage	$-0.30 \le V_{DD} \le 4.0$	V
V_{IN}	Input Voltage (IN) LVCMOS	−0.30 to (V_{DD} + 0.30)	V
V_Q	Output Voltage (Q/$\overline{Q}$) LVDS	−0.30 to +3.90	V
I_{OS}	Output Short Circuit Current LVDS	24	mA
Tj	Maximum Junction Temperature	135	°C
Tstg	Storage Temperature Range	−65 to +150	°C
θ_{JC}	Thermal resistance (Junction−to−Case) – (Note 3)	107	°C/W
θ_{JA}	Thermal resistance (Junction−to−Ambient) – (Note 3)	138.5	°C/W
T_{sol}	Lead Temperature Soldering (4 Seconds) – SOLDERRM/D	260	°C
PD	Package Power Dissipation @ 25°C − Derating of 7.22 mW/°C above 25°C	794	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. The maximum ratings applied are individual stress limit values and not valid simultaneously.
3. JEDEC standard multilayer board −2S2P (2 signal 2 power)

Table 4. DC CHARACTERISTICS V_{DD} = 3.3 V ± 0.3 V, GND = 0 V, T_A −40°C to +125°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Power Supply Current	No−Load (Pin: V_{DD}; V_{IN} = V_{DD} or GND)		5	8	mA
		RL = 100 Ω (Pin: V_{DD}; V_{IN} = V_{DD} or GND)		7	10	mA
V_{IH}	Input High Voltage	Pin: IN	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	Pin: IN	GND		0.8	V
I_{IH}	Input High Current	Pin: IN; V_{IN} = 3.3 V or 2.4 V		±2	±10	μA
I_{IL}	Input Low Current	Pin: IN; V_{IN} = GND or 0.5 V		±1	±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.6		V
C_{IN}	Input Capacitance			3		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. ELECTRICAL CHARACTERISTICS V_{DD} = 3.3 V ± 0.3 V, GND = 0 V, T_A −40°C to +125°C, Pin: Q/$\overline{Q}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$\lvert V_{OD}\rvert$	Differential Output Voltage	R_L = 100 Ω, Figures 1 & 2	250	350	450	mV
$\Delta\lvert V_{OD}\rvert$	Change in Differential Output Voltage magnitude			3	35	mV
V_{OS}	Offset Voltage	R_L = 100 Ω, Figure 1	1.125	1.220	1.375	V
ΔV_{OS}	Change in Offset Voltage magnitude		0	1	50	mV
I_{OFF}	Leakage Current − Power−off	V_Q = 3.6 V or GND, V_{DD} = 0 V		±1	±10	μA
I_{OSD}	Differential Short Circuit Output Current (Note 4)	V_{OD} = 0 V		−5	−12	mA
I_{OS}	Output Short Circuit Current (Note 4)	V_Q and $V_{\overline{Q}}$ = 0 V		−6	−24	mA
C_{OUT}	Output Capacitance			3		pF

4. − minus sign indicated only direction. Current into the device is defined as positive. I_{OS}/I_{OSD} is specified as magnitude only.

Table 6. SWITCHING CHARACTERISTICS
V_{DD} = 3.3 V ± 0.3 V, GND = 0 V, T_A −40°C to +125°C, F = 1 MHz, Z_O = 50 Ω, t_r, t_f ≤ 1 ns (10% to 90%) − (Note 5)

Symbol	Parameters	Min	Typ	Max	Unit
t_{pHLD}	High to Low Differential Propagation Delay	0.3	1.0	1.5	ns
t_{pLHD}	Low to High Differential Propagation Delay	0.3	1.1	1.5	ns
t_r	Rise Time – Transition Low to High	0.2	0.5	1.0	ns
t_f	Fall Time – Transition High to Low	0.2	0.5	1.0	ns
$t_{SKD(P)}$	Differential Pulse Skew $\lvert t_{pHLD} - t_{pLHD}\rvert$ (Note 6)	0	0.1	0.7	ns
$t_{SKD(PP)1}$	Differential Part to Part Skew – (Note 7)	0	0.2	1.0	ns
$t_{SKD(PP)2}$	Differential Part to Part Skew – (Note 8)	0	0.4	1.2	ns
f_{MAX}	Maximum Operating Frequency – (Note 9)		250		MHz

5. Test Conditions for the above − R_L = 100 Ω, C_L = 15 pF (includes Load & Jig Capacitance), Figures 3 and 4
   Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions
6. $\lvert t_{PHLD} - t_{PLHD}\rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
7. Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
8. Part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD2} is defined as |Max − Min| differential propagation delay.
9. f_{MAX} Input Conditions: t_r = t_f < 1 ns (0% to 100%), Duty Cycle 50%, 0 V to 3 V. f_{MAX} Output Conditions: V_{OD} > 250 mV, Duty Cycle = 45%/55%

PARAMETER MEASUREMENT:

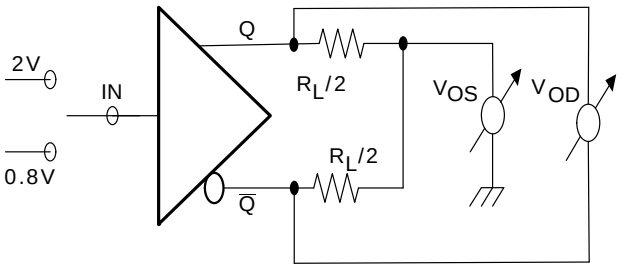


Figure 1. DC Test Circuit for Differential Driver

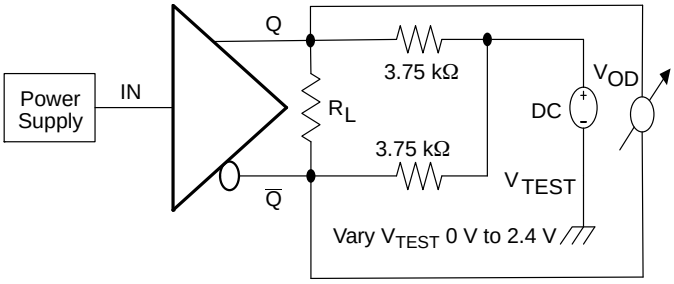


Figure 2. Full Load DC Test Circuit for Differential Driver

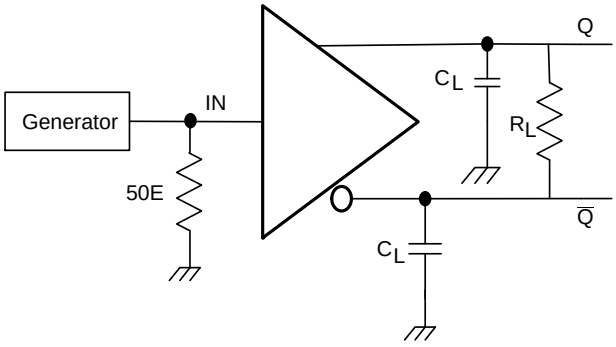


Figure 3. Propagation Delay & Transition Time Test Circuit for Differential Driver

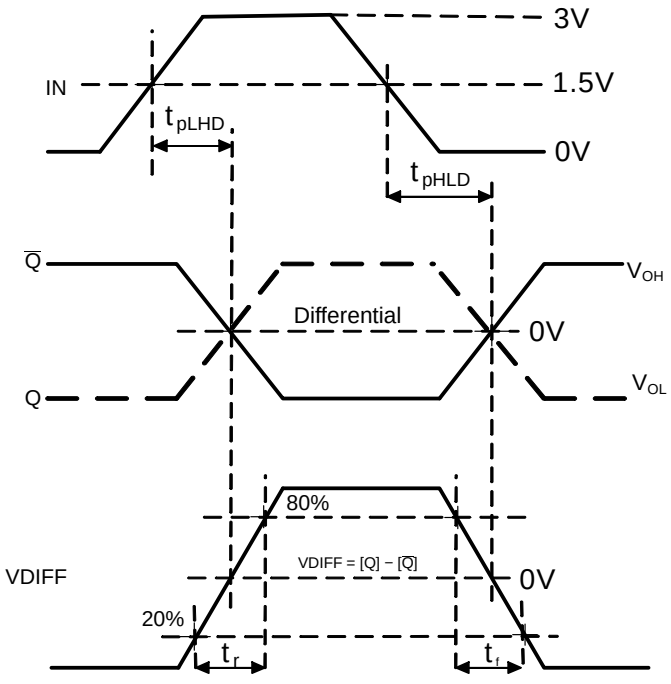


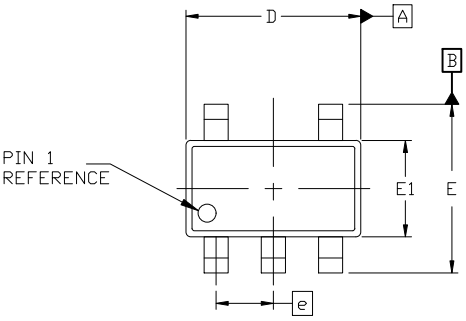
Figure 4. Propagation Delay & Transition Time Waveforms for Differential Driver

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

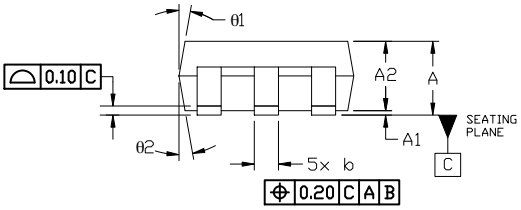
ON Semiconductor®

SOT−23, 5 Lead
CASE 527AH
ISSUE A

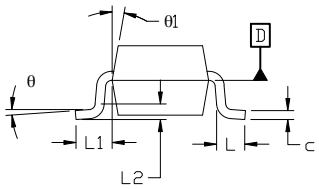
DATE 09 JUN 2021



TOP VIEW



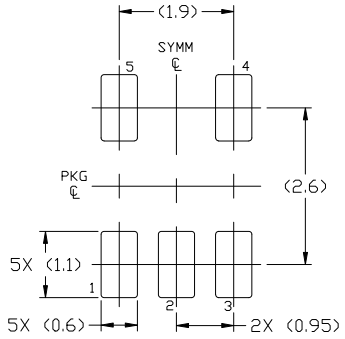
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

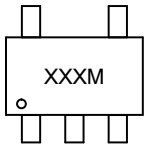
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−23, 5 LEAD**	**PAGE 1 OF 1**

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