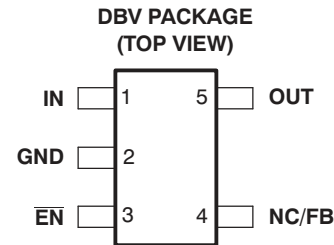


ULTRALOW-POWER 50-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- Qualified for Automotive Applications
- 50-mA Low-Dropout Regulator
- Available in a 3.3-V Fixed-Output Voltage
- Only 17- μ A Quiescent Current at 50 mA
- 1- μ A Quiescent Current in Standby Mode
- Dropout Voltage Typically 35 mV at 50 mA
- –40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



DESCRIPTION

The TPS77033 low-dropout (LDO) voltage regulator offers the benefits of low dropout voltage, ultralow-power operation, and miniaturized packaging. This regulator features low dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a 5-terminal small-outline integrated-circuit SOT-23 package, the TPS77033 series device is ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is low and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (28 μ A maximum) and is stable over the entire range of output load current (0 mA to 50 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-dropout voltage feature and ultralow-power operation result in a significant increase in system battery operating life.

The TPS77033 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μ A typical at $T_J = 25^\circ\text{C}$. The TPS77033 is offered in a 3.3-V fixed-voltage versions.

AVAILABLE OPTIONS⁽¹⁾

T_J	VOLTAGE	PACKAGE ⁽²⁾	PART NUMBER ⁽³⁾	SYMBOL
–40°C to 125°C	3.3 V	SOT-23 – DBV	TPS77033QDBVRQ1	PCXI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

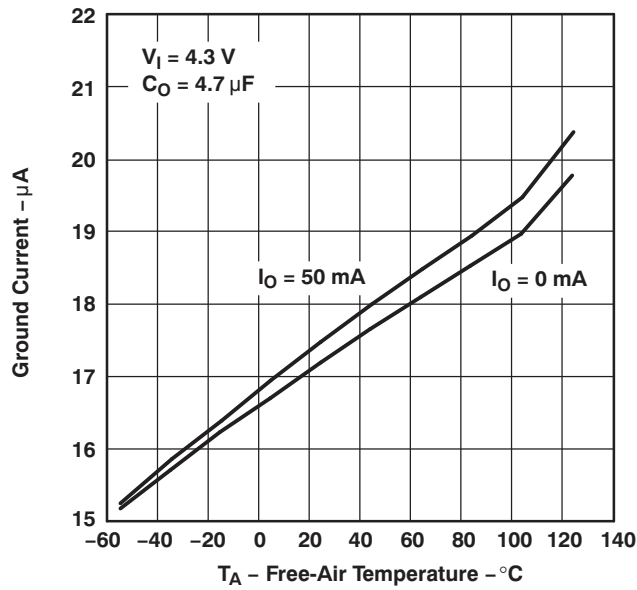
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBVR indicates tape and reel of 3000 parts.

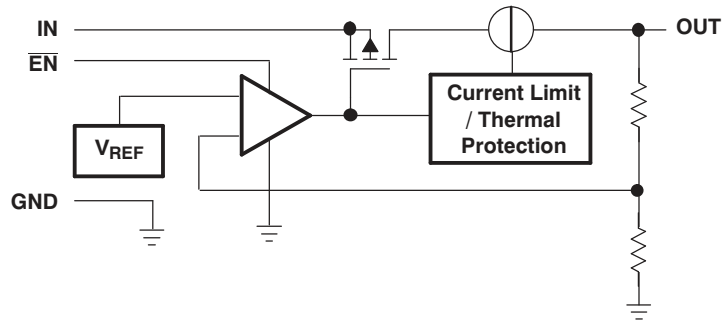


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**GROUND CURRENT
vs
FREE-AIR TEMPERATURE**



FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	2		Ground
$\overline{\text{EN}}$	3	I	Enable input
IN	1	I	Input supply voltage
NC	4		No connection (fixed options only)
OUT	5	O	Regulated output voltage

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		UNIT	
Input voltage range ⁽²⁾		–0.3 V to 13.5 V	
Voltage range at $\overline{\text{EN}}$		–0.3 V to $V_I + 0.3$ V	
Voltage on OUT, FB		7 V	
Peak output current		Internally limited	
ESD rating, HBM		2 kV	
Continuous total power dissipation		See Dissipation Rating Table	
T_J	Operating virtual junction temperature range	–40°C to 150°C	
T_{stg}	Storage temperature range	–65°C to 150°C	
ESD classification per AEC Q100		Human-Body Model (HBM)	4 kV (H2)
		Machine Model (MM)	300 V (M3)
		Charged-Device Model (CDM)	1500 V (C5)

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

Dissipation Ratings

BOARD	PACKAGE	$R_{\theta\text{JC}}$	$R_{\theta\text{JA}}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Low K ⁽¹⁾	DBV	65.8°C/W	259°C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K ⁽²⁾	DBV	65.8°C/W	180°C/W	5.6 mW/°C	555 mW	305 mW	222 mW

- (1) The JEDEC Low K (1s) board design used to derive this data was a 3-in × 3-in, two-layer board with 2-oz copper traces on top of the board.
- (2) The JEDEC High K (2s2p) board design used to derive this data was a 3-in × 3-in, multilayer board with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_I	Input voltage ⁽¹⁾	$3.3 + V_{\text{DO}}$	10	V
V_O	Output voltage	1.2	5.5	V
I_O	Continuous output current ⁽²⁾	0	50	mA
T_J	Operating junction temperature	–40	125	°C

- (1) To calculate the minimum input voltage for your maximum output current, use the following formula:
 $V_I(\text{min}) = V_O(\text{max}) + V_{\text{DO}}(\text{max load})$
- (2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

Electrical Characteristics

over recommended operating free-air temperature range, $V_I = V_O(\text{typ}) + 1 \text{ V}$, $I_O = 50 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 50 mA load) ⁽¹⁾	$T_J = 25^\circ\text{C}$, $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$		3.3		V
	$T_J = -40^\circ\text{C}$ to 125°C , $4.3 \text{ V} < V_{\text{IN}} < 10 \text{ V}$	3.201		3.399	
Quiescent current (GND current) ⁽¹⁾	$\overline{\text{EN}} = 0 \text{ V}$, $0 \text{ mA} < I_O < 50 \text{ mA}$, $T_J = 25^\circ\text{C}$		17		μA
	$\overline{\text{EN}} = 0 \text{ V}$, $I_O = 50 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			28	
Output voltage line regulation ($\Delta V_O/V_O$) ⁽¹⁾⁽²⁾	$V_O + 1 \text{ V} < V_I < 10 \text{ V}$, $T_J = 25^\circ\text{C}$		0.04		%V
	$V_O + 1 \text{ V} < V_I < 10 \text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C			0.1	
Load regulation	$\overline{\text{EN}} = 0 \text{ V}$, $I_O = 0$ to 50 mA , $T_J = 25^\circ\text{C}$		8		mV
Output noise voltage	$\text{BW} = 300 \text{ Hz}$ to 50 kHz , $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$		190		μV_{rms}
Output current limit	$V_O = 0 \text{ V}$ ⁽¹⁾		350	750	mA
Standby current	$\overline{\text{EN}} = V_I$, $2.7 < V_I < 10 \text{ V}$		1		μA
	$T_J = -40^\circ\text{C}$ to 125°C			2	
High-level enable input voltage	$2.7 \text{ V} < V_I < 10 \text{ V}$	1.7			V
Low-level enable input voltage	$2.7 \text{ V} < V_I < 10 \text{ V}$			0.9	V
Power-supply ripple rejection	$f = 1 \text{ kHz}$, $C_O = 10 \mu\text{F}$, $T_J = 25^\circ\text{C}$ ⁽¹⁾		60		dB
Input current ($\overline{\text{EN}}$)	$\overline{\text{EN}} = 0 \text{ V}$	-1	0	1	μA
	$\overline{\text{EN}} = V_I$	-1		1	
Dropout voltage ⁽³⁾	$I_O = 50 \text{ mA}$, $T_J = 25^\circ\text{C}$		48		mV
	$I_O = 50 \text{ mA}$, $T_J = -40^\circ\text{C}$ to 125°C			100	

(1) Minimum IN operating voltage is 2.7 V or $V_O(\text{typ}) + 1 \text{ V}$, whichever is greater. Maximum IN voltage 10 V, minimum output current 10 μA , maximum output current 50 mA.

(2) If $V_O \leq 1.8 \text{ V}$ then $V_{\text{Imin}} = 2.7 \text{ V}$, $V_{\text{Imax}} = 10 \text{ V}$:

$$\text{Line Regulation (mV)} = (\%V) \times \frac{V_O(V_{\text{Imax}} - 2.7 \text{ V})}{100} \times 1000$$
 If $V_O \geq 2.5 \text{ V}$, then $V_{\text{Imin}} = V_O + 1 \text{ V}$, $V_{\text{Imax}} = 10 \text{ V}$:

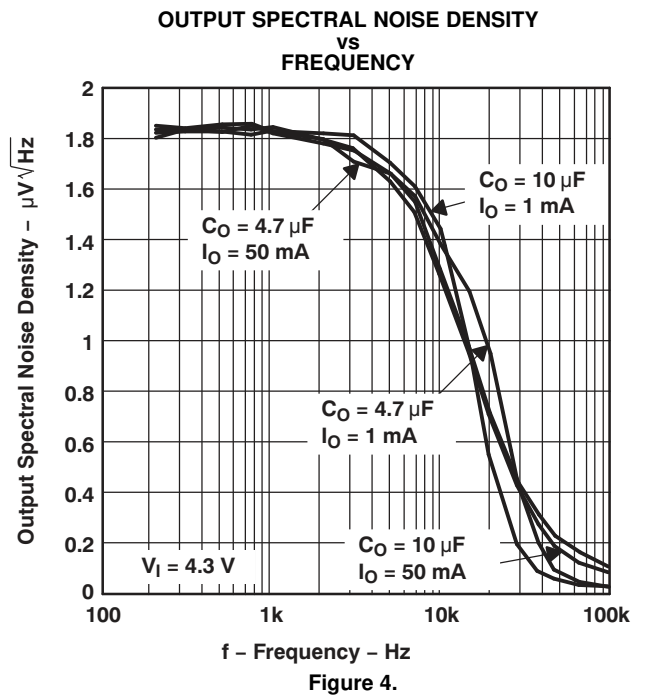
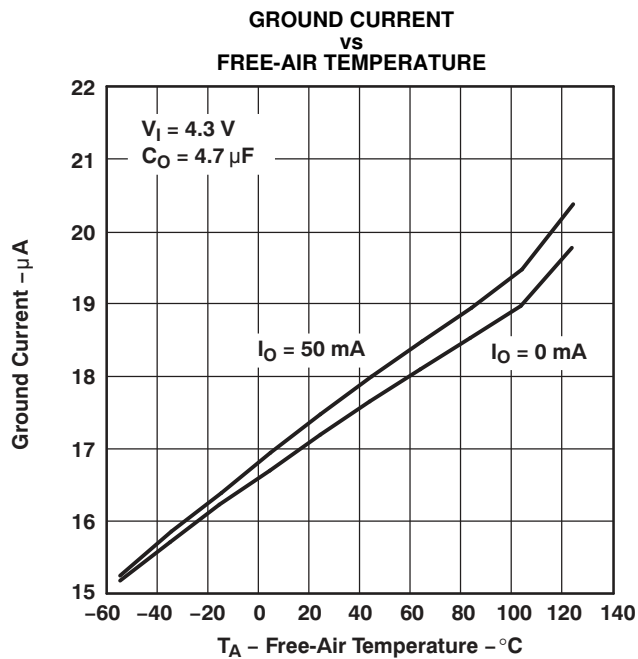
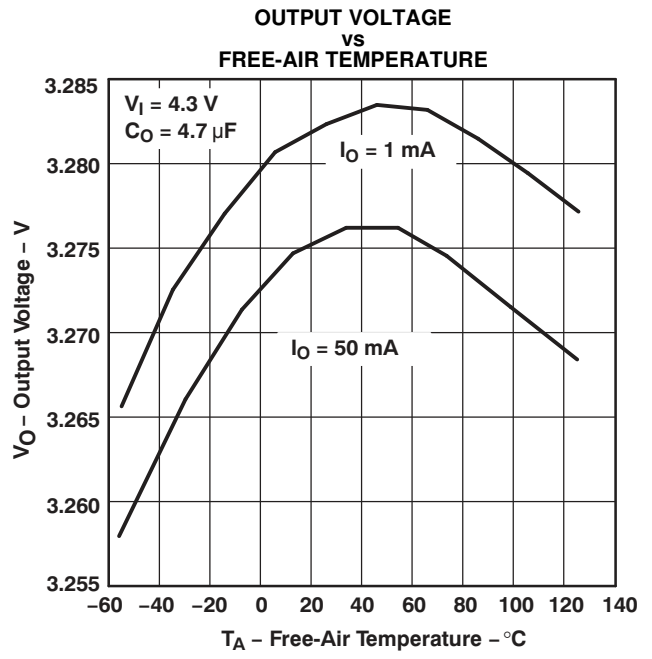
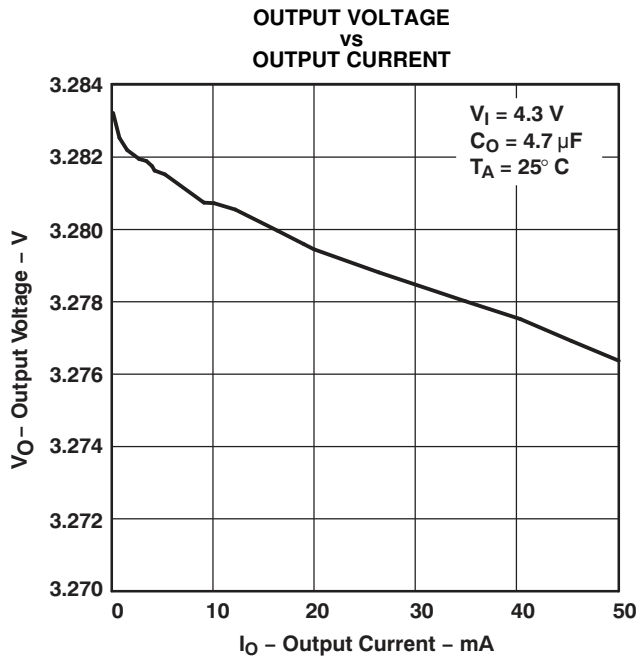
$$\text{Line Regulation (mV)} = (\%V) \times \frac{V_O(V_{\text{Imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

(3) IN voltage equals $V_O(\text{typ}) - 100 \text{ mV}$

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
V_O	Output voltage	vs Output current	1
		vs Free-air temperature	2, 3
	Output spectral noise density	vs Frequency	4
Z_O	Output impedance	vs Frequency	5
V_{DO}	Dropout voltage	vs Free-air temperature	6
	Ripple rejection	vs Frequency	7
	LDO startup time		8
	Line transient response		9
	Load transient response		10
	Equivalent series resistance (ESR)	vs Output current	11, 13
		vs Added ceramic capacitance	12, 14



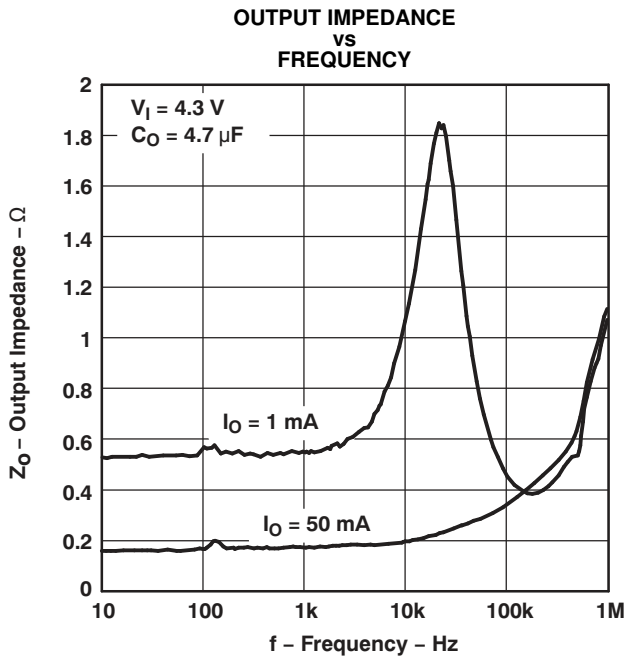


Figure 5.

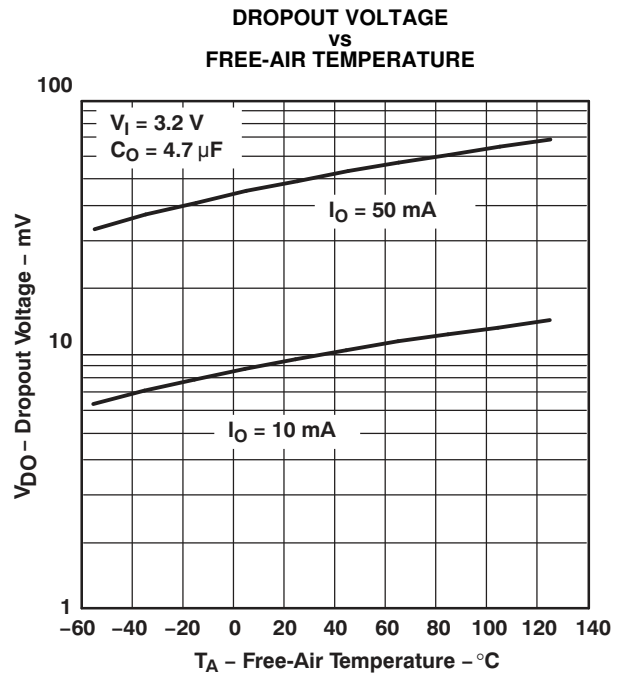


Figure 6.

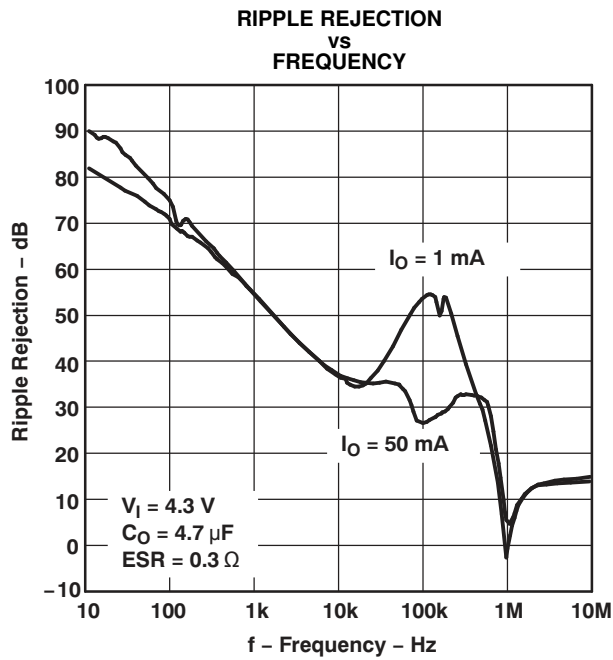


Figure 7.

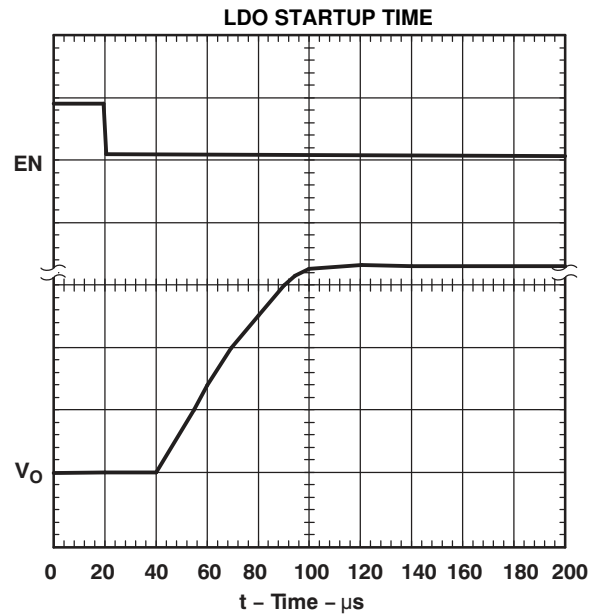


Figure 8.

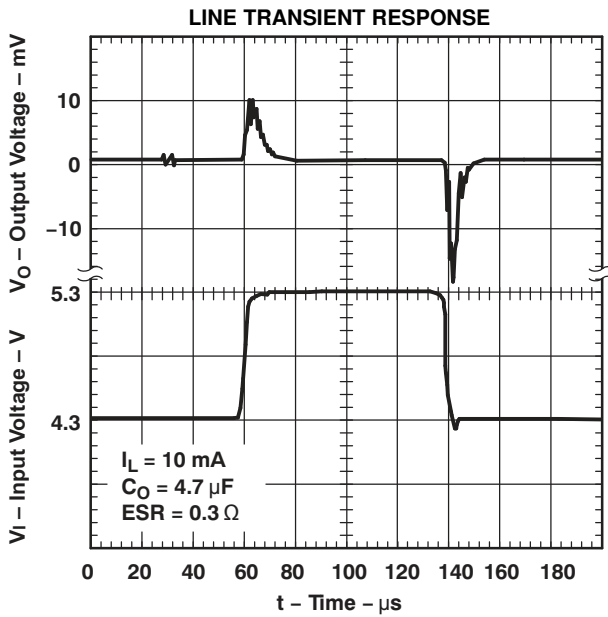


Figure 9.

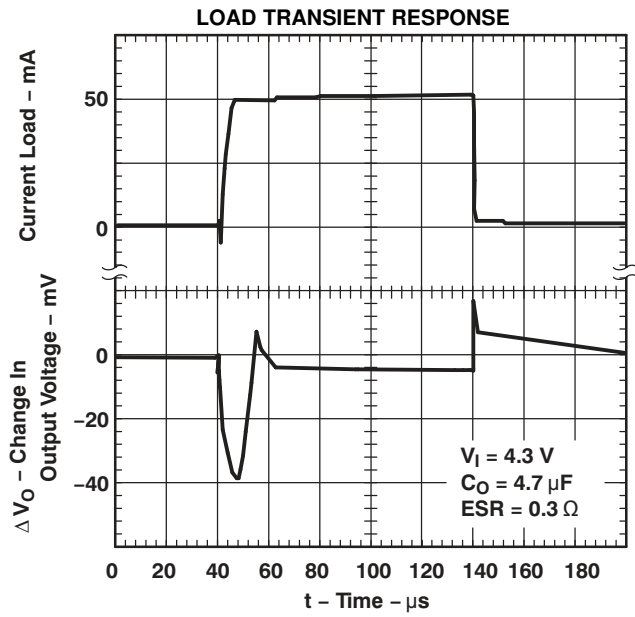


Figure 10.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

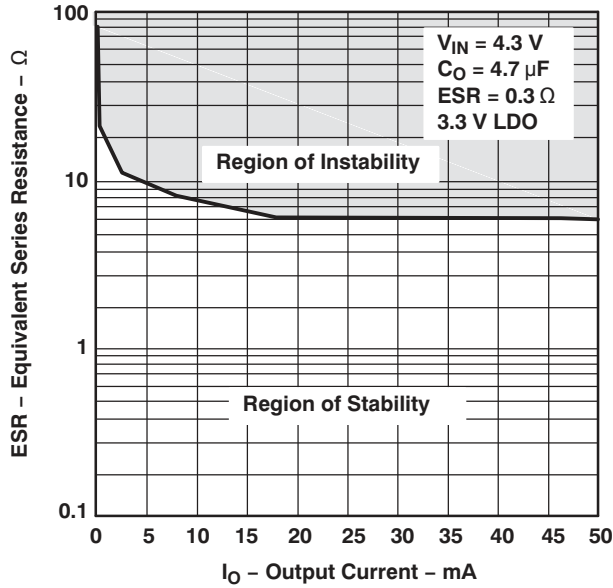


Figure 11.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
ADDED CERAMIC CAPACITANCE

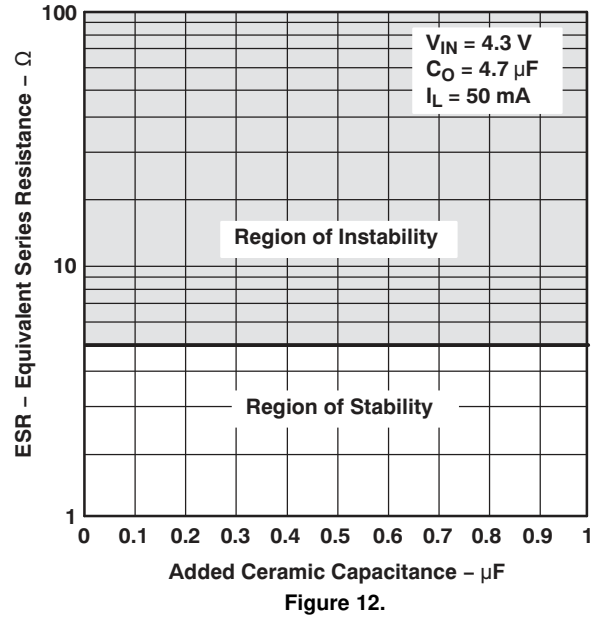
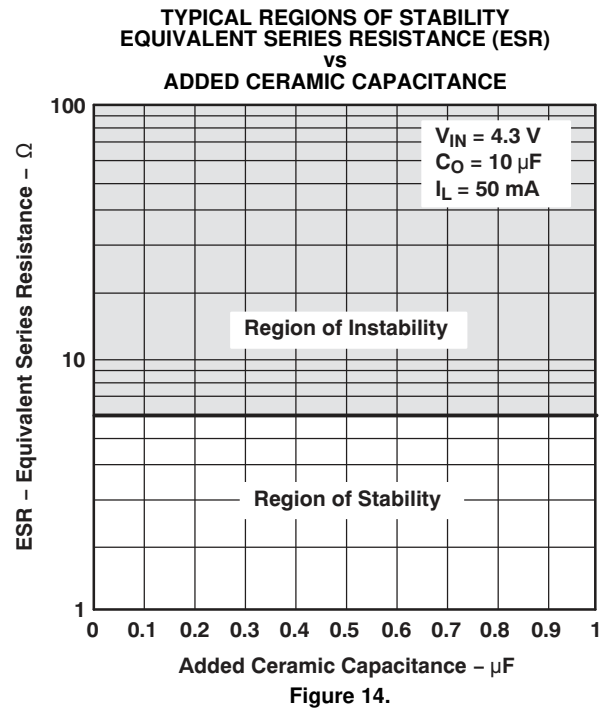
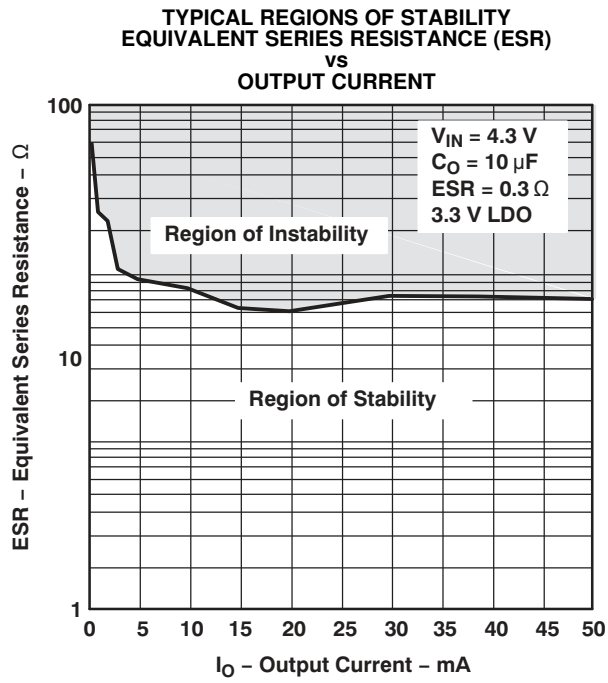


Figure 12.



APPLICATION INFORMATION

The TPS77033 low-dropout (LDO) regulator has been optimized for use in battery-operated equipment. They feature extremely low-dropout voltages, low quiescent current (17 μA nominally), and enable inputs to reduce supply currents to less than 1 μA when the regulators are turned off.

Device Operation

The TPS77033 uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device and, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS77033 essentially is constant from no load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 350 mA; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above approximately 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high-temperature trip point. The PMOS pass element includes a back-gate diode that conducts reverse current when the input voltage level drops below the output voltage level.

A voltage of 1.7 V or greater on the $\overline{\text{EN}}$ input disables the TPS77033 internal circuitry, reducing the supply current to 1 μA . A voltage of less than 0.9 V on the $\overline{\text{EN}}$ input enables the TPS77033 and enables normal operation to resume. The $\overline{\text{EN}}$ input does not include any deliberate hysteresis, and it exhibits an actual switching threshold of approximately 1.5 V.

A typical application circuit is shown in [Figure 15](#).

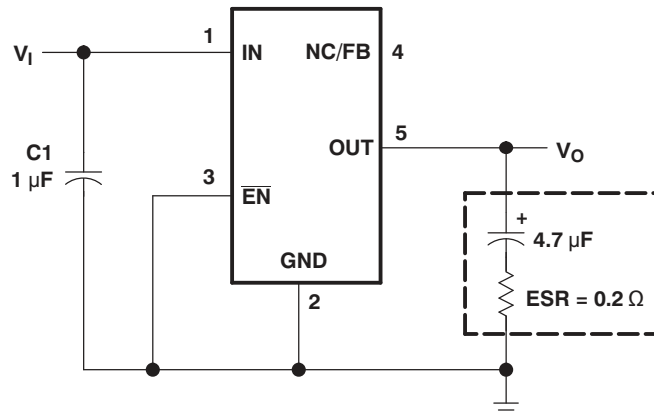


Figure 15. Typical Application Circuit – Fixed-Voltage Option

External Capacitor Requirements

Although not required, a 0.047- μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS77033, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated, and the device is located several inches from the power source.

Like all low-dropout regulators, the TPS77033 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μ F. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω to ensure stability. Capacitor values larger than 4.7 μ F are acceptable and allow the use of smaller ESR values. Capacitances less than 4.7 μ F are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements previously described. Most of the commercially available 4.7- μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low-value series resistor to ensure stability.

CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR ⁽¹⁾	SIZE (H × L × W) ⁽¹⁾
T494B475K016AS	KEMET	4.7 μ F	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 μ F	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 μ F	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 μ F	0.6 Ω	2.6 × 6.0 × 3.2

(1) Size is in mm. ESR is maximum resistance in ohms at 100 kHz and $T_A = 25^\circ\text{C}$. Contact the manufacturer for minimum ESR values.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(\text{max})}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(\text{max})}$.

The maximum power dissipation limit is determined using [Equation 1](#):

$$P_{D(\text{max})} = \frac{T_{J\text{max}} - T_A}{R_{\theta\text{JA}}} \quad (1)$$

where

$T_{J\text{max}}$ = maximum allowable junction temperature

$R_{\theta\text{JA}}$ = junction-to-ambient thermal resistance for the package (see *Dissipation Rating*)

T_A = ambient temperature

The regulator dissipation is calculated using [Equation 2](#):

$$P_D = (V_I - V_O) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Regulator Protection

The TPS77033 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS77033 features internal current limiting and thermal protection. During normal operation, the TPS77033 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS77033QDBVRQ1	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	PCXI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS77033-Q1 :

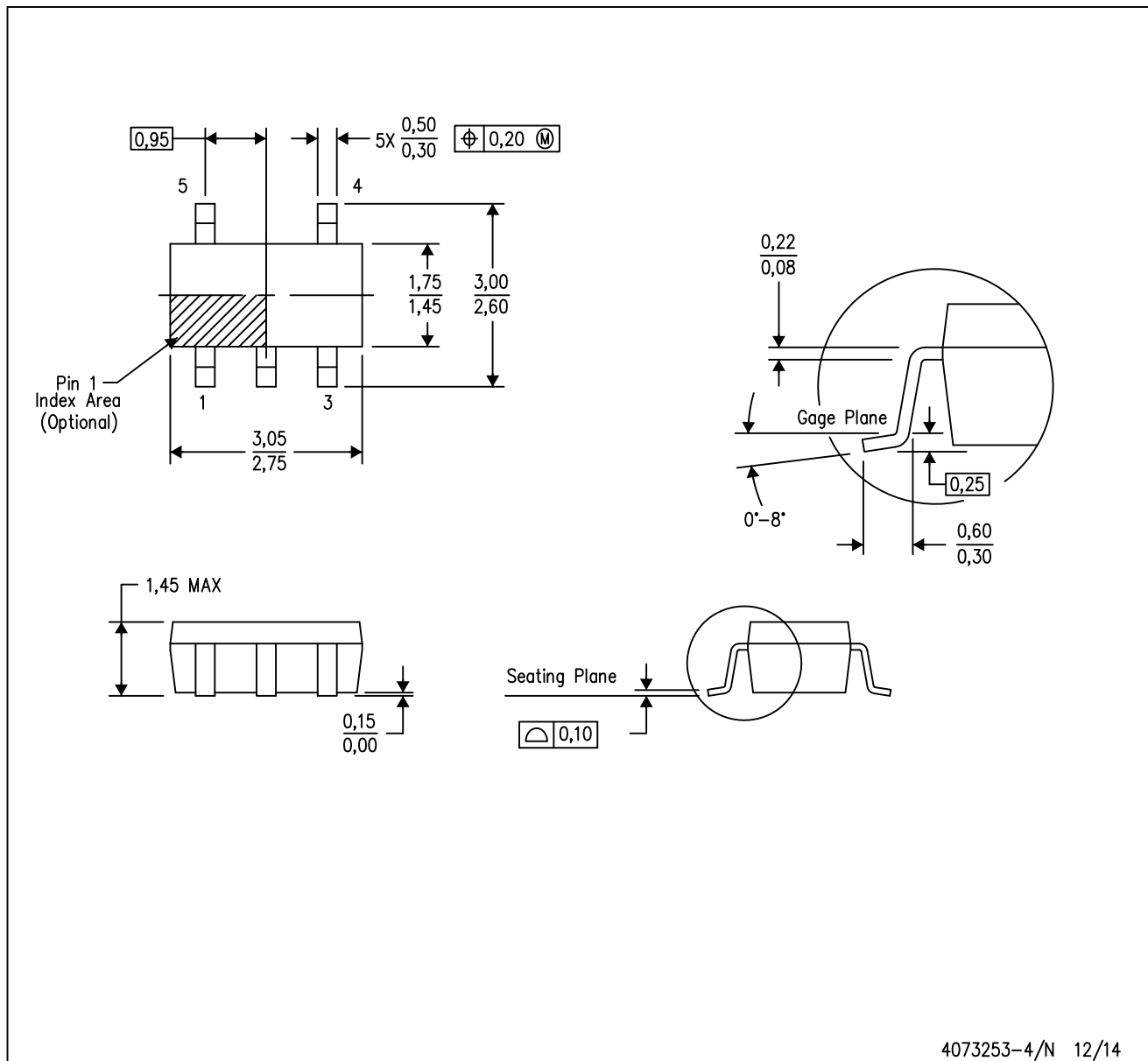
- Catalog: [TPS77033](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

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