May 2007

DM74ALS03B
Quad 2-Input NAND Gate with Open Collector Outputs

Features

- Switching specifications at 50pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

where:

N_1 (I_{OH}) = total maximum output HIGH current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input HIGH current for all inputs tied to pull-up resistor

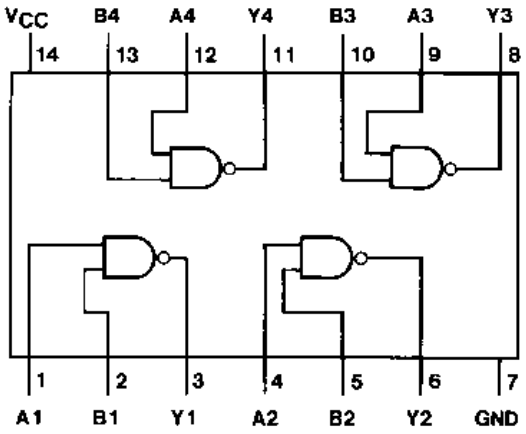
N_3 (I_{IL}) = total maximum input LOW current for all inputs tied to pull-up resistor

Ordering Information

Order Number	Package Number	Package Description
DM74ALS03BM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

Connection Diagram



Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	7V
V_I	Input Voltage	7V
	HIGH Level Ouutput	7V
T_A	Operating Free Air Temperature Range	0°C to +70°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
θ_{JA}	Typical Thermal Resistance	116.0°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Nom.	Max.	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
V_{OH}	HIGH Level Output Voltage			5.5	V
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = –18mA				–1.5	V
I_{OH}	HIGH Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	µA
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V	I_{OL} =4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				–0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs HIGH		0.43	0.85	mA
			Outputs LOW		1.62	3	

Switching Characteristics

Over recommended operating free air temperature range.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2kΩ, C_L = 50pF	20	50	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output		3	13	ns

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

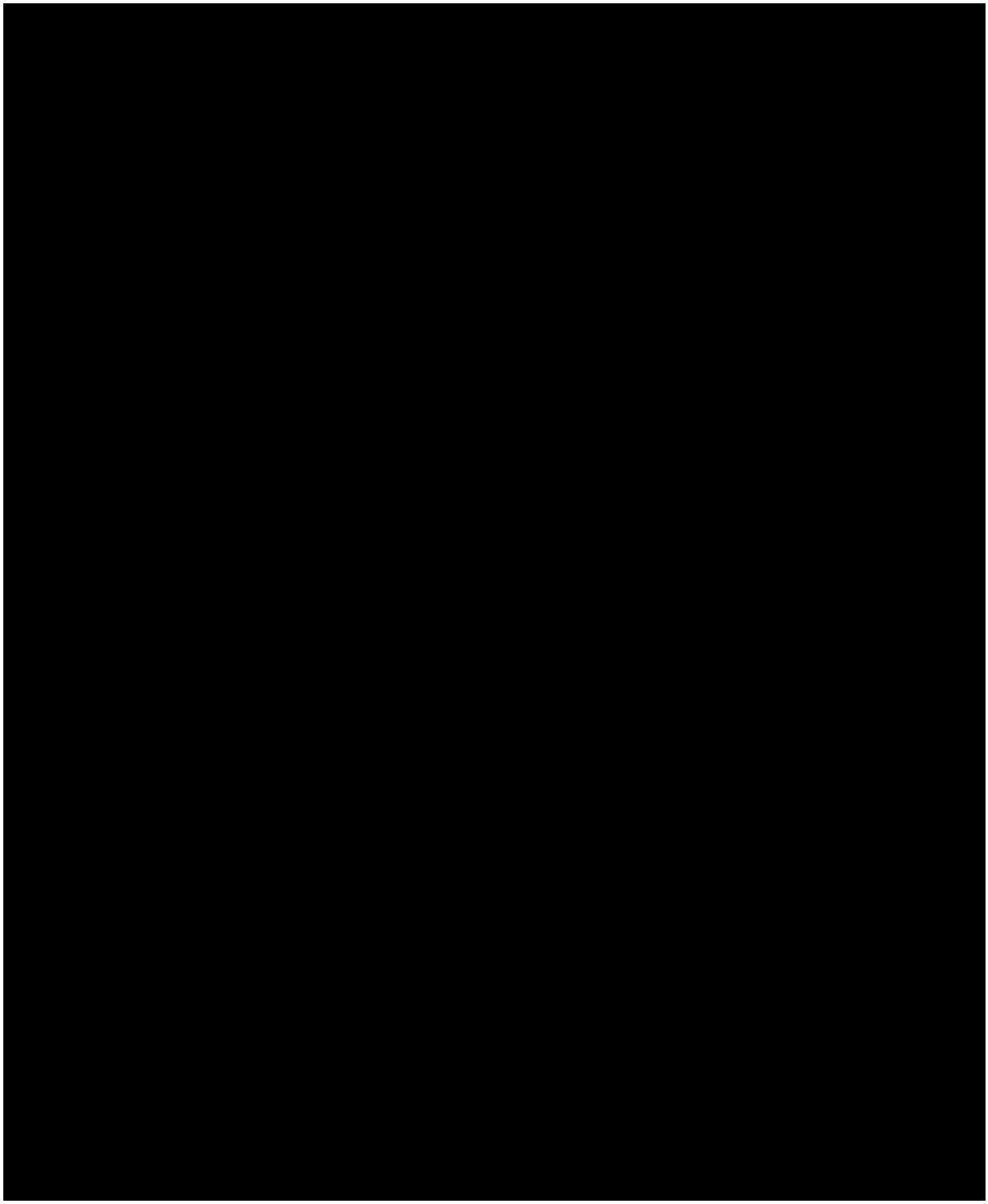


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A