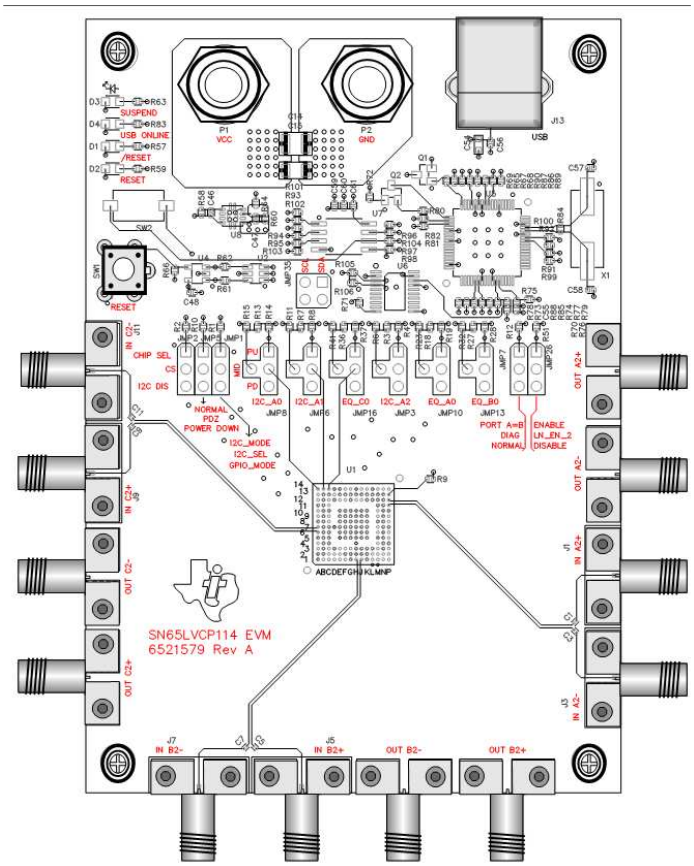
SN65LVCP114 Evaluation Module (EVM)

The Texas Instruments SN65LVCP114 Evaluation Module (EVM) board is used to evaluate the SN65LVCP114, 14.2Gbps Quad 1:2-2:1 Mux, Linear-Redriver with Signal Conditioning. This document provides guidance on the device's proper use by showing some operating configurations and test modes. The EVM board schematic and layout information are also provided for the customer. Information in this guide assists the customer in choosing the optimal design methods and materials in designing a complete system.



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WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices, pursuant to subpart J, part 15 of FCC rules. These rules are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user, at their own expense, must take whatever measures are necessary to correct this interference.

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1 Introduction

The Texas Instruments (TI) SN65LVCP114 is a 14.2Gbps asynchronous, protocol-agnostic, low-latency QUAD 1:2-2:1 mux, linear-redriver switch with signal conditioning. The device linearly compensates for channel loss in backplane and active-cable applications. The architecture of the SN65LVCP114 crosspoint switch is designed to work effectively with ASIC or FPGA products implementing digital equalization by using decision feedback equalizer (DFE) technology. SN65LVCP114 mux, linear-redriver switch preserves the integrity (composition) of the received signal ensuring optimum DFE and system performance. SN65LVCP114 provides low-power mux, linear-redriver solution while at the same time extending the effectiveness of DFE.

2 EVM PCB and High-Speed Design Considerations

The EVM and the contents of this guide are used to evaluate device parameters in addition to helping with high-speed board layout. As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50 Ω single-ended or 100 Ω differential impedance for both the low and high-speed differential serial and clock connections. The use of vias is minimized and, when necessary, are designed to minimize impedance discontinuities along the transmission line. Care was taken to control trace length mismatch (board skew) to less than ±0.1 MIL.

The board layout is designed and optimized to support high-speed operation. Understanding impedance control and transmission line effects is crucial when designing high-speed boards. Some of the advanced features offered by this board include:

- SN65LVCP114 printed circuit board (PCB) designed for optimal high-speed signal integrity using Rogers Material for the outer signal layers and FR-4 for the inner layers. All Gigabit signals are routed over the Rogers Material for minimal signal loss.
- SMA and header fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- On-board capacitors provide AC coupling of high-speed transmit and receive signals.

3 SN65LVCP114 EVM Kit Contents

The SN65LVCP114 EVM kit contains the following:

- SN65LVCP114 EVM board
- SN65LVCP114 EVM User’s Guide (this document)
- SN65LVCP114 datasheet
- CD-ROM containing the graphical user interface (GUI) software

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4 SN65LVCP114 EVM Board Configuration

The SN65LVCP114 is operated from a 2.5-V or 3.3-V power supply with a 1.0 A or greater current rating. The SN65LVCP114 has three ports; each port has four lanes. The switch logic of the SN65LVCP114 is implemented to support 2:1 MUX per lane, 1:2 DEMUX per lane, and independent lane switching. Each of the ports are independently programmed for receive equalization. The device also supports loopback on all three ports.

The EVM provides SMA connections for one lane per port for device evaluation with full configuration control of the device through I2C using the SN65LVCP114 GUI provided. Limited configuration control is available through GPIO. Refer to Section 7 for more details.

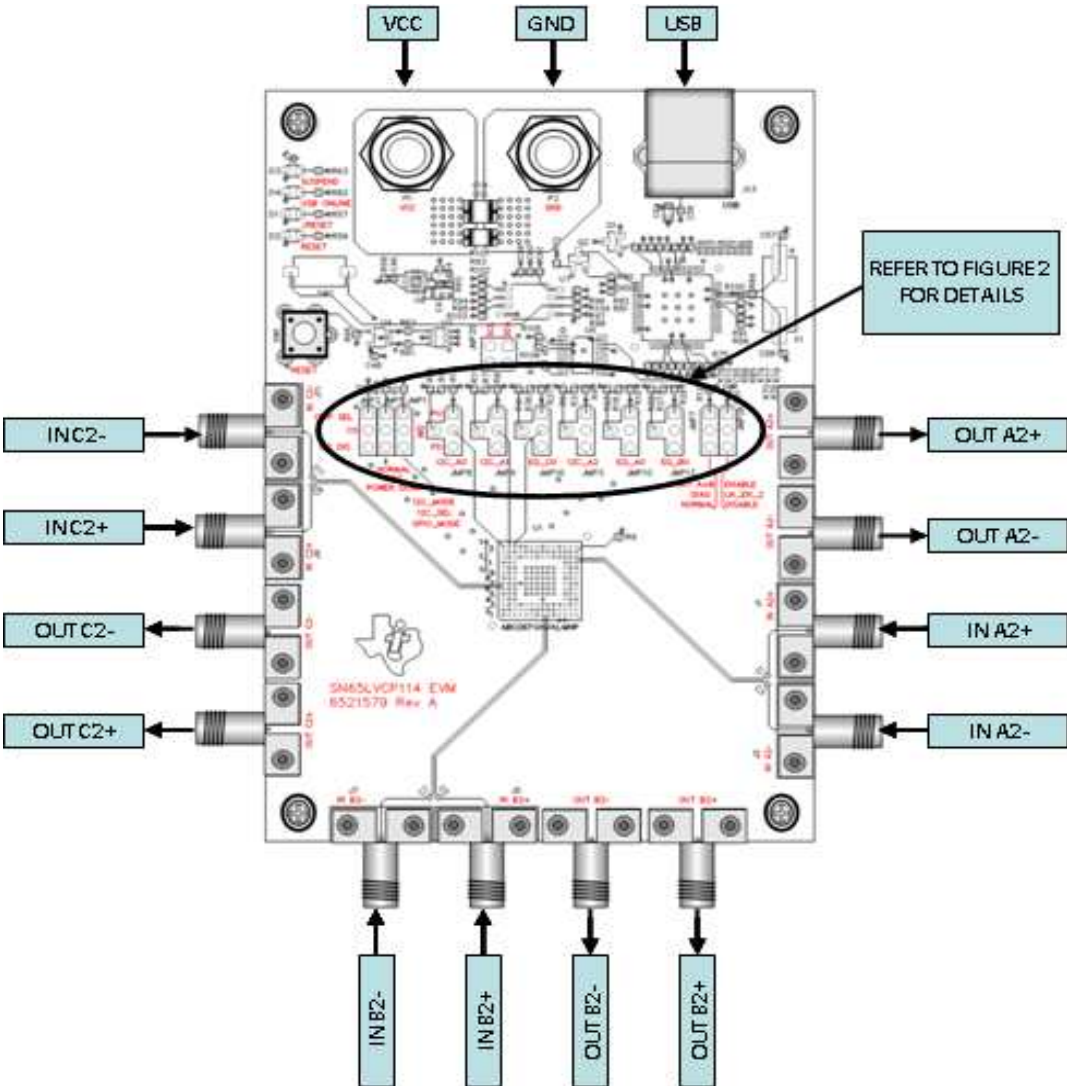

Figure 1. SN65LVCP114 EVM

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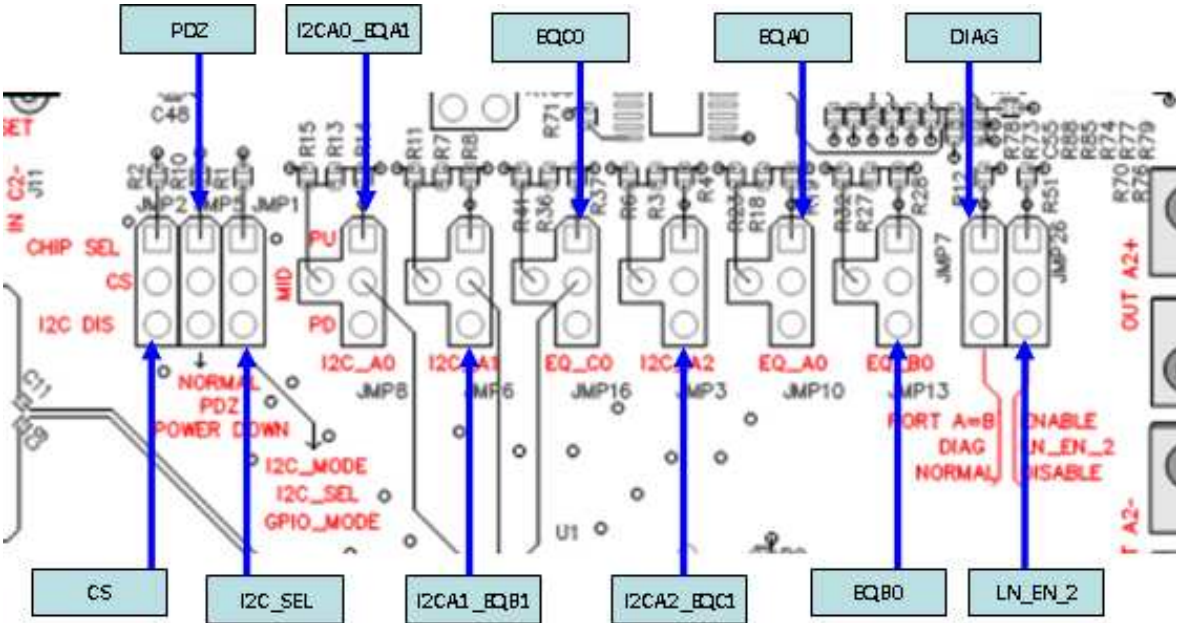

Figure 2. SN65LVCP114 EVM Jumper Description

5 Test Setup

The SN65LVCP114 EVM gives the developer two control interface options for operation, I2C or GPIO mode. Input and Output differential pairs are available through edge-launch SMAs with approximately 2.5 inches of trace with Rogers Low–Dielectric material with 0.1 µF AC Coupling capacitors. Power to the device, VCC, is applied using banana jacks (P1, P2). The USB-to-I2C circuitry on the board uses power from the USB 5-V signal.

Table 1. SN65LVCP114 EVM Pin and Jumper Functionality

Ref Des	Symbol	Description	
		GPIO mode	I2C mode
J1, J3	AINP2, AINN2	Differential input, lane 2, Fabric switch A side	
J2, J4	AOUTP2, AOUTN2	Differential output, lane 2, Fabric switch A side	
J5, J7	BINP2, BINN2	Differential input, lane 2, Fabric switch B side	
J6, J8	BOUTP2, BOUTN2	Differential output, lane 2, Fabric switch B side	
J9, J11	CINP2, CINN2	Differential input, lane 2, Fabric switch C side	
J10, J12	COUTP2, COUTN2	Differential output, lane 2, Fabric switch C side	
P1	VCC	Banana jack, positive power supply connection	
P2	GND	Banana jack, ground power supply connection	
J13	USB	USB cable connection	
JMP2	CS	Don't Care	High, acts as Chip Select Low, disables the I2C interface
JMP5	PDZ	High, normal operation Low, powers down the device, inputs off and outputs disabled, resets the I2C	
JMP1	I2C_SEL	Configures the device in I2C or GPIO mode of operation High, enables I2C mode Low, enables GPIO mode	
JMP8	I2C_A0_EQA1	3 level control for EQ gain of port A	I2C Address
JMP6	I2C_A1_EQB1	3 level control for EQ gain of port B	I2C Address
JMP16	EQ_C0	3 level control for EQ gain of port C	Don't care
JMP3	I2C_A2_EQC1	3 level control for EQ gain of port C	I2C Address

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Table 1. SN65LVCP114 EVM Pin and Jumper Functionality (continued)

Ref Des	Symbol	Description	
		GPIO mode	I2C mode
JMP10	EQ_A0	3 level control for EQ gain of port A	Don't care
JMP13	EQ_B0	3 level control for EQ gain of port B	Don't care
JMP7	DIAG	High, enables the same data on the line side (Port C) to be output on both fabric side ports (Port A & B) Low, normal operation	Don't care
JMP26	LN_EN_2	High, enables lane 2 of ports A, B & C	Don't care

6 I2C Mode

The I2C mode is implemented using the SN65LVCP114 user interface software included in the CD-ROM with the EVM. Refer to the SN65LVCP114 EVM GUI User's Guide for details on how to use the GUI. Table 2 shows the appropriate jumper settings on the EVM to configure the device in I2C mode. Refer to Appendix A for jumper shunt settings.

See the SN65LVCP114 Datasheet for a detailed description of the register map.

Table 2. SN65LVCP114 EVM I2C Mode Settings

Ref Des	Symbol	I2C Mode Pin Settings
JMP8	I2C_A0_EQA1	Low
JMP6	I2C_A1_EQB1	Low
JMP3	I2C_A2_EQC1	Low
JMP5	PDZ	High, normal operation Low, powers down the device, inputs off and outputs disabled, resets the I2C
JMP1	I2C_SEL	Configures the device in I2C or GPIO mode of operation High, enables I2C mode

7 GPIO Mode

Although it is recommended to use the EVM in I2C mode so that the user has full control of the device some control of the SN65LVCP114 device is available on the EVM through GPIO mode. Refer to Table 3 for the different jumper and EQ settings. Table 4 shows the appropriate jumper and default settings on the EVM to configure and control the device in GPIO mode. Refer to Appendix A for jumper shunt settings.

See the SN65LVCP114 Datasheet for a detailed description of the control signals.

Table 3. SN65LVCP114 EVM Jumper and EQ Settings

EQ[x]0	EQ[x]1	Peaking in dB
0	0	1.3
0	HiZ	2
0	1	3.6
HiZ	0	5
HiZ	HiZ	6.5
HiZ	1	8.3
1	0	10
1	HiZ	11.9
1	1	13.9

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Table 4. SN65LVCP114 EVM GPIO Mode Settings

Ref Des	Symbol	GPIO Mode Pin Description
JMP8	I2C_A0_EQA1	3 level control for EQ gain of port A
JMP6	I2C_A1_EQB1	3 level control for EQ gain of port B
JMP3	I2C_A2_EQC1	3 level control for EQ gain of port C
JMP10	EQ_A0	3 level control for EQ gain of port A
JMP13	EQ_B0	3 level control for EQ gain of port B
JMP16	EQ_C0	3 level control for EQ gain of port C
	LPA	Default setting, Loopback disabled
	LPB	Default setting, Loopback disabled
	LPC	Default setting, Loopback disabled
	SEL0	Default setting, port B is selected on Lane 0
	SEL1	Default setting, port B is selected on Lane 1
	SEL2	Default setting, port B is selected on Lane 2
	SEL3	Default setting, port B is selected on Lane 3
JMP2	CS	Don't Care
JMP5	PDZ	High, normal operation Low, powers down the device, inputs off and outputs disabled, resets the I2C
JMP7	DIAG	High, enables the same data on line side (Port C) to be output on both fabric side ports (Port A & B) Low, normal operation
	LN_EN_0	Default setting, lane 0 of ports A, B & C are disabled
	LN_EN_1	Default setting, lane 1 of ports A, B & C are disabled
JMP26	LN_EN_2	High, enables lane 2 of ports A, B & C Low, disables lane 0 of ports A, B & C
	LN_EN_3	Default setting, lane 3 of ports A, B & C are disabled
	DIS_AGC_A	Default setting, AGC loop enable
	DIS_AGC_B	Default setting, AGC loop enable
	DIS_AGC_C	Default setting, AGC loop enable
	VOD_A	Default setting; VOD output range = 600 mV
	VOD_B	Default setting; VOD output range = 600 mV
	VOD_C	Default setting; VOD output range = 600 mV
	GAIN_A	Default setting; Receiver Gain = 0.5
	GAIN_B	Default setting; Receiver Gain = 0.5
	GAIN_C	Default setting; Receiver Gain = 0.5
	FST_SW	Default setting; fast switching, the idle outputs are squelched
JMP1	I2C_SEL	Configures the device in I2C or GPIO mode of operation High, enables I2C mode Low, enables GPIO mode

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8 Schematics

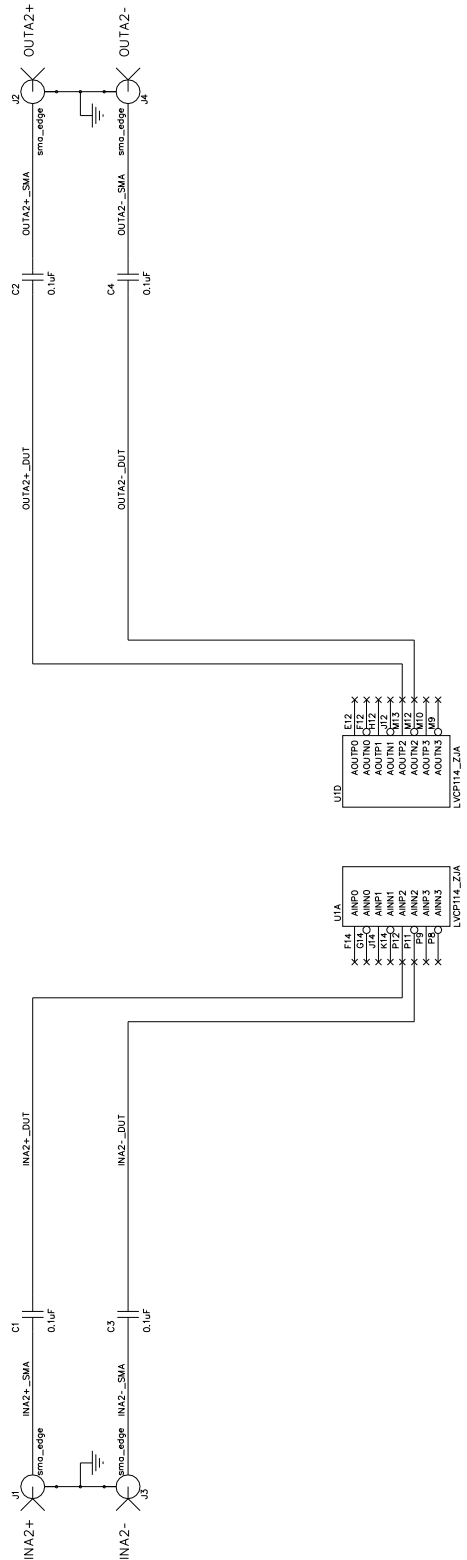

Figure 3. SN65LVCP114 EVM Schematic, Port A

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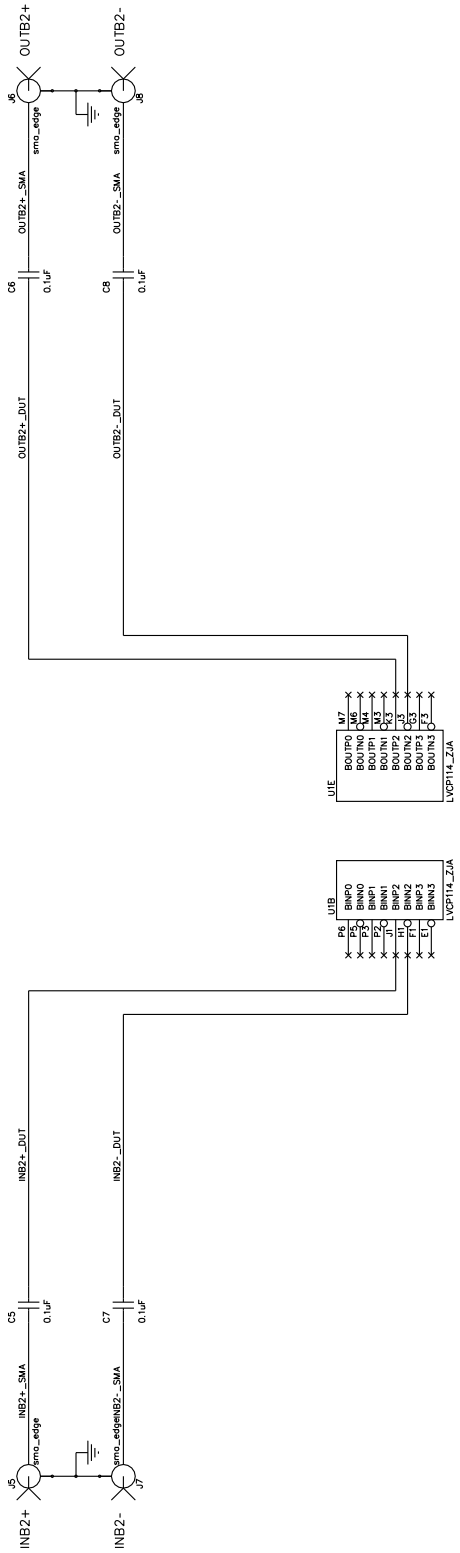

Figure 4. SN65LVCP114 EVM Schematic, Port B

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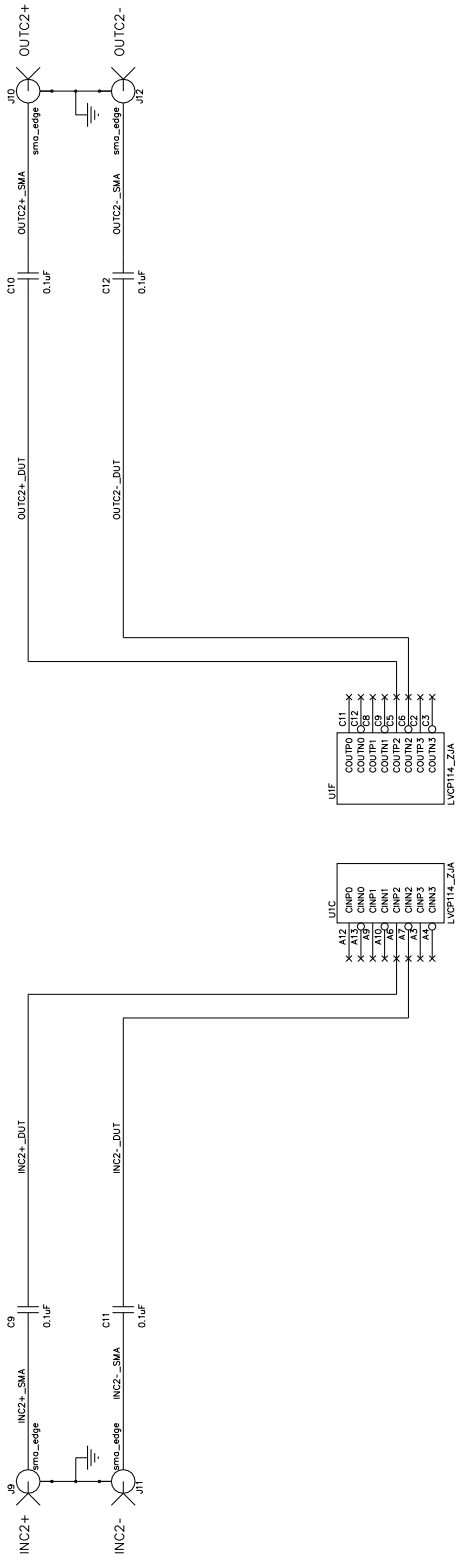

Figure 5. SN65LVCP114 EVM Schematic, Port C

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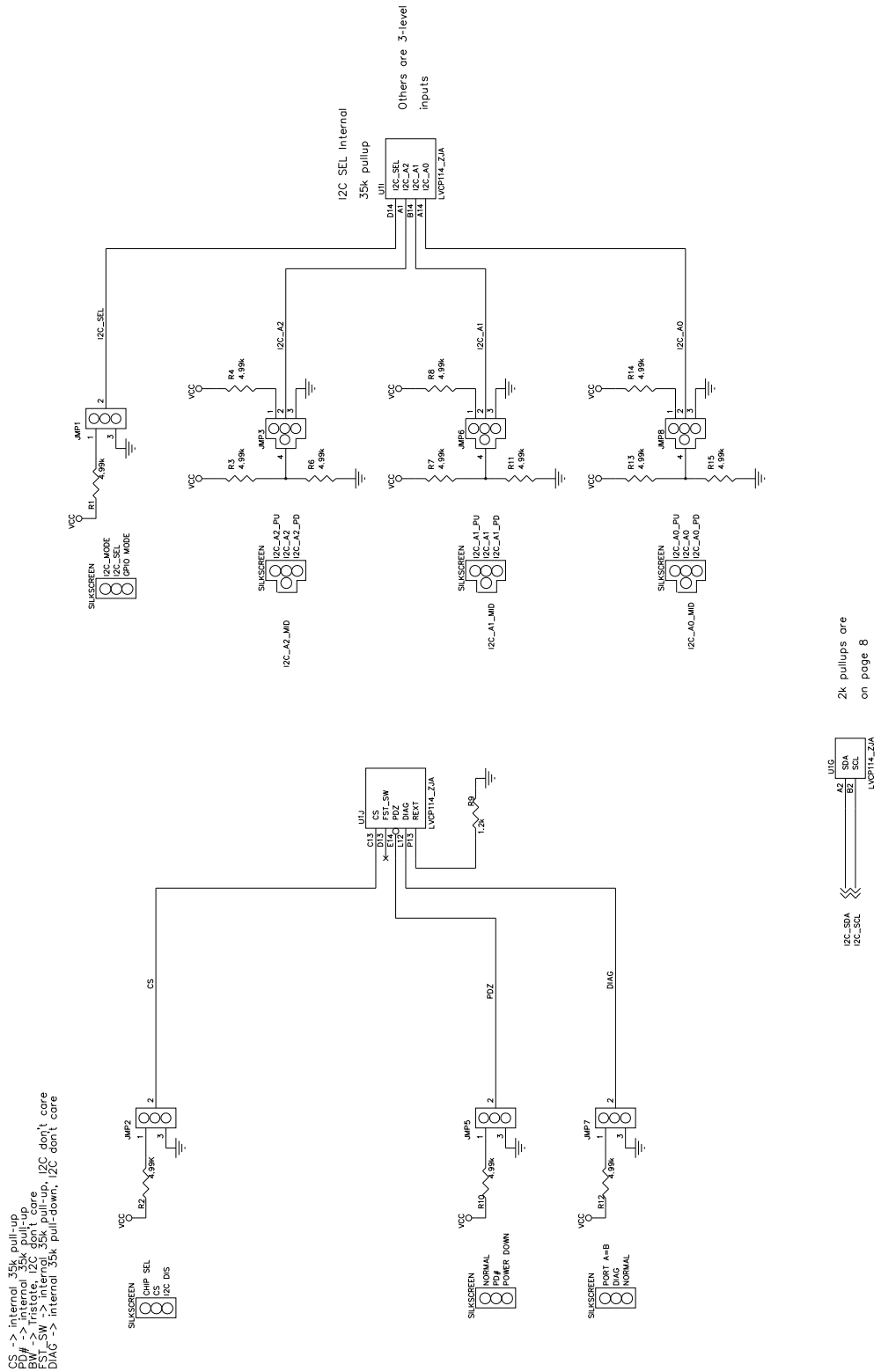

Figure 6. SN65LVCP114 EVM Schematic, Controls_1

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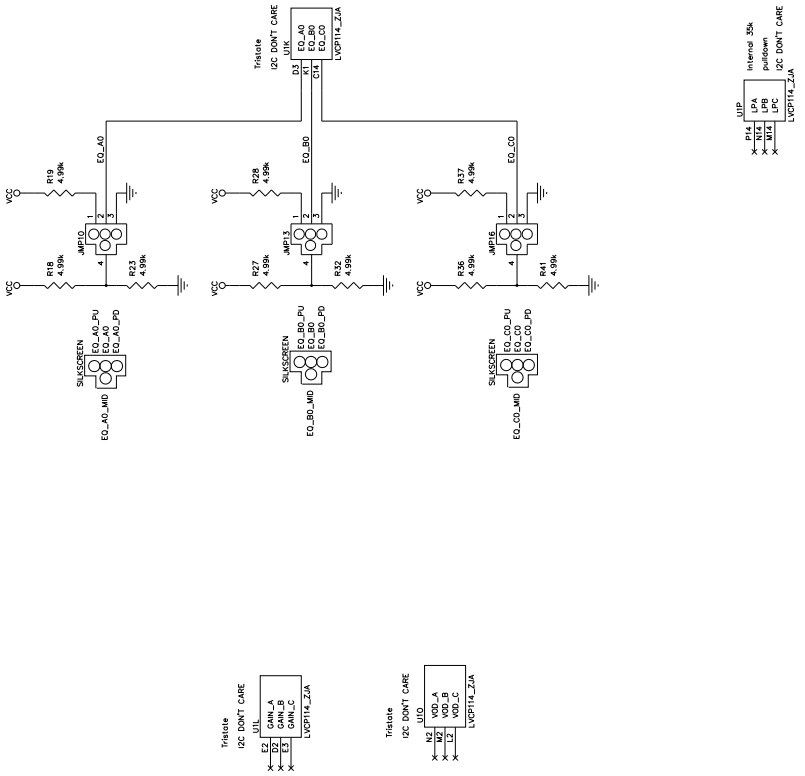

Figure 7. SN65LVCP114 EVM Schematic, Controls_2

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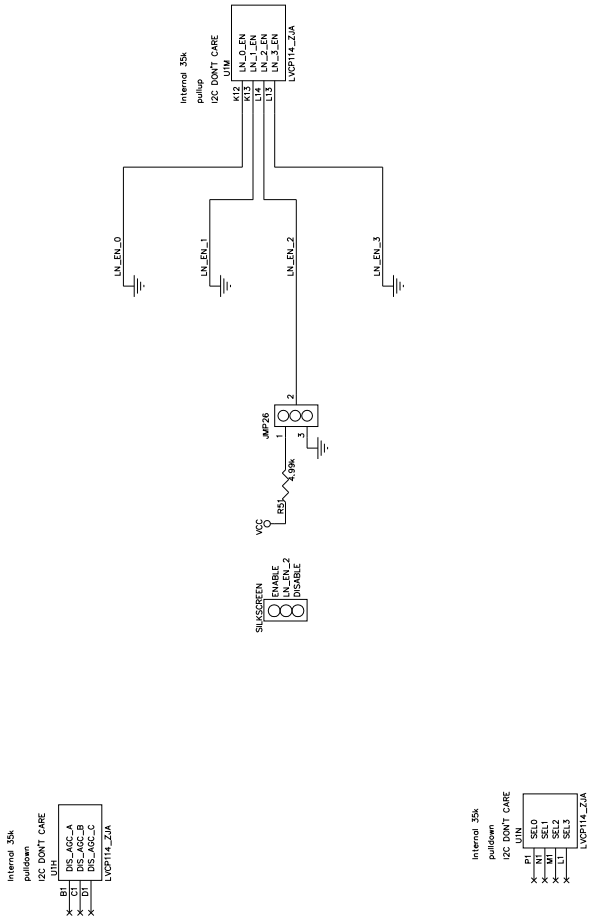

Figure 8. SN65LVCP114 EVM Schematic, Controls_3

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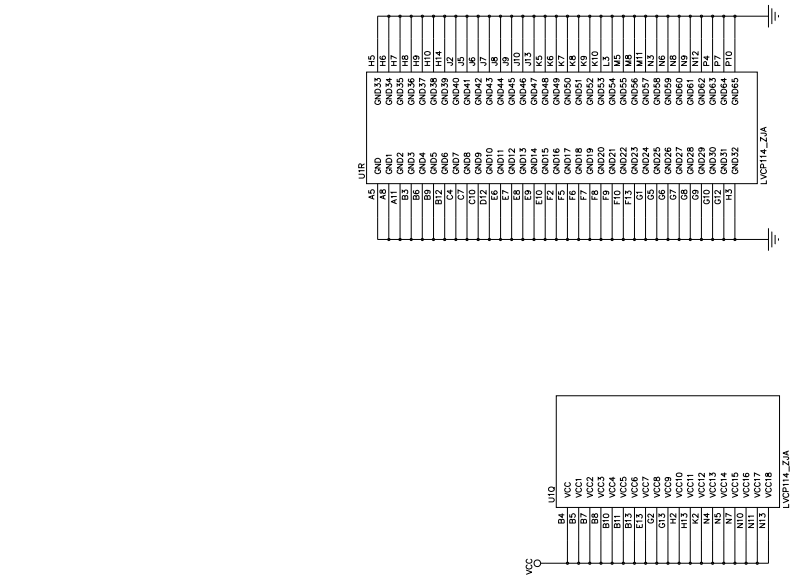

Figure 9. SN65LVCP114 EVM Schematic, Power Distribution

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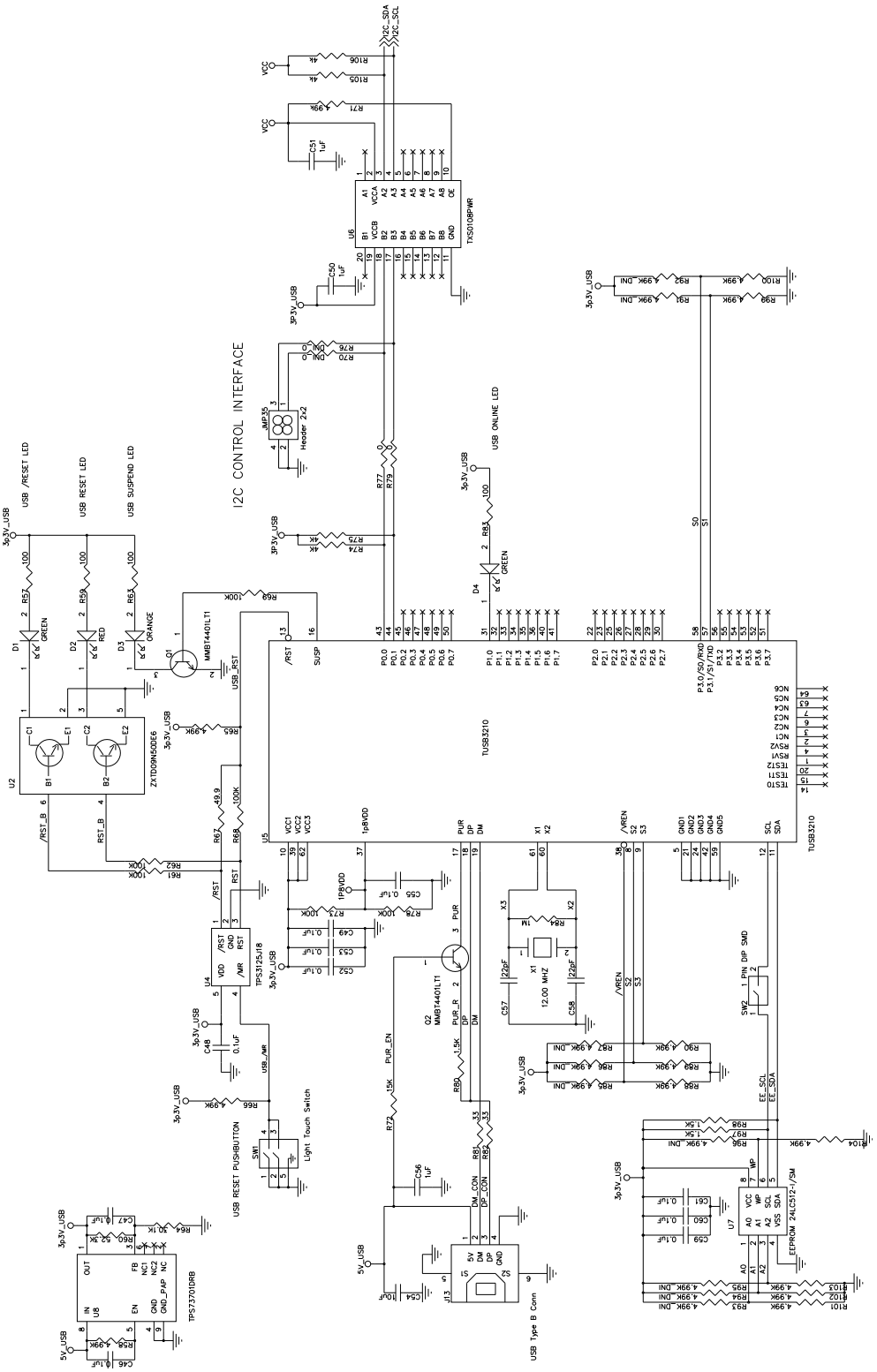

Figure 10. SN65LVCP114 EVM Schematic, USB Interface

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9 Bill of Materials

Table 5. SN65LVCP114 EVM Bill of Materials

Reference	Value	Part	Part Number	Manufacturer
C1–C12, C22, C29–C45	0.1 µF	0201 CAP	LMK063BJ104KP-F	Taiyo Yuden
C14	47 µF	1210 CAP	EMK325BJ476MM-T	Taiyo Yuden
C15	22 µF	1206 CAP	EMK316BJ226ML-T	Taiyo Yuden
C46–C49, C52, C53, C55, C59-C61	0.1 µF	0402 CAP	C1005X5R1E104K	TDK Corporation
C50, C51, C56	1 µF	0402 CAP	LMK105BJ105KV-F	Taiyo Yuden
C54	10 µF	0603 CAP	C1608X5R1A106M	TDK Corporation
C57, C58	22 pF	0402 CAP	C0402COG500-220JNE	Venkel
D1, D4	LED - GREEN	C170	HSMG-C170	Avago Technologies
D2	LED - RED	C170	SML-LXT0805IW-TR	Lumex Opto/Components
D3	LED - ORANGE	C170	HSMD-C170	Avago Technologies
JMP1, JMP2, JMP5, JMP7, JMP26	1 X 3	0.1"	HTSW-150-08-G-S	Samtec
JMP3, JMP6, JMP8, JMP10, JMP13, JMP16	1 X 4 T	0.1"	HTSW-150-08-G-S	Samtec
JMP35	2 X 2	0.1x0.1"	HTSW-150-08-G-D	Samtec
J1–J12	Edge Mount SMA	CON_02K243-40M	32K243-40ML5	Rosenberger
J13	USB - B Type	B Type	USB-B-S-F-B-TH	Samtec
P1, P2	Banana Plug - Metal	4 mm	108-0740-001	Emerson Network Power
Q1, Q2	NPN	SOT23	MMBT4401	Fairchild Semiconductor
R1–R4, R6-R8, R10–R15, R18, R19, R23, R27, R28, R32, R36, R37, R41, R51, R58, R65, R66, R71, R88–R90, R99–R104	4.99 KΩ	0402 RES	RG1005P-4991-B-T5	Susumu Co., Ltd.
R9	1.2 KΩ	0402 RES	ERJ-XGNJ122Y	Panasonic - ECG
R57, R59, R63, R83	100 Ω	0402 RES	RC0402FR-07100RL	Yageo
R60	52.3 KΩ	0402 RES	ERJ-2RKF5232X	Panasonic - ECG
R61, R62, R68, R69, R73, R78	100 KΩ	0402 RES	RC0402FR-07100KL	Yageo
R64	30.1 KΩ	0402 RES	ERJ-2RKF3012X	Panasonic - ECG
R67	49.9 Ω	0402 RES	RC0402FR-0749R9L	Yageo
R70, R76	DNI_0 Ω	0402 RES	ERJ-2GE0R00X	Panasonic - ECG
R72	15 KΩ	0402 RES	ERJ-2RKF1502X	Panasonic - ECG
R74, R75, R105, R106	4.02 KΩ	0402 RES	CRCW04024K02FKED	Vishay/Dale
R77, R79	0.0 (Zero Ohm)	0402 RES	RC0402JR-070RL	Yageo
R80, R97, R98	1.5 KΩ	0402 RES	RG1005P-152-B-T5	Susumu Co., Ltd.

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Table 5. SN65LVCP114 EVM Bill of Materials (continued)

Reference	Value	Part	Part Number	Manufacturer
R81, R82	33 Ω	0402 RES	RR0510R-330-D	Susumu Co., Ltd.
R84	1 MΩ	0402 RES	RMCF0402FT1M00	STACKPOLE ELEC. INC.
R85–R87, R91–R96	4.99 KΩ_DNI	0402 RES	RG1005P-4991-B-T5	Susumu Co., Ltd.
SW1	Momentary Push-Button Switch	6.00 mm x 6.00 mm	EVQ-PBE05R	Panasonic - ECG
SW2	1 PIN DIP SMD	SMT	SDA01H0SB	ITT Cannon - C&K
U1	LVCP114_ZJA	197pin_0.8 mm pitch BGA	SN65LVCP114ZJA	Texas Instruments
U2	DUAL NPN	SOT-23-6	ZXTD09N50DE6TA	Zetex Inc
U4	Voltage Supervisor with Manual Reset	SOT-23-5	TPS3125J18DBVR	Texas Instruments
U5	USB Microcontroller	64-LQFP	TUSB3210PM	Texas Instruments
U6	Bidirectional Level Shifter	20-TSSOP	TXB0108PWR	Texas Instruments
U7	512Kb EEPROM	8-SOIC	24LC512-I/SM	Microchip Technology
U8	Single Output LDO	8-SON	TPS73701DRB	Texas Instruments
X1	12.00 MHz Crystal	SMD	ECS-120-32-5PVX	ECS Inc
	#4-40 Machine Screw		H703-ND	Digikey
	#4-40 Rounded Thread		2029K-ND	Digikey

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10 Board Layout

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Dielectric constant	Thickness After lamination [mil]
Soldermask										0.80
L1	Signal	H	20	6.6 mil H/1		Core		RO4350B/RO4450B	3.7	2.00
										6.60
L2	Plane	1.0	100							1.20
				Press thk = 6.12 mil		Prepreg	2113(58)	PCL-370HR	3.9	6.12
							1080(65)	PCL-370HR	3.9	
L3	Plane	1.0	60	28.0 mil 1/1		Core		PCL-370HR	3.9	1.20
										28.00
L4	Plane	1.0	60							1.20
				Press thk = 6.12 mil		Prepreg	1080(65)	PCL-370HR	3.9	6.12
							2113(58)	PCL-370HR	3.9	
L5	Plane	1.0	100	6.6 mil 1/H		Core		RO4350B/RO4450B	3.7	1.20
										6.60
L6	Signal	H	20							2.00
Soldermask										0.80

Specification (Over mask on plated copper):	mil
Overall Board Thickness:	64.0
Tolerance:	+6.4/-6.4
Min-Max Board Thickness:	57.6 - 70.4

Anticipated Board Thickness:	mil
After lamination:	59.4
Over mask on plated copper:	63.8

Figure 11. SN65LVCP114 EVM PCB Layer Construction

NOTE: Always consult your board manufacturer for their process/design requirements to ensure the desired impedance is achieved.

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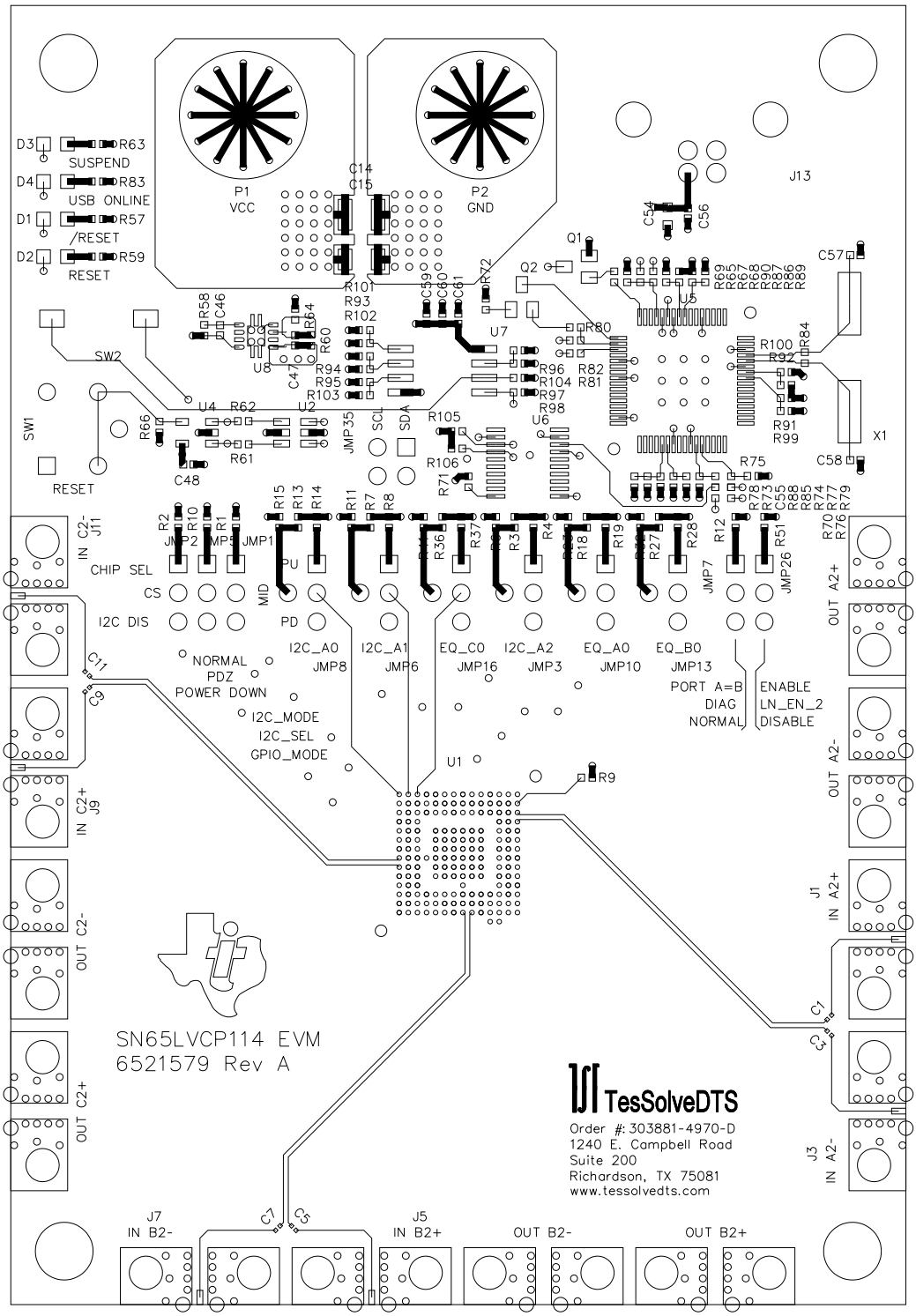

Figure 12. SN65LVCP114 Board Layout: Top Signal (Layer 1 of 6)

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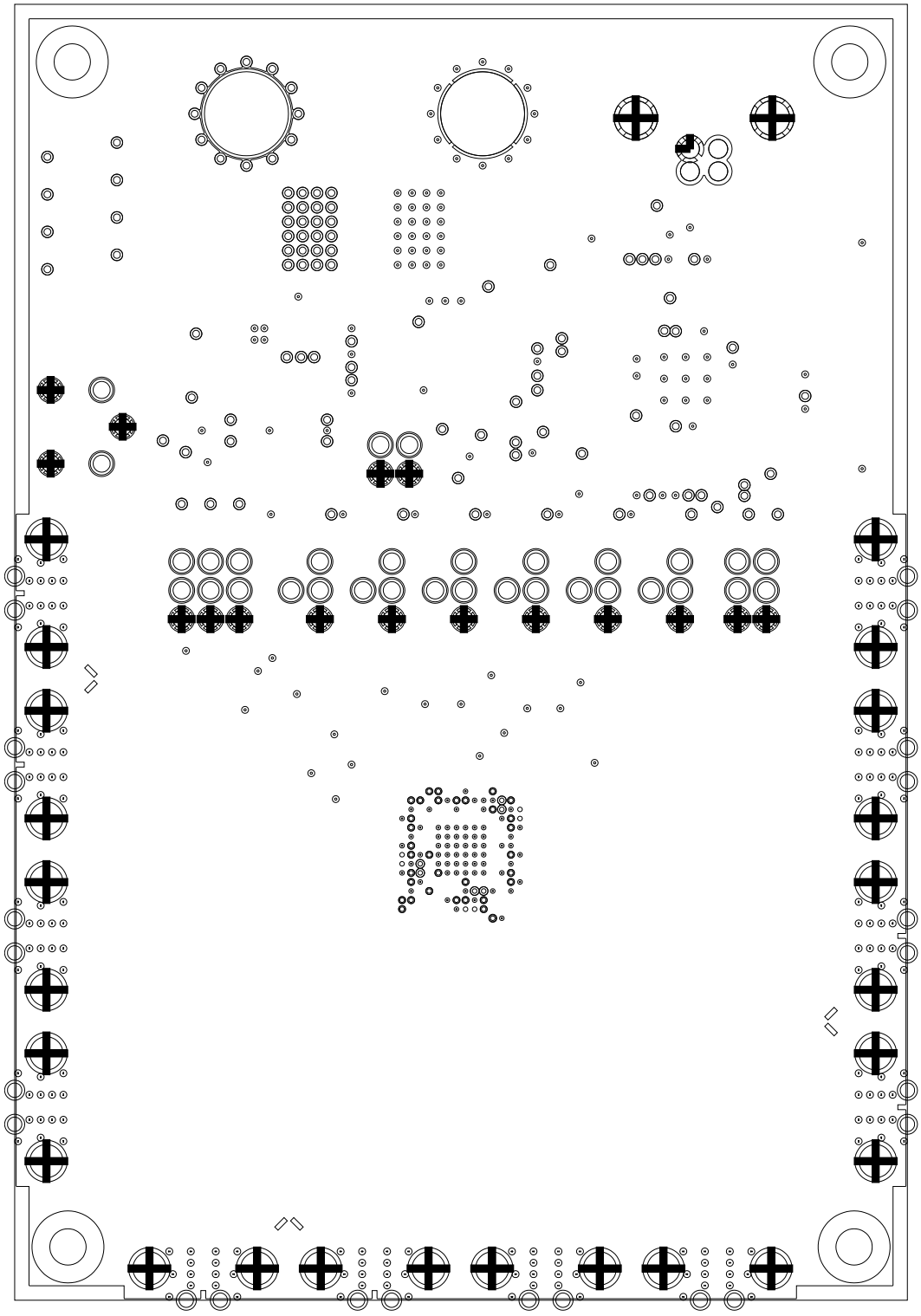

Figure 13. SN65LVCP114 Board Layout: Internal Ground (Layer 2 of 6)

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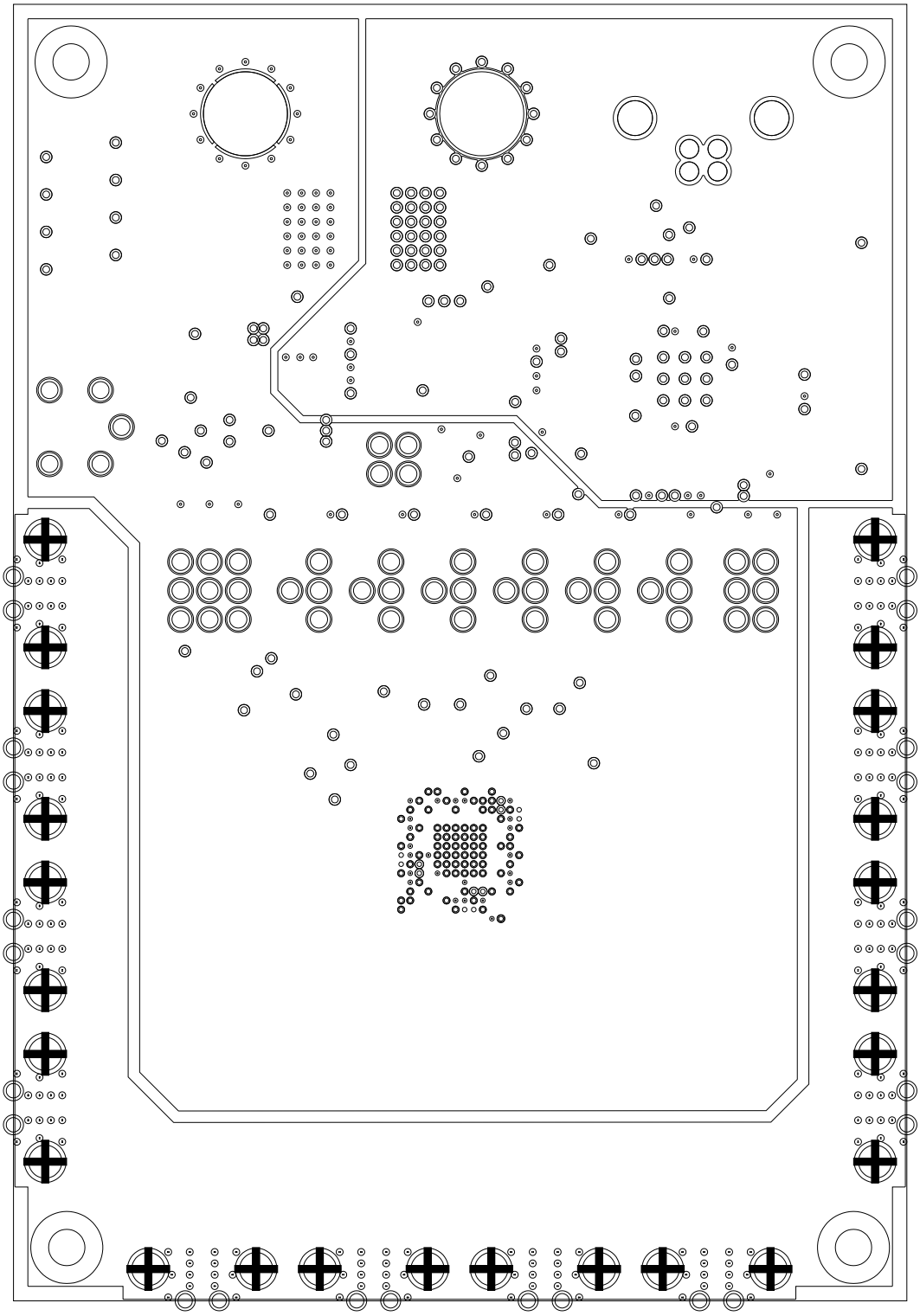

Figure 14. SN65LVCP114 Board Layout: Internal Power (Layer 3 of 6)

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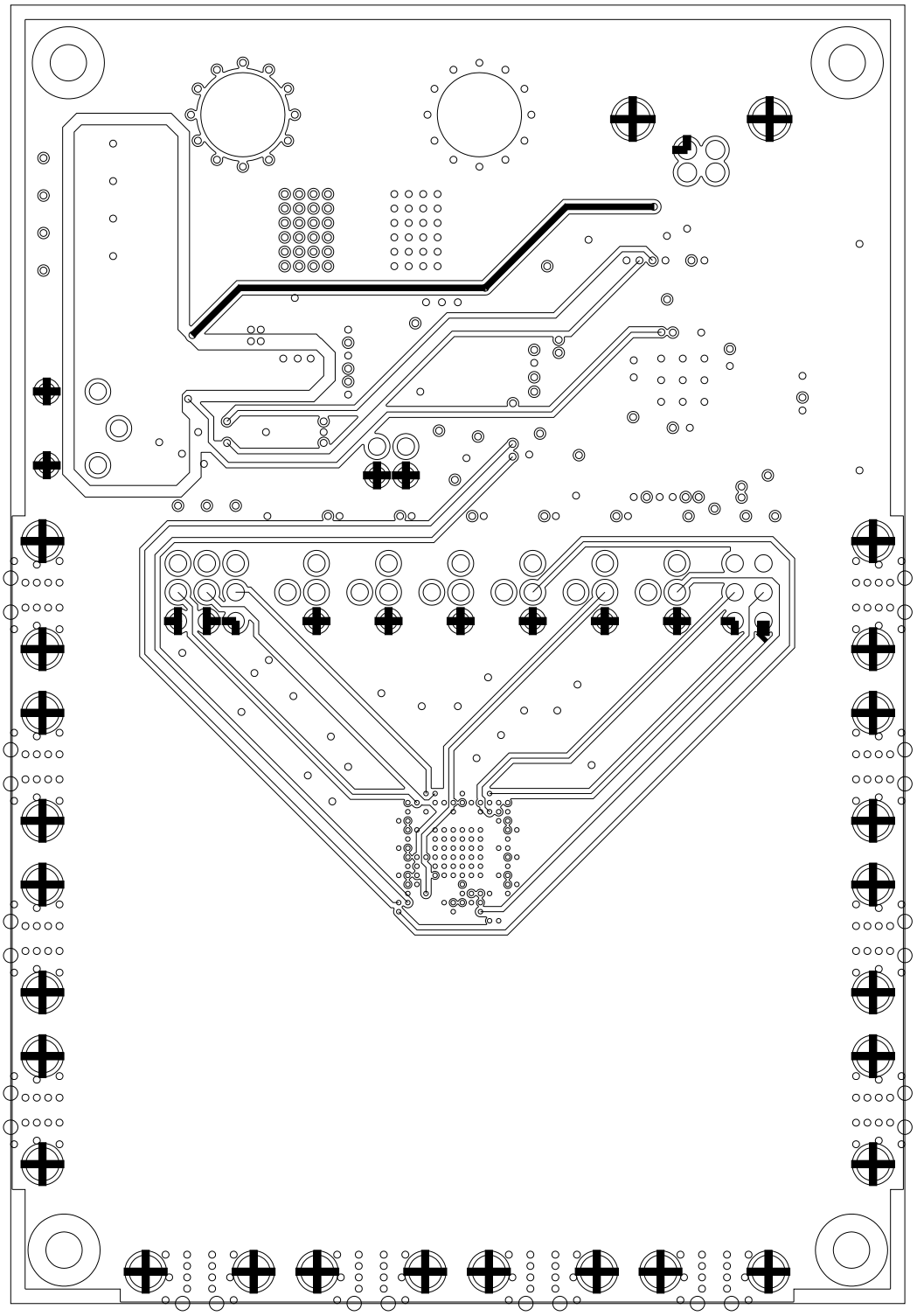

Figure 15. SN65LVCP114 Board Layout: Internal Signal (Layer 4 of 6)

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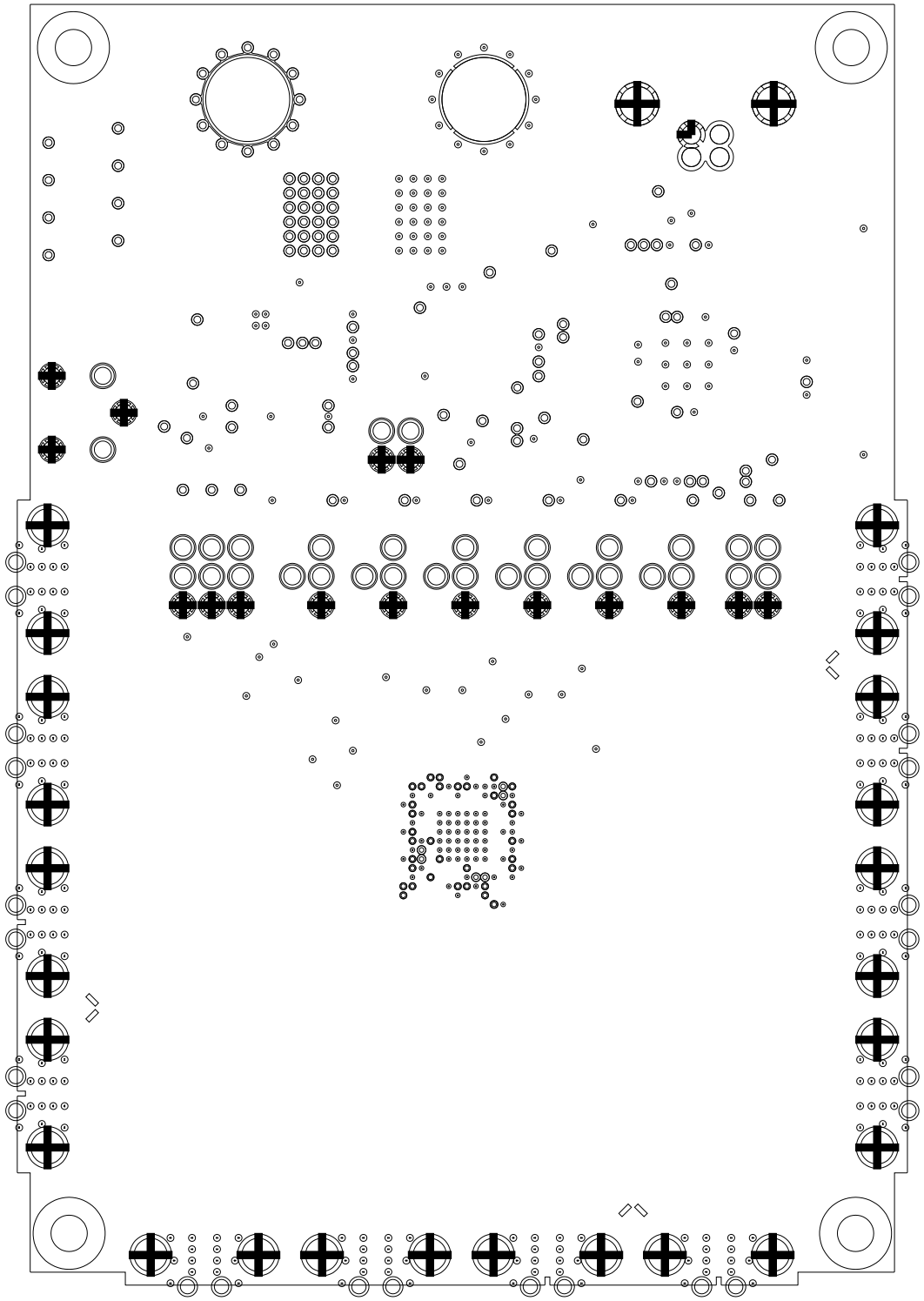

Figure 16. SN65LVCP114 Board Layout: Internal Ground (Layer 5 of 6)

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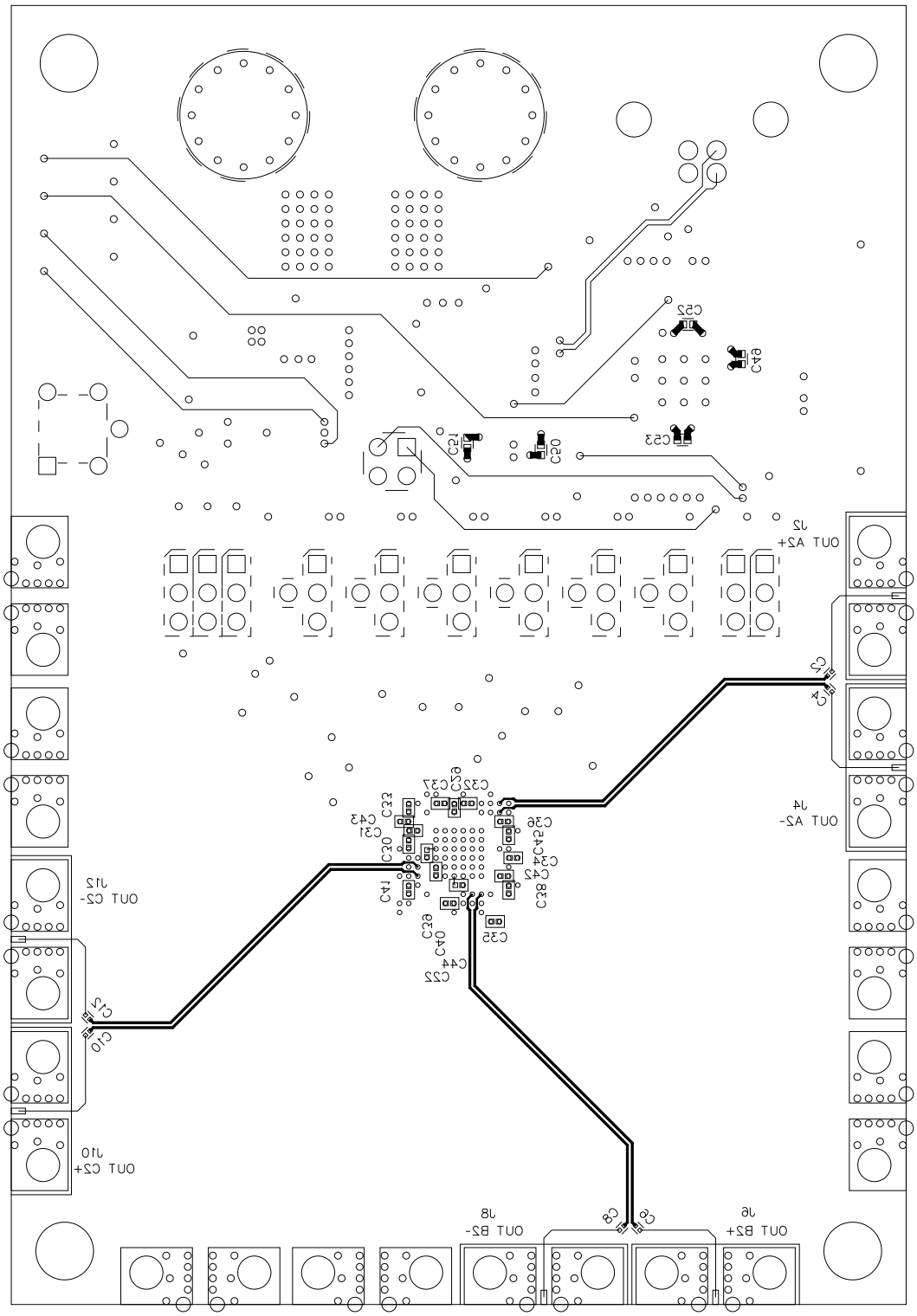

Figure 17. SN65LVCP114 Board Layout: Bottom Signal (Layer 6 of 6)

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Appendix A Jumper Shunt Settings

The table below shows the different shunt settings of the 3 and 4 pin jumpers on the EVM.

Shunt Setting	Description
	High
	HiZ
	Low
	High
	Low

Appendix B Typical Evaluation Setups

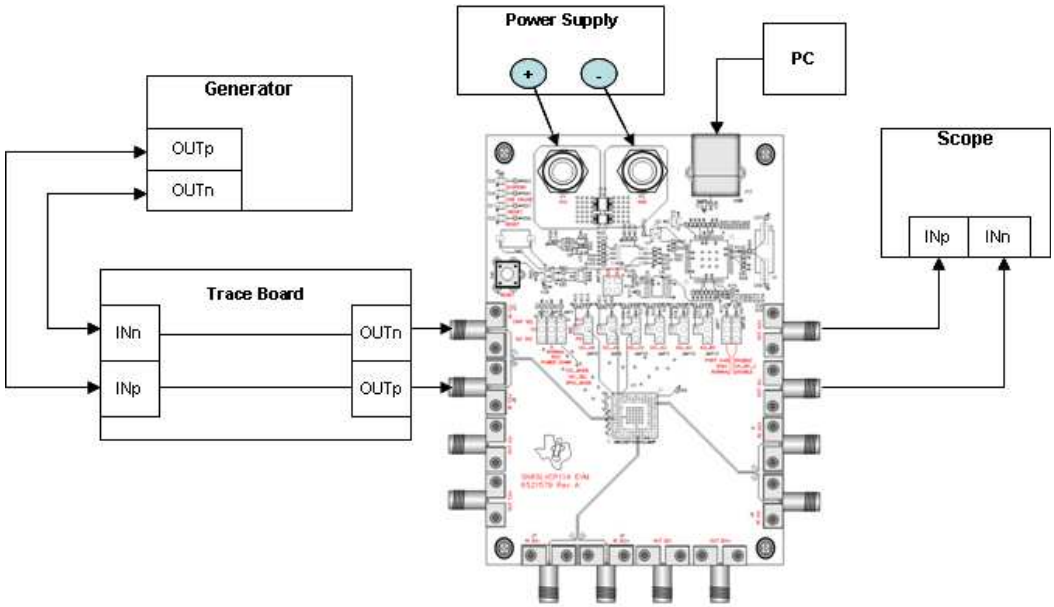

Figure 18. Receive Side Use Case

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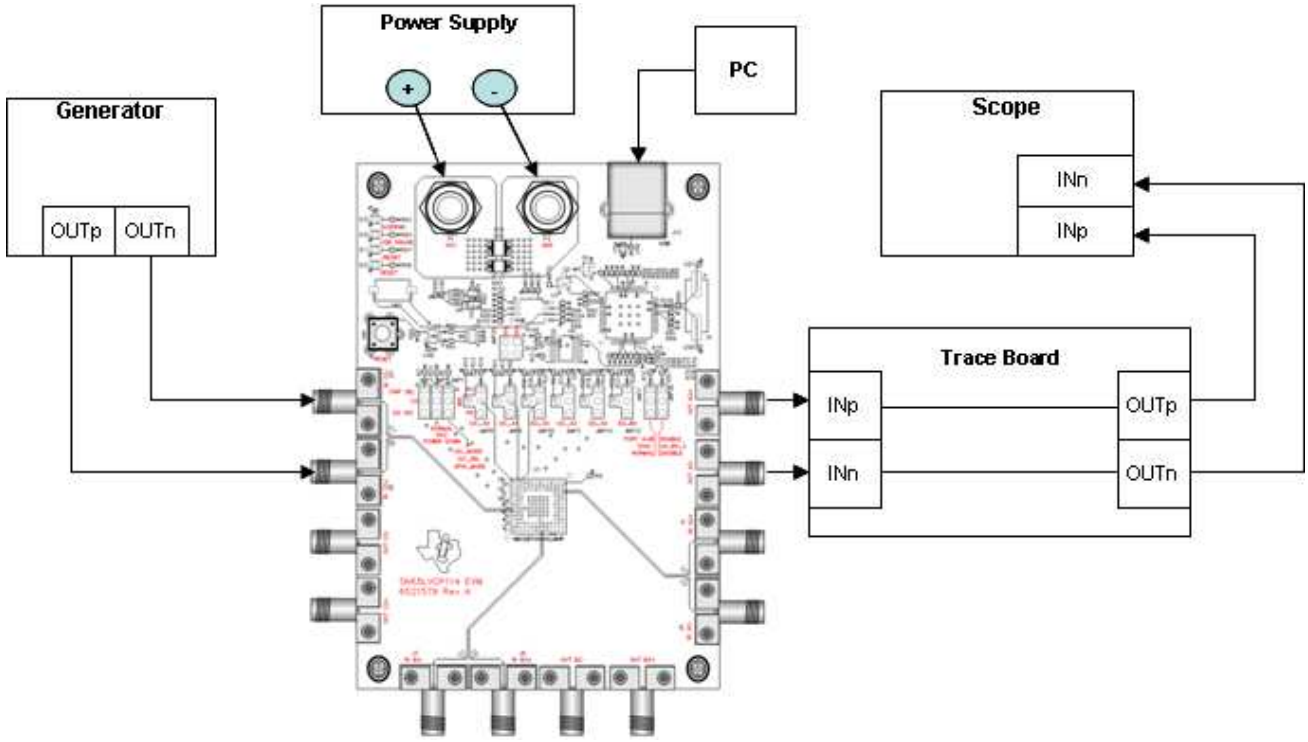

Figure 19. Transmit Side Use Case

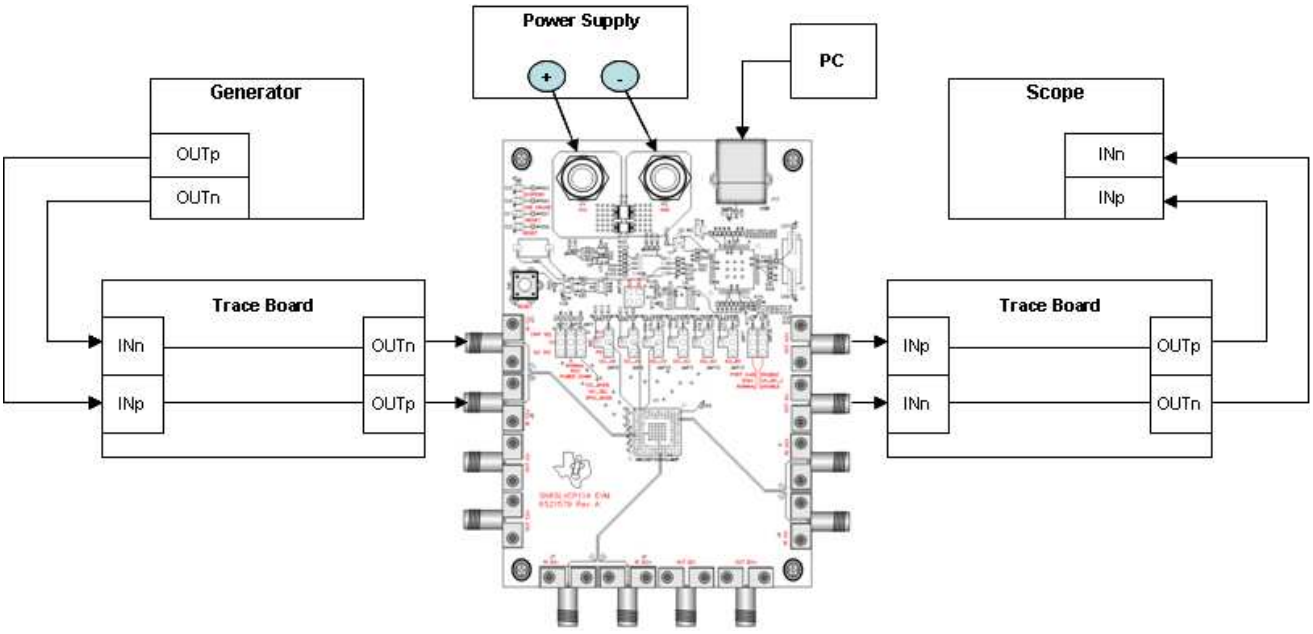

Figure 20. Combined Bus Extension Use Case

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
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