# LV8805V

## BI-CMOS LSI Fan Motor Driver for PC and Server

## **Overview**

The LV8805V is a motor driver for PC and server fans.

## Feature

• Direct PWM three-phase sensorless motor driver

## **Typical Applications**

- Computer peripherals
- Fan motor Unit
- Server

#### **Specifications Absolute Maximum Ratings** at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V <sub>CC</sub> maximum supply voltage	V <sub>CC</sub> max		16	V
VG maximum supply voltage	VG max		21	V
OUT pin withstand voltage	V <sub>OUT</sub> max		16	V
OUT pin maximum output	I <sub>OUT</sub> max		1.2	А
SOFTST pin withstand voltage	V <sub>SOFTST</sub> max		6	V
FR pin withstand voltage	V <sub>FR</sub> max		6	V
PWMIN pin withstand voltage	V <sub>PWMIN</sub> max		6	V
FG output pin withstand voltage	V <sub>FG</sub> max		16	V
FG pin output current	I <sub>FG</sub> max		5	mA
1/2FG output pin withstand	V <sub>1/2FG</sub> max		16	V
1/2FG pin output current	I <sub>1/2FG</sub> max		5	mA
RD output pin withstand voltage	VRD max		16	V
RD pin output current	IRD max		5	mA
Allowable Power dissipation 1	Pd max1	Independent IC	0.6	W
Allowable Power dissipation 2	Pd max2	Mounted on designated board *1	1.3	W
Operating temperature	Topr		-40 to +95	°C
Storage temperature	Tstg	*2	–55 to +150	°C

\*1: When mounted on the designated 76.1mm × 114.3mm × 1.6mm, glass epoxy board (single-layer)

\*2: Do not exceed Tjmax=150°C.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

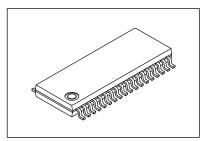
Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 12 of this data sheet.





SSOP36J (275mil)

## **Recommended Operating Conditions** at $Ta = 25^{\circ}C$

6 to 15	V
0 to VREG	V
0 to VREG	V
0 to VREG	V
	0 to VREG 0 to VREG

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## **Electrical Characteristics** at Ta = 25°C, V<sub>CC</sub> = 12V, unless otherwise specified

				Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Circuit current 1	I <sub>CC</sub> 1			2.6	3.6	mA
Charge pump block						
Charge pump output voltage	V <sub>VG</sub>			17		V
Regulator block	•	·				
5V regulator voltage	VVREG		4.75	5	5.25	V
Output on resistance						
Sum of high-/low-side output transistor on	Ron (H+L)	I <sub>O</sub> = 0.7A, V <sub>CC</sub> = 12V, VG = 17V		1.2	2	Ω
resistance						
Startup oscillator (OSC) pin	1					
OSC pin charge current	IOSCC			-2.5		μA
OSC pin discharge current	I <sub>OSC</sub> D			2.5		μA
PWM input (PWMIN) pin						
High-level input voltage range	V <sub>PWMIN</sub> H		2.5		VREG	V
Low-level input voltage range	VPWMINL		0		1	V
Range of PWM input frequency	<sup>f</sup> PWMIN		15		60	kHz
Minimum pulse width	T <sub>MINPW</sub>	Input HIGH voltage 5[V] and input LOW voltage 0[V]			0.2	μS
$(T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for minin}$ $(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty	naximum v cycle range = 1.2% v cycle range = 1.0%	6 - 99.0%				
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty	haximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5%	6 - 99.0% 6 - 99.5%				
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b>	haximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3%	6 - 99.0% 6 - 99.5% 6 - 99.7%				
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty	haximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5%	<ul> <li>6 - 99.0%</li> <li>6 - 99.5%</li> <li>6 - 99.7%</li> <li>Order of current application : UOUT→VOUT→WOUT</li> </ul>	2.5		VREG	V
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b>	haximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3%	6 - 99.0% 6 - 99.5% 6 - 99.7% Order of current application :	2.5		VREG 1	V
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60[kHz]$ , the input PWM duty When $f_{PWMIN} = 50[kHz]$ , the input PWM duty When $f_{PWMIN} = 25[kHz]$ , the input PWM duty When $f_{PWMIN} = 15[kHz]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range	haximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH	<ul> <li>6 - 99.0%</li> <li>6 - 99.5%</li> <li>6 - 99.7%</li> <li>Order of current application : UOUT→VOUT→WOUT</li> <li>Order of current application :</li> </ul>				-
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\%$ for m When $f_{PWMIN} = 60[kHz]$ , the input PWM duty When $f_{PWMIN} = 50[kHz]$ , the input PWM duty When $f_{PWMIN} = 25[kHz]$ , the input PWM duty When $f_{PWMIN} = 15[kHz]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range	haximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH	<ul> <li>6 - 99.0%</li> <li>6 - 99.5%</li> <li>6 - 99.7%</li> <li>Order of current application : UOUT→VOUT→WOUT</li> <li>Order of current application :</li> </ul>		0.25		-
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG, 1/2FG, and RD output pins</b>	naximum y cycle range = 1.2% y cycle range = 1.0% y cycle range = 0.5% y cycle range = 0.3% VFRH VFRL	6 - 99.0% 6 - 99.5% 6 - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT		0.25	1	V
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG, 1/2FG, and RD output pins</b> FG output pin low-level voltage	naximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH VFRL VFRL	% - 99.0% 6 - 99.5% 6 - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT When I <sub>O</sub> is 2mA		0.25	1	V
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG</b> , <b>1/2FG</b> , <b>and RD output pins</b> FG output pin low-level voltage FG output pin leak voltage	aximum y cycle range = 1.2% y cycle range = 1.0% y cycle range = 0.5% y cycle range = 0.3% VFRH VFRL VFRL VFG ILFG				1 0.35 1	V V µA
$(1 - T_{MINPW} \times f_{PWMM}) \times 100\% \text{ for m}$ When $f_{PWMM} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG</b> , 1/2 <b>FG</b> , and <b>RD</b> output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin low-level voltage	Aaximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH VFRH VFRL VFG ILFG V1/2FG	<ul> <li>6 - 99.0%</li> <li>6 - 99.5%</li> <li>6 - 99.7%</li> <li>Order of current application : UOUT→VOUT→WOUT</li> <li>Order of current application : UOUT→WOUT→VOUT</li> <li>When I<sub>O</sub> is 2mA</li> <li>When V<sub>FG</sub> is 16V</li> <li>When I<sub>O</sub> is 2mA</li> </ul>			1 0.35 1 0.35	۷ ۷ μΑ ۷
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG</b> , 1/2 <b>FG</b> , and <b>RD</b> output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage	aximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH VFRL VFRL VFG ILFG V1/2FG IL1/2FG			0.25	1 0.35 1 0.35 1	V V μΑ V μΑ
$(1 - T_{MINPW} \times f_{PWMIN}) \times 100\% \text{ for m}$ When $f_{PWMIN} = 60[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 50[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 25[\text{kHz}]$ , the input PWM duty When $f_{PWMIN} = 15[\text{kHz}]$ , the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG, 1/2FG, and RD output pins</b> FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin low-level voltage	naximum         v cycle range = 1.2%         v cycle range = 1.0%         v cycle range = 0.5%         v cycle range = 0.3%         Verge range = 0.3%         VFRH         VFRL         VFRL         VFG         ILFG         V1/2FG         IL1/2FG         VRD			0.25	1 0.35 1 0.35 1 0.35	V ν μΑ ν ν ν
<ul> <li>(1 - <i>T<sub>MINPW</sub></i> x <i>f<sub>PWMIN</sub></i>) x 100% for m When <i>f<sub>PWMIN</sub></i> = 60[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 50[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 25[kHz], the input PWM duty <b>Forward/reverse switching pin</b></li> <li>High-level input voltage range</li> <li>Low-level input voltage range</li> <li>FG, 1/2FG, and RD output pins</li> <li>FG output pin leak voltage</li> <li>1/2FG output pin leak voltage</li> <li>RD output pin leak voltage</li> <li>RD output pin leak voltage</li> </ul>	naximum         v cycle range = 1.2%         v cycle range = 1.0%         v cycle range = 0.5%         v cycle range = 0.3%         Verge range = 0.3%         VFRH         VFRL         VFRL         VFG         ILFG         V1/2FG         IL1/2FG         VRD			0.25	1 0.35 1 0.35 1 0.35	V ν μΑ ν ν ν
<pre>(1 - T<sub>MINPW</sub> x f<sub>PWMMN</sub>) x 100% for m When f<sub>PWMMN</sub> = 60[kHz], the input PWM duty When f<sub>PWMMN</sub> = 50[kHz], the input PWM duty When f<sub>PWMMN</sub> = 25[kHz], the input PWM duty When f<sub>PWMMN</sub> = 15[kHz], the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin low-level voltage 1/2FG output pin low-level voltage RD output pin leak voltage RD output pin leak voltage RD output pin leak voltage</pre>	naximum         v cycle range = 1.2%         v cycle range = 1.0%         v cycle range = 0.5%         v cycle range = 0.3%         VFRH         VFRL         VFR         ILFG         V1/2FG         IL1/2FG         VRD	% - 99.0% % - 99.5% % - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT When I <sub>O</sub> is 2mA When V <sub>FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA	0	0.25	1 0.35 1 0.35 1 0.35 1	V V Αμ V V V V Αμ
(1 - <i>T<sub>MINPW</sub></i> x <i>f<sub>PWMIN</sub></i> ) x 100% for m When <i>f<sub>PWMIN</sub></i> = 60[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 50[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 25[kHz], the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range FG, 1/2FG, and RD output pins FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin leak voltage RD output pin leak voltage RD output pin leak voltage	naximum         v cycle range = 1.2%         v cycle range = 1.0%         v cycle range = 0.5%         v cycle range = 0.3%         VFRH         VFRL         VFR         ILFG         V1/2FG         IL1/2FG         VRD	% - 99.0% % - 99.5% % - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT When I <sub>O</sub> is 2mA When V <sub>FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA	0	0.25	1 0.35 1 0.35 1 0.35 1	V V Αμ V V V Αμ
(1 - <i>T<sub>MINPW</sub></i> x <i>f<sub>PWMIN</sub></i> ) x 100% for m When <i>f<sub>PWMIN</sub></i> = 60[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 50[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 25[kHz], the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG, 1/2FG, and RD output pins</b> FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin low-level voltage RD output pin low-level voltage <b>Current limiter circuit</b> Limiter voltage	aximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH VFRL VFRL VFG ILFG V1/2FG IL1/2FG VRD ILRD VRF	% - 99.0% % - 99.5% % - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT When I <sub>O</sub> is 2mA When V <sub>FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA	0	0.25	1 0.35 1 0.35 1 0.35 1 0.275	V ν μΑ ν ν μΑ ν ν ν
(1 - <i>T<sub>MINPW</sub></i> x <i>f<sub>PWMIN</sub></i> ) x 100% for m When <i>f<sub>PWMIN</sub></i> = 60[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 55[kHz], the input PWM duty When <i>f<sub>PWMIN</sub></i> = 25[kHz], the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG, 1/2FG, and RD output pins</b> FG output pin low-level voltage FG output pin leak voltage 1/2FG output pin leak voltage RD output pin leak voltage RD output pin leak voltage RD output pin leak voltage <b>Current limiter circuit</b> Limiter voltage <b>Constraint protection circuit</b> CT pin high-level voltage	Aaximum v cycle range = 1.2% v cycle range = 1.0% v cycle range = 0.5% v cycle range = 0.3% VFRH VFRH VFRL VFRL VFG ILFG V1/2FG IL1/2FG VRD ILRD VRF VRF	% - 99.0% % - 99.5% % - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT When I <sub>O</sub> is 2mA When V <sub>FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA	0	0.25	1 0.35 1 0.35 1 0.35 1 0.275 2.95	V V μA V μA V μA V V V
(1 – <i>T<sub>MINPW</sub></i> x <i>f<sub>PWMMN</sub></i> ) x 100% for m When <i>f<sub>PWMMN</sub></i> = 60[kHz], the input PWM duty When <i>f<sub>PWMMN</sub></i> = 50[kHz], the input PWM duty When <i>f<sub>PWMMN</sub></i> = 25[kHz], the input PWM duty <b>Forward/reverse switching pin</b> High-level input voltage range Low-level input voltage range <b>FG, 1/2FG, and RD output pins</b> FG output pin low-level voltage FG output pin low-level voltage 1/2FG output pin low-level voltage RD output pin low-level voltage RD output pin leak voltage RD output pin leak voltage <b>Current limiter circuit</b> Limiter voltage <b>Constraint protection circuit</b> CT pin high-level voltage	aximum         v cycle range = 1.2%         v cycle range = 1.0%         v cycle range = 0.5%         v cycle range = 0.3%         VFRH         VFRH         VFR         ILFG         V1/2FG         IL1/2FG         VRD         ILRD         VRF         VCTH         VCTL	% - 99.0% % - 99.5% % - 99.7% Order of current application : UOUT→VOUT→WOUT Order of current application : UOUT→WOUT→VOUT When I <sub>O</sub> is 2mA When V <sub>FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA When V <sub>1/2FG</sub> is 16V When I <sub>O</sub> is 2mA	0	0.25 0.25 0.25 2.8 0.5	1 0.35 1 0.35 1 0.35 1 0.275 2.95 0.65	V μA V μA V μA V μA V V

Continued on next page.

## LV8805V

Continued from preceding page.							
Parameter	O: mah al	Conditions	Ratings			Unit	
Parameter	Symbol		min	typ	max	Unit	
Soft start circuit							
Soft start releasing voltage	VSOFTST			2.5		V	
SOFTST pin charge current				0.6		μA	
Thermal protection circuit							
Thermal protection circuit operating	TSD	Design target *	150	180	210	°C	
temperature							

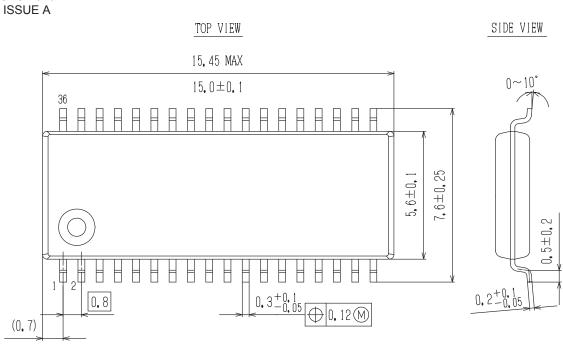
\*: Design target value and no measurement is made. The thermal protection circuit is incorporated to protect the IC from burnout or thermal destruction. Since it operates outside the IC's guaranteed operating range, the customer's thermal design should be performed so that the thermal protection circuit will not be activated when the fan is running under normal operating conditions.

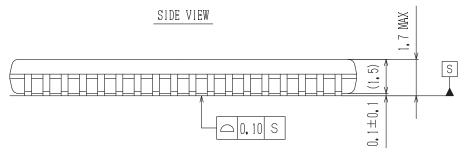
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## **Package Dimensions**

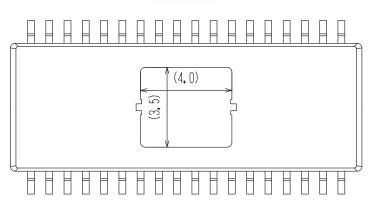
unit : mm

SSOP36J (275mil) Exposed Pad CASE 940AH

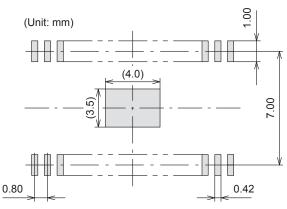




BOTTOM VIEW



#### SOLDERING FOOTPRINT\*

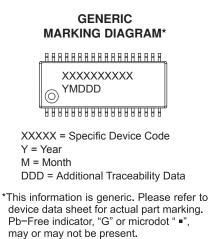


#### NOTES:

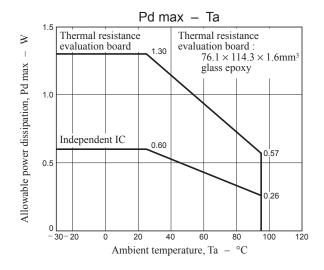
- 1. The measurements are for reference only, and unable to guarantee.
- 2. Please take appropriate action to design the actual Exposed Die Pad and Fin portion.
- 3. After setting, verification on the product must be done.

(Although there are no recommended design for Exposed Die Pad and Fin portion Metal mask and shape for Through–Hole pitch (Pitch & Via etc), checking the soldered joint condition and reliability verification of soldered joint will be needed. Void = gradient = insufficient thickness of soldered joint or bond degradation could lead IC destruction because thermal conduction to substrate becomes poor.)

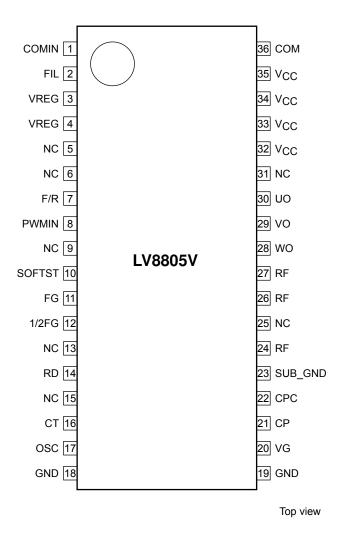
\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

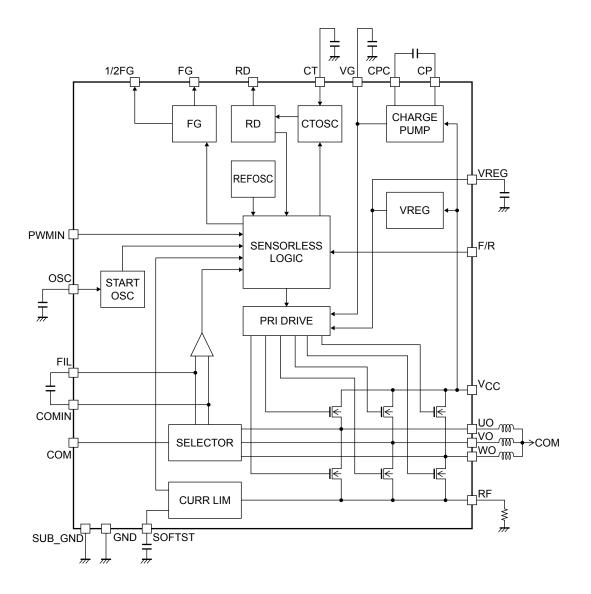


www.onsemi.com 5



## **Pin Assignment**



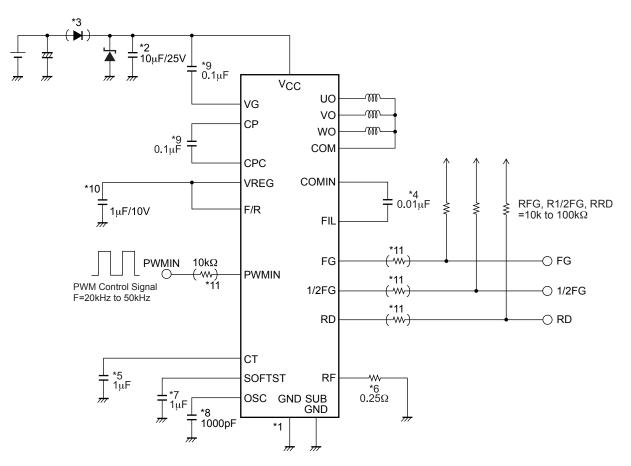


Pin Fu	Inction		
Pin No.	Pin name	Function	Equivalent circuit
36	СОМ	Motor middle point connection.	VG
2	COMIN	Motor position detection comparator filter pin. A capacitor must be connected between this pin and the FIL pin (pin 2). Motor position detection comparator filter pin. A capacitor must be connected between this pin and the COMIN pin (pin 5).	
3 4	VREG	Regulator voltage (5V) output. A capacitor must be connected between these pins and ground.	VCC VREF VREF WREF WREF WREF WREF WREF WREF WREF W
5, 6, 9 13, 15, 25, 31	NC	No connection. These pins are not connected with the internal parts.	
7	F/R	Motor rotation direction switching. A high-level input causes current to flow into the motor in the order of U, V, and W and a low-level input in the order of U, W, and V. Changing the order of current application turns the motor in the opposite direction.	VREG Reverse signal 7 $15k\Omega$ 7 $100k\Omega$ Forward signal
8	PWMIN	PWM signal input pin. "H" The output transistor is turned on by the level voltage input. "L" The output transistor is turned off by the level voltage input, and the motor stops. The speed of the motor is controlled by controlling Duty of the input signal. When the pin opens, the motor becomes all velocities.	
10	SOFTST	Soft start time setting. The motor can be started smoothly by connecting a capacitor between this pin and ground.	

Continued on next page.

	om preceding pag		Equivalent eizevit
Pin No.	Pin name	Function	Equivalent circuit
11	FG	FG pulse output. This pin outputs a Hall sensor system equivalent pulse signal.	(11) (12) (14)
12	1/2FG	FG pulse output. This pin outputs 1/2 Hall sensor system equivalent pulse signal.	
14	RD	Motor lockup detection output. Output is fixed high when motor is locked up.	
16	СТ	Motor lockup detection time setting. When the motor lockup condition is detected, the protection time period before the protection circuit is activated is set by connecting a capacitor between this pin and ground.	VREG VREG 5500Ω 16 m
17	OSC	Motor startup frequency setting. A capacitor must be connected between this pin and ground. The startup frequency is adjusted by controlling the charge/discharge current and capacitance of the capacitor.	$VREG$ $500\Omega$ $17$ $500\Omega$ $17$ $6$ $7$ $7$ $7$ $7$ $7$ $7$ $7$ $7$ $7$ $7$
18, 19	GND	GND pin.	
20	VG	Charge pump step-up voltage output. A capacitor must be connected between this pin and the $V_{CC}$ pin or ground.	(21) (22) ↑ Vcc → →
21	CP	Charge pump step-up pulse output pin. A capacitor must be connected between this pin and the CPC pin (pin 22).	
22	CPC	Charge pump step-up pin. A capacitor must be connected between this pin and the CP pin (pin 21).	
23	SUB_GND	GND pin.	
32, 33,	V <sub>CC</sub>	Power supply for the IC and motor. Capacitors must be connected between	
34, 35		these pins and ground.	
30	UO	Output pins. Connect these pins to the U, V, and W of the motor coil.	
29	VO		
28	WO		
24, 26, 27	RF	Output current detection pins. The drive current is detected by connecting a resistor between these pins and ground.	

## Application Circuit Example



\*1. Power supply and GND wiring

The GND is connected to the control circuit power supply system.

\*2. Power-side power stabilization capacitor

For the power-side power stabilization capacitor, use a capacitor of  $10\mu$ F or more. Connect the capacitor between V<sub>CC</sub> and GND with a thick and along the shortest possible route. The V<sub>CC</sub> pins (pins 32, 33, 34, and 35) must be short-circuited on the print pattern. The GND pins (pins 18 and 19) and the SUB\_GND pin (pin 23) must be short-circuited on the print pattern.

LV8805V uses synchronous rectification for high efficiency drive. Synchronous rectification is effective for heat reduction and higher efficiency. However, it may increase supply voltage. If the supply voltage shall increase make sure that it does not exceed the maximum ratings by inserting a zener dic

If the supply voltage shall increase, make sure that it does not exceed the maximum ratings by inserting a zener diode between power supply and GND.

\*3. Reverse connection protection diode

This diode protects reverse connection.

Insert a diode between power supply and  $V_{CC}$  pin to protect the IC from destruction due to reverse connection. Connection of this diode is not necessary required.

\*4. COMIN and FIL pins

These pins are used to connect the filter capacitor. The LV8805V uses the back EMF signal generated when the motor is running to detect the information on the rotor position. The IC determines the timing at which the output block applies current to the motor based on the position information obtained here. Insert a filter capacitor with a capacitance ranging from 1,000pF to 10,000pF (reference value) between the COMIN pin and FIL pin to prevent any motor startup misoperation that is caused by noise. However, care must be taken since an excessively high capacitance will give rise to deterioration in efficiency and delays in the output power-on timing while the motor is running at high speed. Furthermore, connect the capacitor between the COMIN pin and FIL pin as close as possible in order to avoid the effects of noise from other sources.

## \*5. CT pin

This pin is used to connect the lock detection capacitor.

The constant-current charging and constant-current discharging circuits incorporated cause locking when the pin voltage reaches 2.5V, and releasing the lock protection when it drops to 0.5V. This pin must be connected to the GND when it is not going to be used.

## \*6. RF pins

These pins are used to set the current limit.

When the pin voltage exceeds 0.25V, the current is limited, and regeneration mode is established. In the application circuit, this voltage is set in such a way that the current limit will be established at 1A.

The calculation formula is given below.

RF resistance = 0.25V/target current limit value

All the RF pins (pins 24, 26 and 27) must be short-circuited on the print pattern.

## \*7. SOFTST pin

This pin is used to set the soft start.

By connecting a capacitor between this pin and GND, the motor speed can be increased gradually. When the pin voltage exceeds 2.5V, the soft start is released, and the LV8805V is switched to normal control. If the soft start function is not going to be used, connect the pin to the VREG pin.

### \*8. OSC pin

This pin is used to connect the capacitor for setting the startup frequency.

A capacitor with a capacitance ranging from about 500pF to 2,200pF (reference value) must be connected between this pin and GND.

The OSC pin determines the motor startup frequency, so be sure to connect a capacitor to it.

<How to select the capacitance>

Select a capacitance value that will result in the shortest possible startup time for achieving the target speed and produce minimal variations in the startup time. If the capacitance is too high, variations in the startup time will increase; conversely, if it is too low, the motor may idle. The optimum OSC constant depends on the motor characteristics and startup current, so be sure to recheck them when the type of motor used or circuit specifications are changed.

## \*9. VG, CP, and CPC pins

These pins are used to connect the capacitors to generate the pre-drive voltage and stabilize the pre-drive power supply.

Be sure to connect these capacitors in order to generate the drive voltage for the high-side (upper) output DMOS transistor.

## \*10. VREG pins

These are the control system power supply pin and regulator output pin, which create the power supply of the control unit. Be sure to connect a capacitor between this pin and GND in order to stabilize control system operation. Since these pins are used to supply current for control and generate the charge pump voltage, connect a capacitor with a capacitance that is higher than that of the capacitor connected to the charge pump. Both the VREG pins (pins 3 and 4) must be short-circuited on the print pattern.

#### \*11. Pin protection resistor

It is recommended that resistors higher than  $1k\Omega$  are connected serially to protect pins against misconnection such as GND open and reverse connection.

## **ORDERING INFORMATION**

Device	Package	Shipping (Qty / Packing)	
LV8805V-MPB-H	LV8805V-MPB-H SSOP36J (275mil) (Pb-Free / Halogen Free)		
LV8805V-TLM-H	SSOP36J (275mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel	

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC modults for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent reg