Data Sheet | January 30, 2007 | FN6427.0

Low Jitter Clock Generators for Set-Top Box

The ISL14011 series of devices are general purpose integrated Clock Synthesizers and Generators suited for consumer applications such as Set-top Box, and various other consumer applications.

The selectable reference input accepts 30MHz signal either from crystal or an external source. It is specified to operate with a nominal 3.3V supply and is offered in 16 Ld QFN package.

Contact Factory for other output frequency options.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL14011IRZ*	11IZ	-40 to +85	16 Ld QFN	L16.3x3

*Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Selection Table

PART OPTIONS	INPUT FREQUENCY	NUMBER OF OUTPUTS	OUTPUT FREQUENCY	PACKAGE
ISL14011	30MHz	4 LVTTL	25, 30, 24, 27	16 Ld QFN

Features

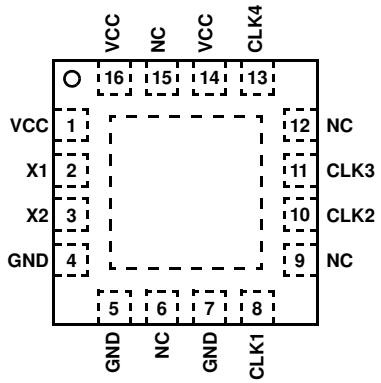
- LVTTL Outputs
- Selectable Crystal or Ref. Clock for Inputs
- Period Jitter ~50ps RMS
- Single Supply; 3.3V nominal
- Extended Temperature Range: -40°C to +85°C
- Available in small foot print package
  - 16 Ld QFN 3mmx3mm
- Pb-Free plus anneal available (RoHS Compliant)

Applications

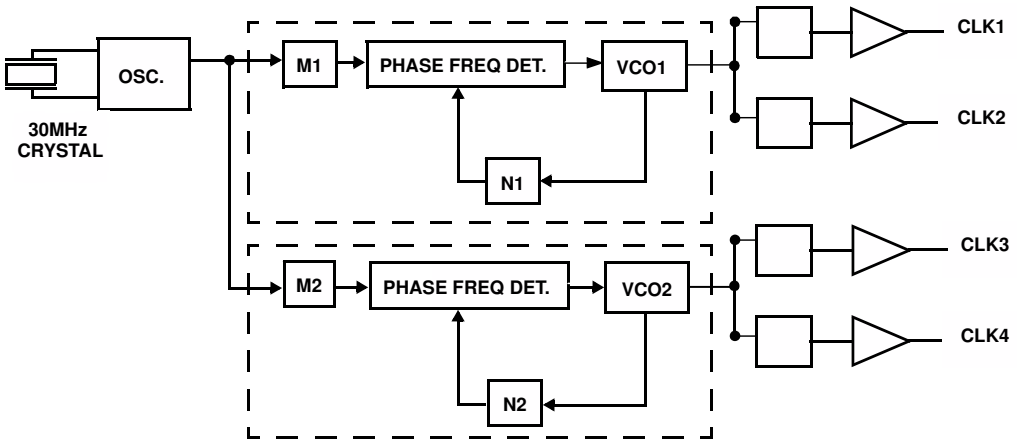
- Set-Top Boxes

Pinout

ISL14011
(16 LD QFN)
TOP VIEW



Functional Block Diagram



Pin Description

16 LD QFN	SYMBOLS	PIN DESCRIPTION
1,14,16	VCC	Supply Voltage
2	X1	The X1 pin is the terminal 1 of an external 30MHz crystal. This pin is grounded for external CK input.
3	X2	The X2 pin is the terminal 2 of external 30MHz crystal, or external clock input.
4, 5, 7	GND	Ground
8	CLK1	CLK1 Output: 25MHz
10	CLK2	CLK2 Output: 30MHz
11	CLK3	CLK3 Output: 24MHz
13	CLK4	CLK4 Output: 27MHz
6, 9,12,15	NC	No Connect

Absolute Maximum Ratings

Voltage on VCC, CLK pins (respect to Gnd) . . . . . -0.3V to 4.0V
Voltage on X1, X2 pins (respect to Gnd) . . . . . -0.3V to 2.5V
ESD Rating
MIL STD-883, Method 3014 . . . . . >±5kV
Machine Model . . . . . >500V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package	59	11.5

Storage Temperature . . . . . -65ºC to +150ºC
Lead Temperature (Soldering 10s) . . . . . +300ºC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

DC Electrical Specifications

V_{CC} = 3.3V ±10%, T_A = -40ºC to +85ºC, Typical values are at T_A = +25ºC and V_{CC} = 3.3V, Unless otherwise noted

SYMBOL	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Supply Voltage	3.0	3.3	3.6	V
Supply Current	I_{CC}	Supply Current CL = 5pF on all outputs		11	15	mA
CLOCK INPUT X_2 (X_1 GROUNDED) FOR EXTERNAL CLOCK MODE						
Input High Level	V_{IH}		1.5		2.4	V
Input Level Low	V_{IL}				0.5	V
Input Current	IIL, IIH	V_{X2} to Ground		0.5		mA
CLOCK OUTPUTS (CLK)						
Output High Level	V_{OH}	I_{OH} = -100µA	V_{CC}-0.2			V
		I_{OH} = -4mA	2.4			V
		I_{OH} = -6mA	2.1			V
Output Low Level	V_{OL}	I_{OL} = 100µA			0.2	V
		I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.75	V
Output Short Circuit Current	IOSC	CLK = V_{CC} or Gnd	6	13	30	mA

AC Electrical Specifications

CL= 5pF on all outputs

SYMBOL	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Crystal Frequency	fin			30		MHz
CLOCK OUTPUTS						
Rise Time	t_R	20% to 80% V_{CC}		1.8		ns
Fall Time	t_F	80% to 20% V_{CC}		1.8		ns
Duty Cycle			40		60	%
Period Jitter	J_P	RMS		50		ps
Power Up Time	t_{PO}	V_{CC} >2.7V		2		ms

Typical Performance Curves (Period Jitter)

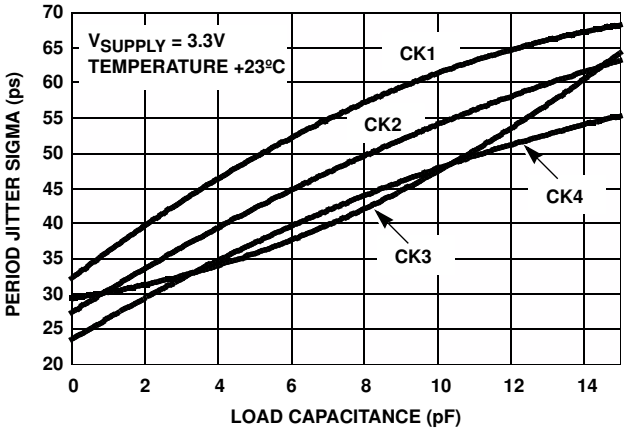
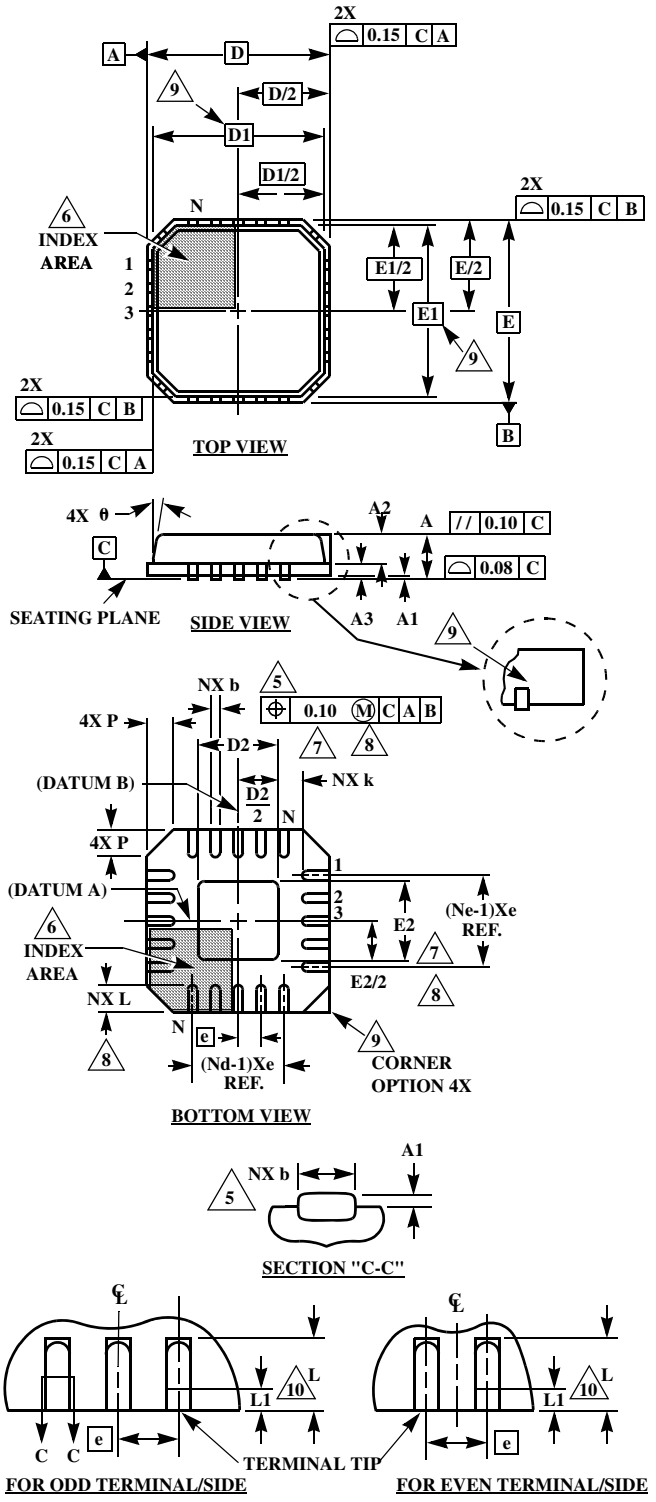


FIGURE 1. STANDARD DEVIATION vs LOAD CAPACITANCE

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.3x3

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		3.00 BSC		-
D1		2.75 BSC		9
D2	1.35	1.50	1.65	7, 8, 10
E		3.00 BSC		-
E1		2.75 BSC		9
E2	1.35	1.50	1.65	7, 8, 10
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VEED-2 Issue C, except for the E2 and D2 MAX dimension.