

4-Lines, Bi-directional Ultra-low Capacitance ESD Protection Array

DESCRIPTIONS

The TESDH3V3B02P4Q2 is a design which includes ESD rated diode arrays to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-voltage damage caused by Electrostatic Discharging (ESD).

TESDH3V3B02P4Q2 incorporates four pair of ultra-low capacitance steering diodes. During transient conditions, the steering diodes direct the transient to either the internal ESD line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

The TESDH3V3B02P4Q2 may be used to provide ESD protection up to $\pm 10\text{kV}$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 5.5A (8/20 μs) according to IEC61000-4-5

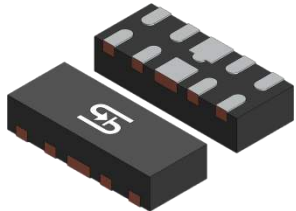
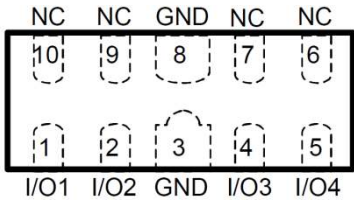
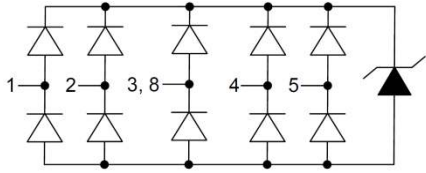
FEATURES

- ESD protect for 4 line with bidirectional
- Provide ESD protection for each channel to IEC61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 10\text{kV}$ (contact) IEC61000-4-5 (Lightning): 5.5A (8/20 μs)
- Suitable for $\pm 3.3\text{V}$ and below, operating voltage applications
- Ultra-low capacitance: $C_J = 0.21\text{pF}$ (typ.)
- Ultra-low leakage current
- Low voltage: $V_{CL} = 9\text{V}$ (typ.)@ $I_{TLP} = 16\text{A}$
- Protect one I/O line
- Fast turn-on and Low clamping voltage
- Moisture sensitivity level: level 3, per J-STD-020
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

APPLICATION

- USB 3.0 and USB 3.1
- HDMI 1.3 ,HDMI 1.4 and HDMI2.0
- SATA and eSATA
- DisplayPort interface
- Portable Electronics
- Notebooks



PACKAGE: DFN2510-10L	PIN CONFIGURATION	CIRCUIT DIAGRAM																				
	 <table border="1" data-bbox="587 1720 1018 1874"> <tr> <td>PIN 1</td> <td>I/O1</td> <td>PIN 6</td> <td>NC</td> </tr> <tr> <td>PIN 2</td> <td>I/O2</td> <td>PIN 7</td> <td>NC</td> </tr> <tr> <td>PIN 3</td> <td>GND</td> <td>PIN 8</td> <td>GND</td> </tr> <tr> <td>PIN 4</td> <td>I/O3</td> <td>PIN 9</td> <td>NC</td> </tr> <tr> <td>PIN 5</td> <td>I/O4</td> <td>PIN 10</td> <td>NC</td> </tr> </table>	PIN 1	I/O1	PIN 6	NC	PIN 2	I/O2	PIN 7	NC	PIN 3	GND	PIN 8	GND	PIN 4	I/O3	PIN 9	NC	PIN 5	I/O4	PIN 10	NC	
PIN 1	I/O1	PIN 6	NC																			
PIN 2	I/O2	PIN 7	NC																			
PIN 3	GND	PIN 8	GND																			
PIN 4	I/O3	PIN 9	NC																			
PIN 5	I/O4	PIN 10	NC																			

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power ($t_p = 8/20\mu\text{s}$)	P_{PK}	33	W
Peak pulse current ($t_p = 8/20\mu\text{s}$)	I_{PP}	5.5	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 15	kV
ESD according to IEC61000-4-2 contact discharge		± 10	kV
Junction temperature	T_J	125	$^\circ\text{C}$
Operating temperature range	T_{OP}	-40 to +85	$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 to +150	$^\circ\text{C}$

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Reverse working voltage		V_{RWM}	-	-	3.3	V
Reverse breakdown voltage	$I_R = 100\mu\text{A}$, $T_J = 25^\circ\text{C}$	V_{BR}	9	-	12	V
Reverse leakage current	$V_{RWM} = 3.3\text{V}$, $T_J = 25^\circ\text{C}$	I_R	-	-	100	nA
Clamping voltage ⁽¹⁾	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$	V_C	-	-	3.5	V
	$I_{PP} = 5.5\text{A}$, $t_p = 8/20\mu\text{s}$		-	-	6.0	V
Clamping voltage ⁽²⁾	$I_{TLP} = 16\text{A}$, $t_p = 100\text{ns}$	V_{CL}	-	9	-	V
Junction capacitance	$f = 1\text{MHz}$, $V_R = 1.5\text{V}$	C_J	-	0.21	0.28	pF
Dynamic resistance ⁽²⁾		R_{DYN}	-	0.40	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: $Z_0 = 50\ \Omega$, $t_p = 100\text{ns}$, $t_r = 2\text{ns}$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

ORDERING INFORMATION		
ORDERING CODE	PACKAGE	PACKING
TESDH3V3B02P4Q2 RIG	DFN2510-10L	3,000 / 7" Tape & Reel

CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature **Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time**

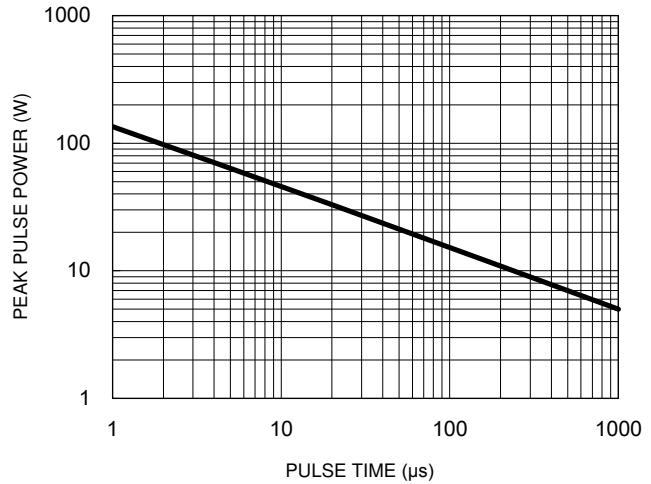
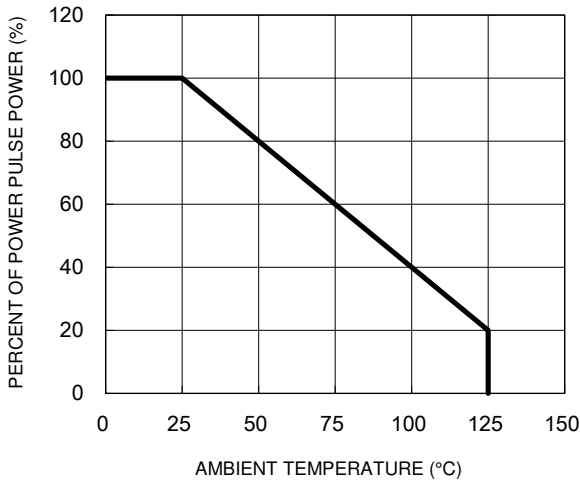


Fig.3 Clamping Voltage vs. Peak Pulse Current

Fig.4 Capacitance vs. Reverse Voltage

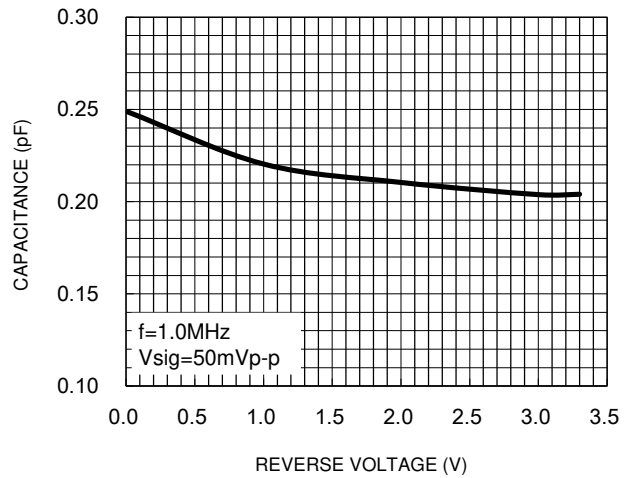
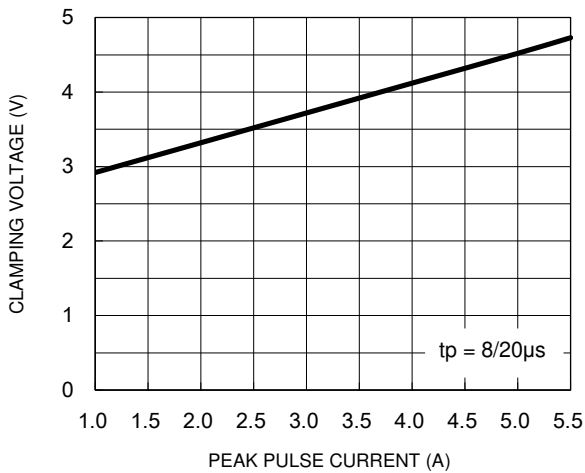
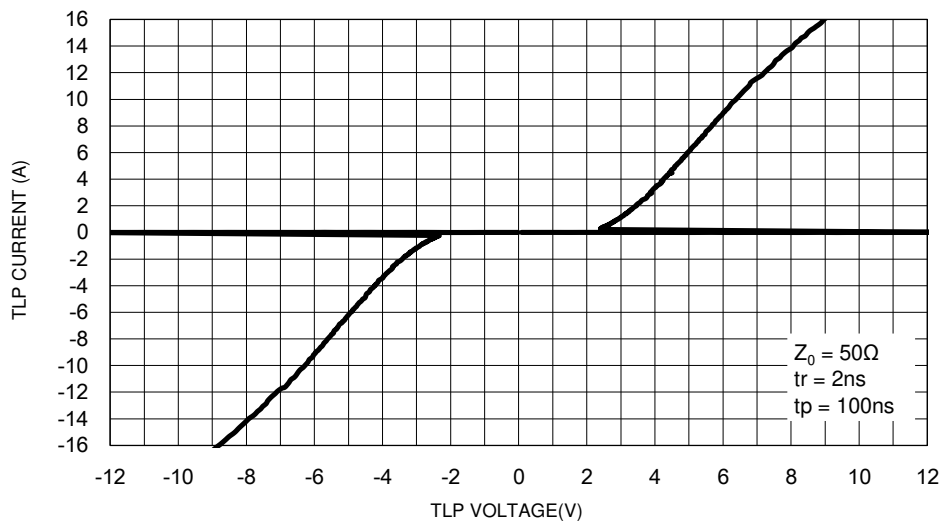


Fig.5 TLP Curve



CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig.6 8/20 μs pulse waveform per IEC61000-4-5

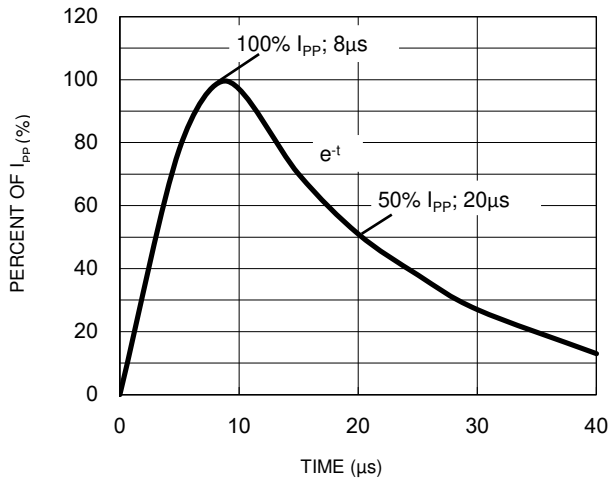
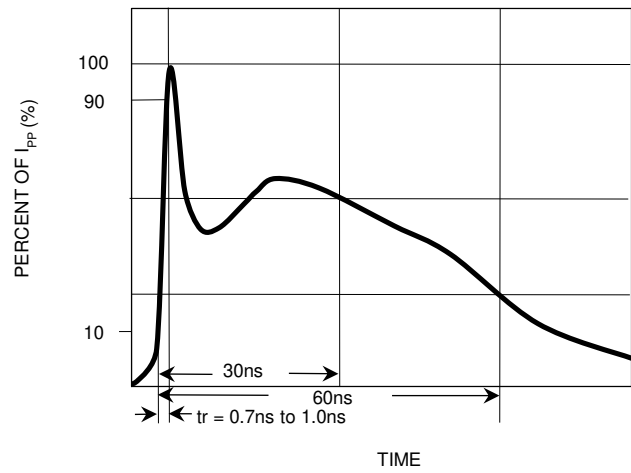


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

Device Connection

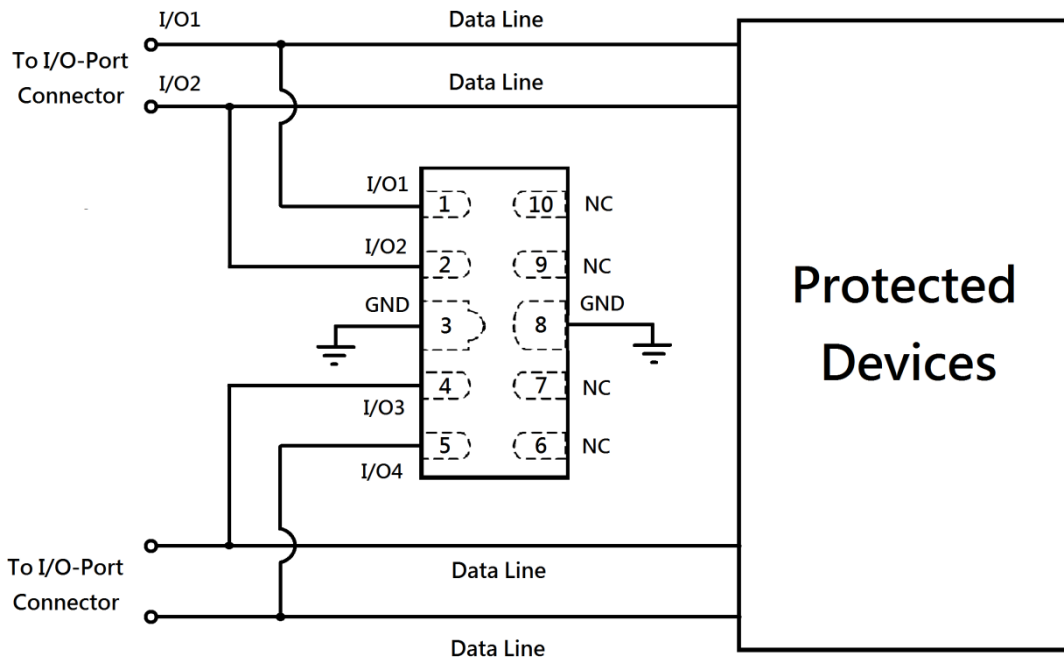
The TESDH3V3B02P4Q2 is designed to protect four data lines from transient over-voltage (such as ESD stress pulse).

The usage of the TESDH3V3B02P4Q2 is shown in Fig.1. The four protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, and pin5) of TESDH3V3B02P4Q2. The ground pins (pin3 and pin8) of TESDH3V3B02P4Q2 are the negative reference pins.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

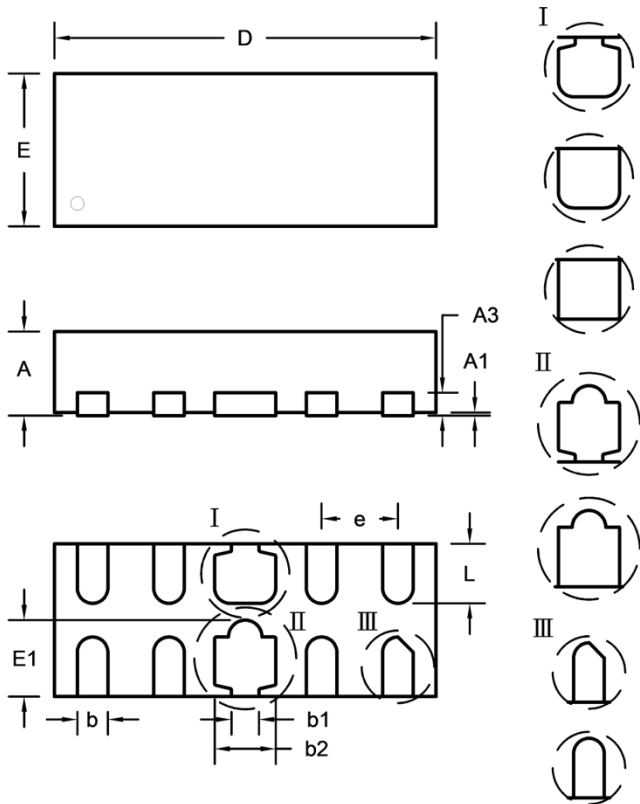
TESDH3V3B02P4Q2 can provide ESD protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

Fig.1 ESD protection by TESDH3V3B02P4Q2



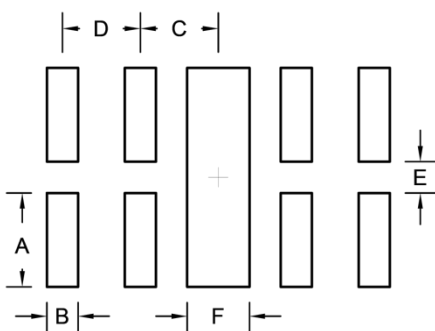
PACKAGE OUTLINE DIMENSIONS

DFN2510-10L



DIM.	Unit (mm)		Unit (inch)	
	Min.	Max.	Min.	Max.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.15 Ref.		0.006 Ref.	
b	0.15	0.25	0.006	0.010
b1	0.13	0.23	0.005	0.009
b2	0.35	0.45	0.014	0.018
D	2.40	2.60	0.094	0.102
E	0.90	1.10	0.035	0.043
E1	0.50 Ref.		0.020 Ref.	
e	0.50 BSC		0.020 BSC	
L	0.28	0.50	0.011	0.020

SUGGESTED PAD LAYOUT



Symbol	Unit (mm)	Unit (inch)
A	0.60	0.024
B	0.20	0.008
C	0.50	0.020
D	0.50	0.020
E	0.20	0.008
F	0.40	0.016

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

MARKING DIAGRAM



TG = Device Code
YW = Date Code

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Purchasers are solely responsible for the choice, selection, and use of TSC products and TSC assumes no liability for application assistance or the design of Purchasers' products.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.