HDMI Mezzanine Card – Revision B

User's Guide

September 2012
Revision: EB55_01.1

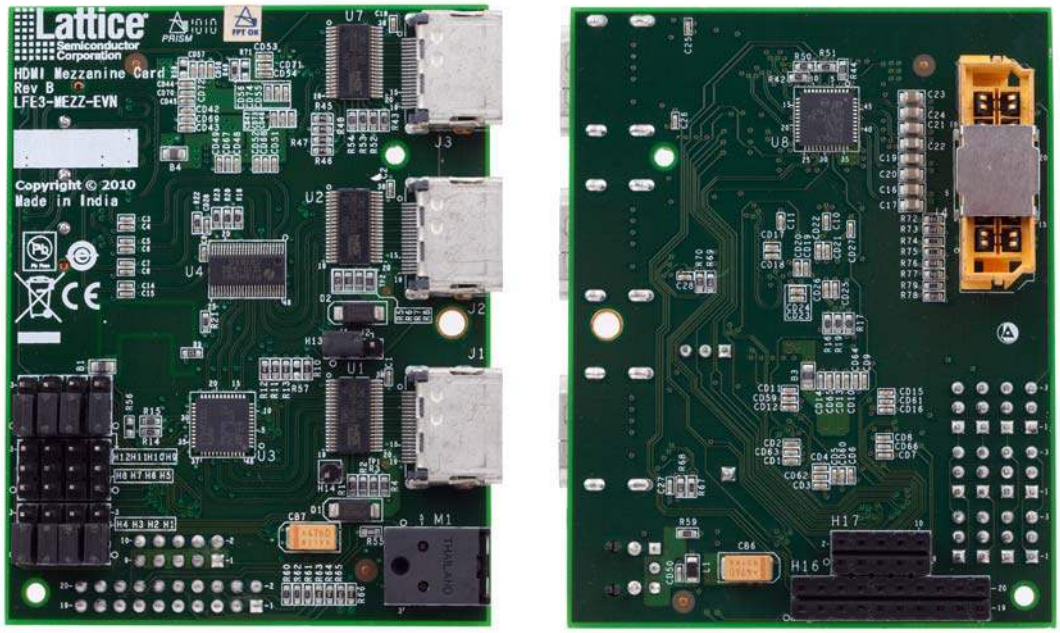
Introduction

LatticeECP3 Video Protocol Board includes a daughter card connection to support applications that can be implemented using SERDES. This daughter card connection includes three connectors for the signals of a whole SERDES quad, the control/status signals and the power/ground pins.

The HDMI Mezzanine Card is a LatticeECP3 Video Protocol Board daughter card designed for demonstrating the Lattice HDMI/DVI solution using LatticeECP3 SERDES. The scope of this user's guide covers only revision B of the HDMI Mezzanine Card. Please refer to EB52, LatticeECP3 Video Protocol Board Revision C User's Guide for more information about the LatticeECP3 device connection to the daughter card.

As shown in Figure 1, this card uses Single-Link 19-pin HDMI Type-A connectors. If using passive HDMI-to-DVI cables, this card can also be used to support DVI video.

Figure 1. HDMI Mezzanine Card



Features

- Supports two different HDMI/DVI input paths, with or without the cable equalizer
- Supports HDMI/DVI output with TMDS level shifter
- TOSLINK fiber optic receiving module for S/PDIF audio input
- Headers for HPD, CEC controls and the EDID signals
- ESD protection devices for both HDMI/DVI inputs and HDMI/DVI outputs

Functional Description

There are four transmit channels and four receive channels in each of the LatticeECP3 SERDES quads. For implementing a Single Link HDMI or DVI interface, which includes three data channels and one clock channel, all four transmit channels and three receive channels are used. The clock channel on the receive side is connected to the dedicated SERDES differential reference clock pins. Since the common mode voltage of the HDMI/DVI TMDS sig-

nals is different from the SERDES CML signals, and the TMDS coding scheme maintains the DC balance of the signal, the AC coupling capacitors are used to block the DC component of the driving signal.

Figure 2 shows the functional block diagram of the HDMI Mezzanine Card. For validation purposes, this card is designed to include two HDMI/DVI input ports. One of these input paths has a TMDS cable equalizer and the other does not. The signals of both paths will go into the 2-to-1 TMDS MUX, then the AC coupling capacitors to the SERDES input pins. Depending on which pins a shunt is installed on a 3-pin header, one of the two inputs will be selected and the signals will be fed to the SERDES.

For meeting the HDMI/DVI's strict electrical compliance test specification, a TMDS level shifter is added to the output path. This level shifter can be removed if the design does not have this requirement. The ESD protector is added on both the input and output HDMI/DVI ports. Other than the HDMI/DVI, an S/PDIF input interface is also included for bringing in a digital audio stream through the TOSLINK connector.

Figure 2. Functional Block Diagram

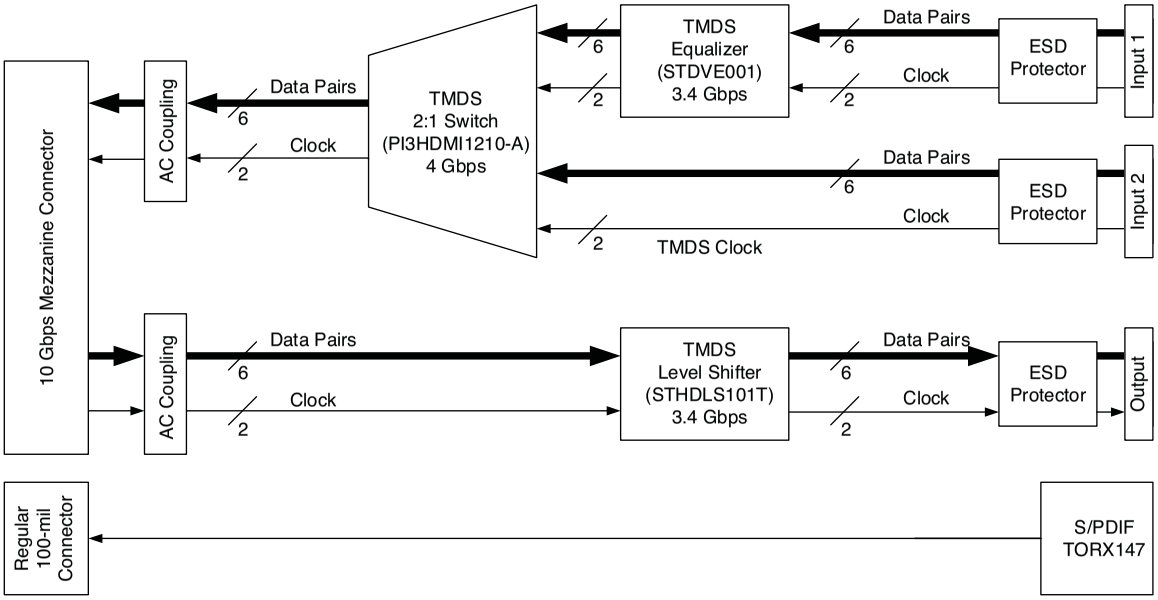
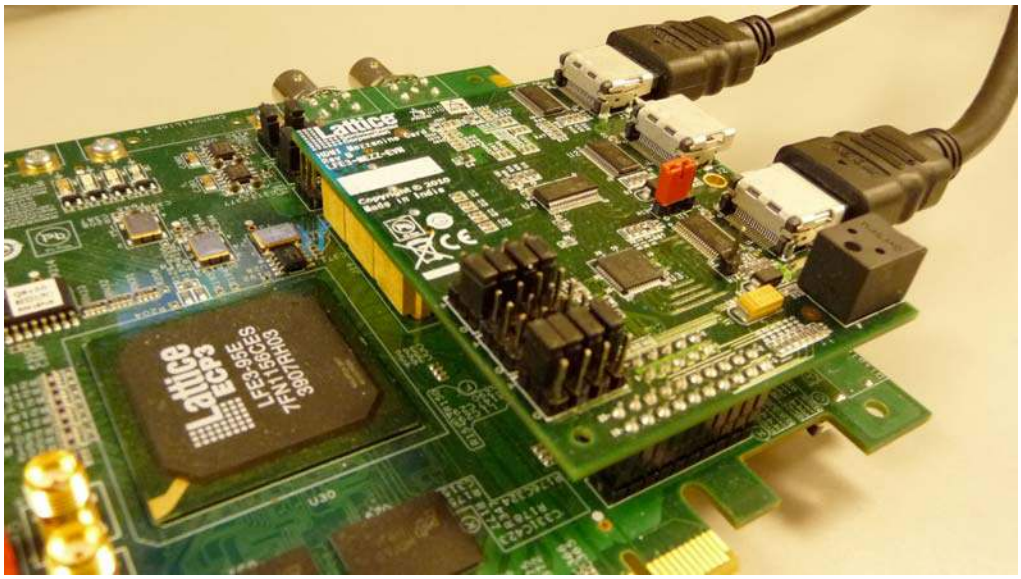


Figure 3 shows the HDMI Mezzanine Card installed on the LatticeECP3 Video Protocol Board. The two cables are the HDMI cables connecting to J1 (HDMI/DVI input) and J3 (HDMI/DVI output) of the daughter card. A 12 mm tall standoff is recommended for securing the HDMI Mezzanine Card on the LatticeECP3 Video Protocol Board through screws.

Figure 3. HDMI Mezzanine Card Installed on the LatticeECP3 Video Protocol Board



Header Settings

This section describes the header settings on the HDMI Mezzanine Card. However, since the card uses SERDES quad C when plugging into the LatticeECP3 Video Protocol Board, the VCCOB and the VCCIB of SERDES quad C need to be powered properly. Please make sure shuts are installed on J18 and J22 of the LatticeECP3 Video Protocol Board.

As mentioned previously, the selection of the two HDMI/DVI inputs is done by a 3-pin header. Table 1 shows the locations of where the shunt should be installed.

Table 1. MUX Selection Control

HDMI/DVI Input	Mode	MUX Select	Shunt Installation on H13
J1	Equalized HDMI/DVI Input	High	Pin 1/Pin 2
J2	Non-Equalized HDMI/DVI Input	Low	Pin 2/Pin 3

Other than the TMDS clock and data pairs, the HDMI/DVI interface includes CEC, HPD and the DDC clock and data signals. By installing shuts on different locations of the 12 headers, these signals can be selected to be bypassed from the HDMI/DVI input to the HDMI/DVI output, or they can be selected to be connected to the LatticeECP3 FPGA on the LatticeECP3 Video Protocol Board.

Figure 4 shows the locations of these 12 headers on the HDMI Mezzanine Card and the signals these headers control. The 12 headers are divided into four groups as shown in Figure 4. Each group includes three headers for controlling one of the four signals. The black square is used to indicate pin 1 of each header.

Figure 4. Headers for CEC, HDP, S Settings, LatticeECP3 Video Protocol Board

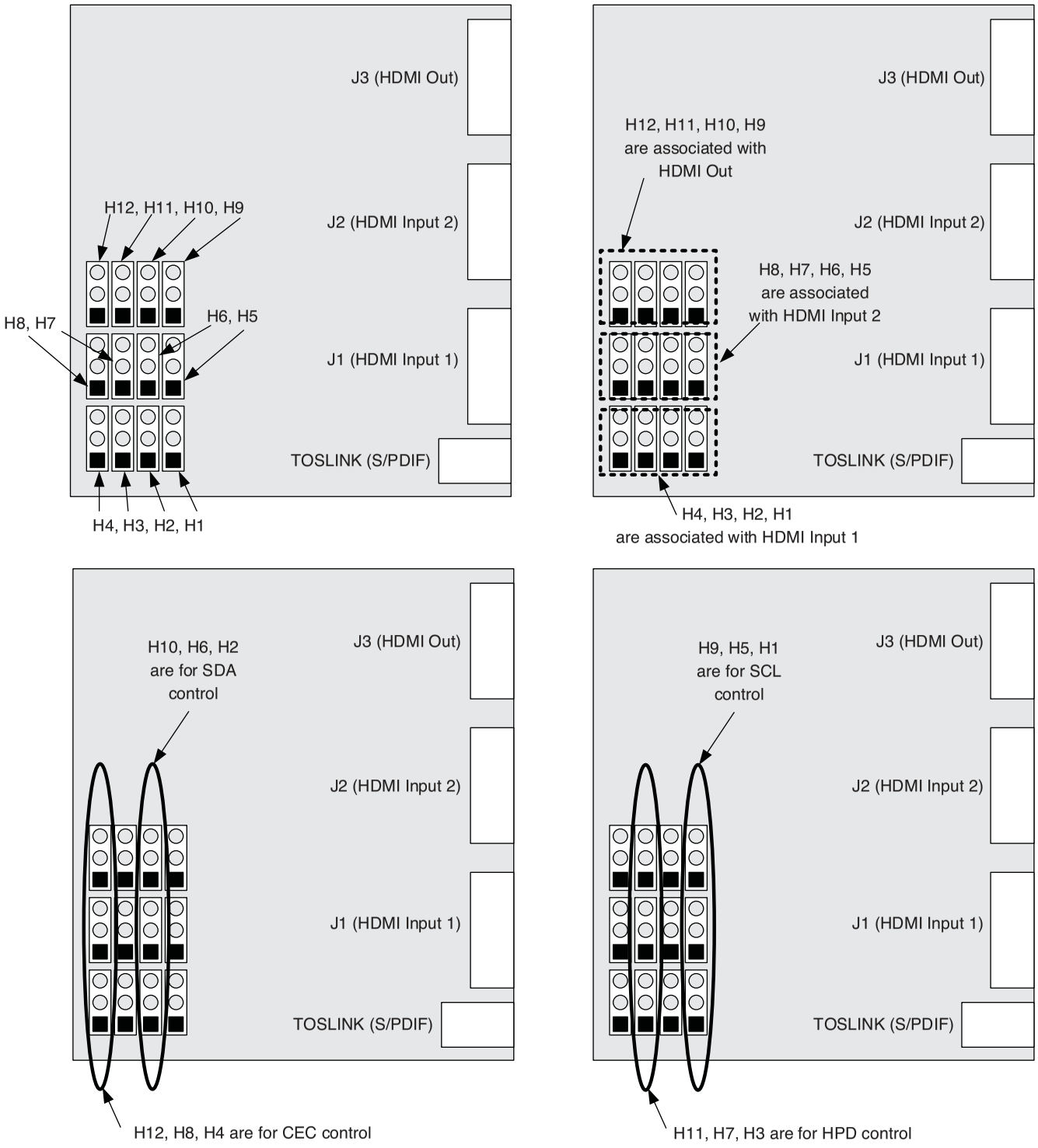


Figure 5 is a conceptual connection of the header connections. This applies to all four signals. An example of the connection is shown in Figure 6. In this example, the shunts are installed on pin1/pin 2 of H9 ~ H12 and pin2/pin3 of H1 ~ H4. This will bypass the four signals between J1 and J3.

Figure 5. Conceptual Connection for Headers H1 to H12

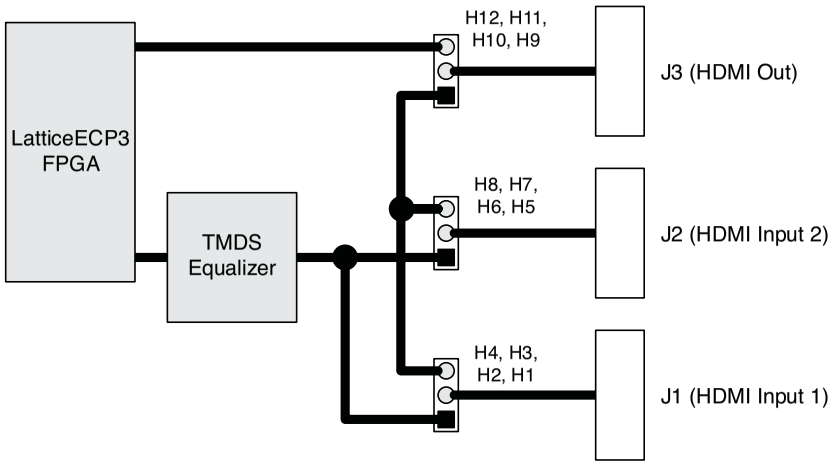
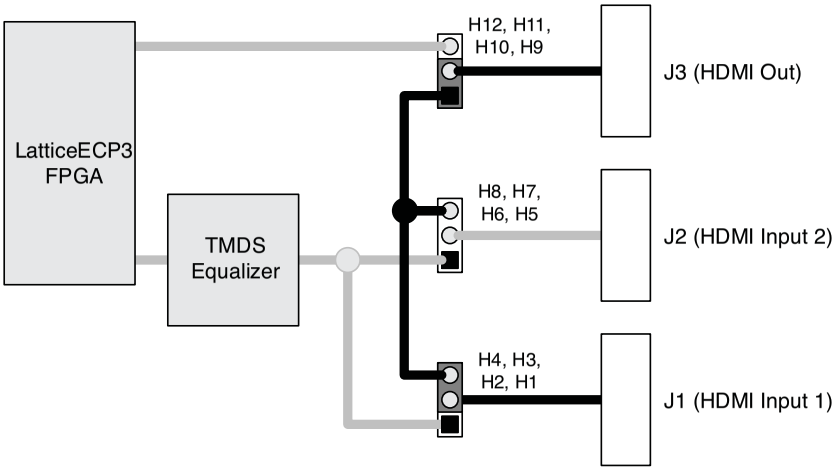


Figure 6. Example for Bypassing CEC, HPD, SDA, SCL Between J1 and J3



Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2010	01.0	Initial release.
September 2012	01.1	Added Appendix B. Hardware Variants.
		Updated document with new corporate logo.

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Appendix A. Schematic

Figure 7. Cover Page

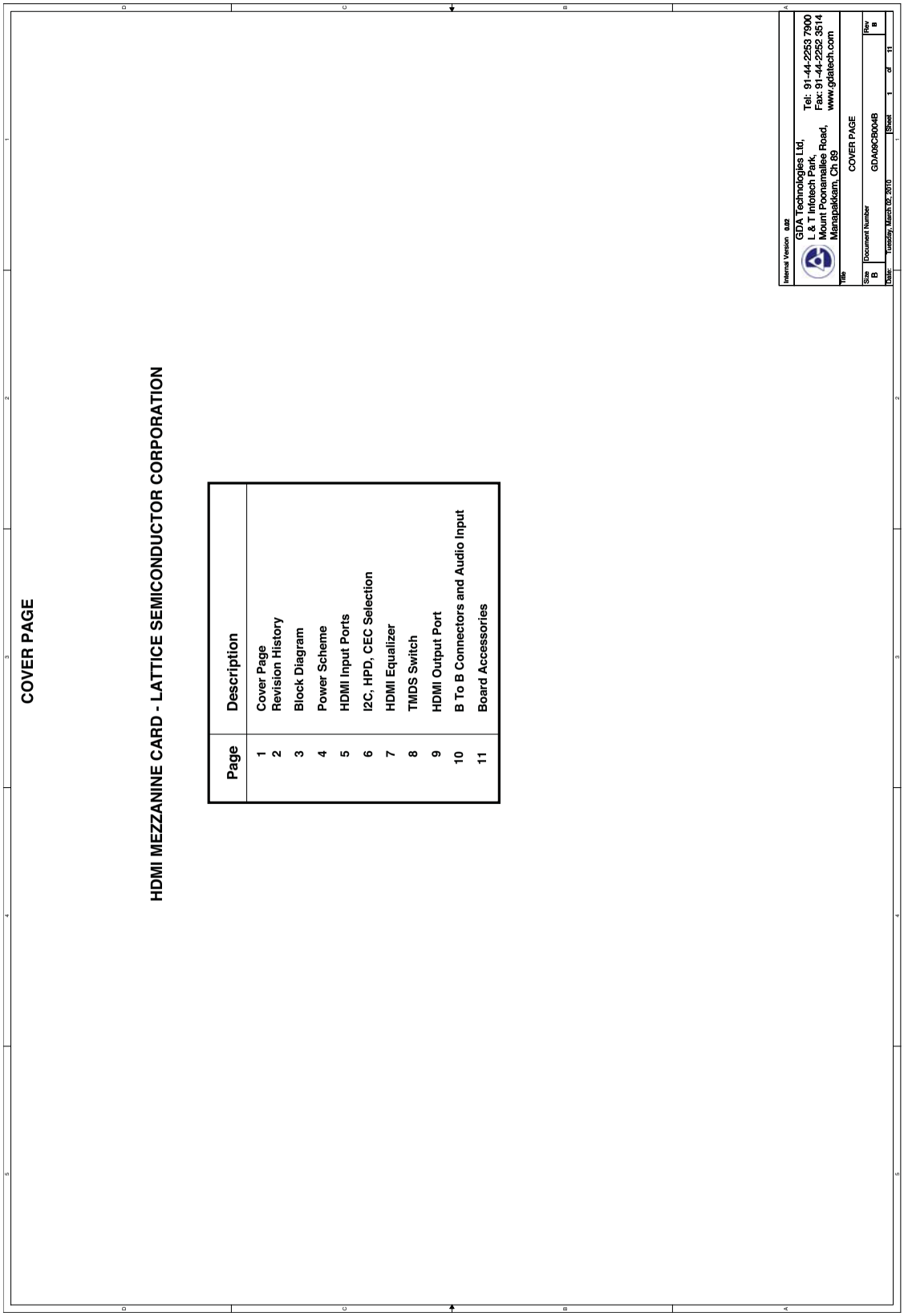
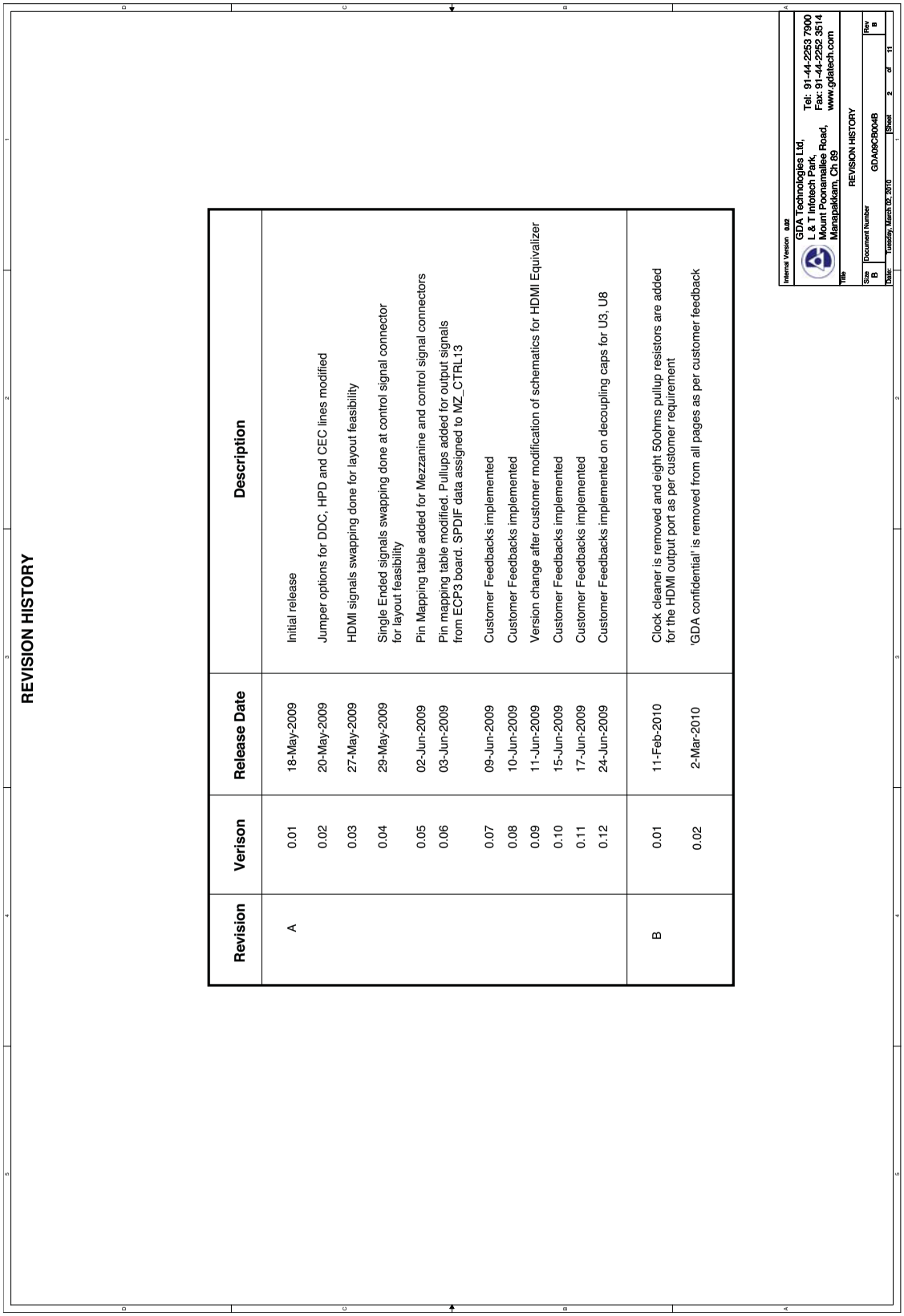


Figure 8. Revision History



REVISION HISTORY

Revision	Verison	Release Date	Description
A	0.01	18-May-2009	Initial release
	0.02	20-May-2009	Jumper options for DDC, HPD and CEC lines modified
	0.03	27-May-2009	HDMI signals swapping done for layout feasibility
	0.04	29-May-2009	Single Ended signals swapping done at control signal connector for layout feasibility
	0.05	02-Jun-2009	Pin Mapping table added for Mezzanine and control signal connectors
	0.06	03-Jun-2009	Pin mapping table modified. Pullups added for output signals from ECP3 board. SPDIF data assigned to MZ_CTRL13
	0.07	09-Jun-2009	Customer Feedbacks implemented
	0.08	10-Jun-2009	Customer Feedbacks implemented
	0.09	11-Jun-2009	Version change after customer modification of schematics for HDMI Equivalizer
	0.10	15-Jun-2009	Customer Feedbacks implemented
	0.11	17-Jun-2009	Customer Feedbacks implemented
	0.12	24-Jun-2009	Customer Feedbacks implemented on decoupling caps for U3, U8
B	0.01	11-Feb-2010	Clock cleaner is removed and eight 50ohms pullup resistors are added for the HDMI output port as per customer requirement
	0.02	2-Mar-2010	'GDA confidential' is removed from all pages as per customer feedback

Figure 9. Block Diagram

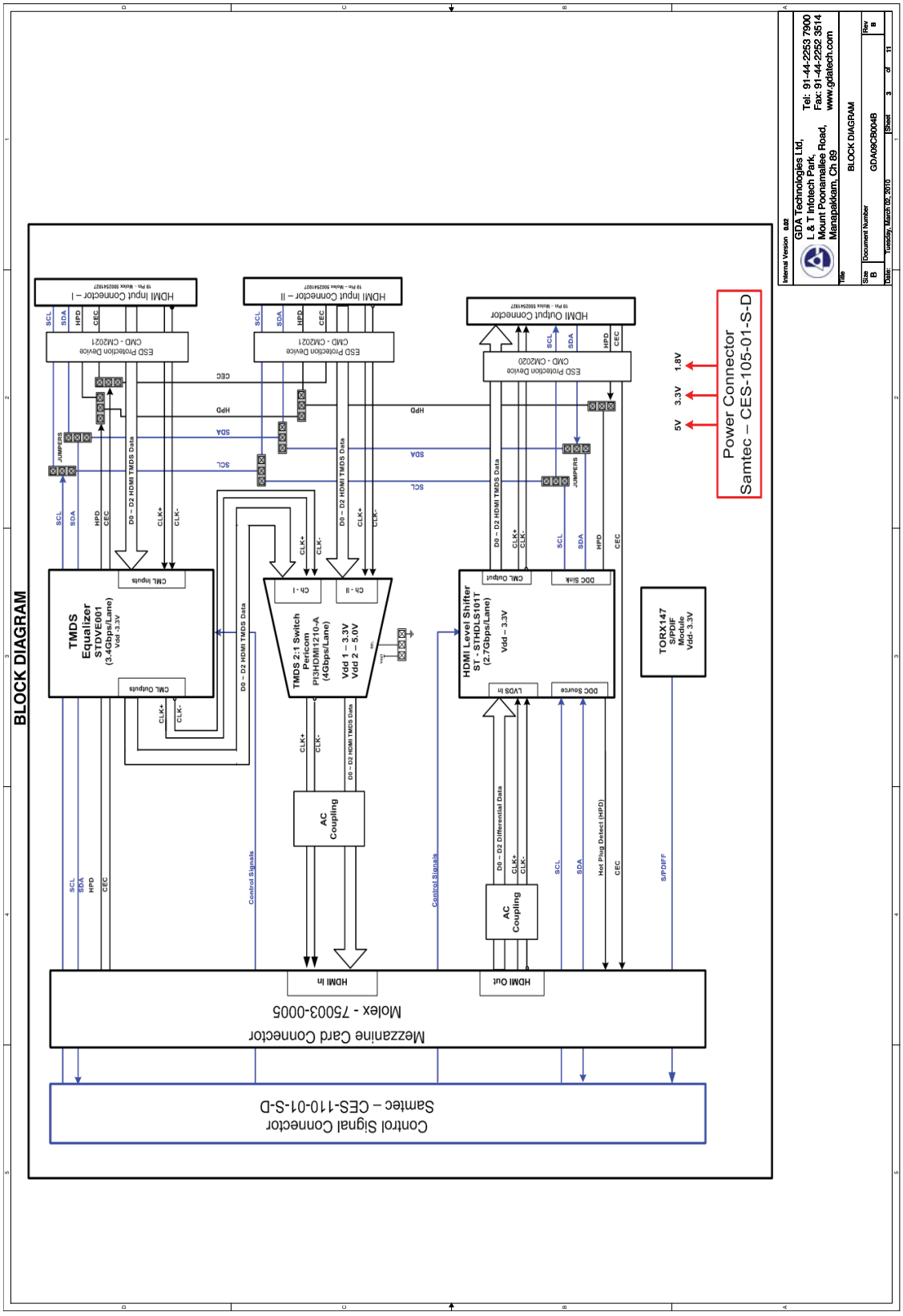


Figure 10. Power Scheme

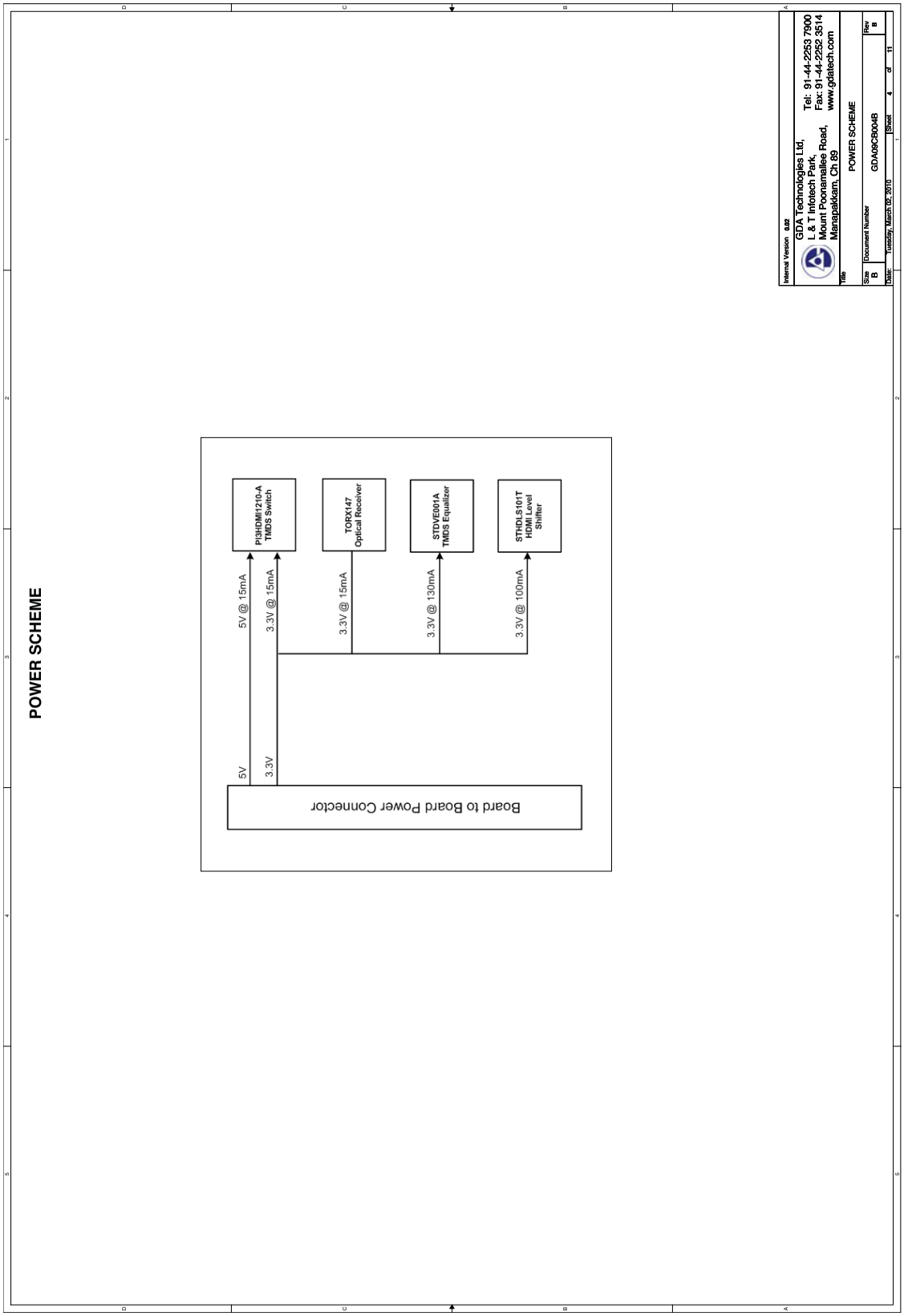
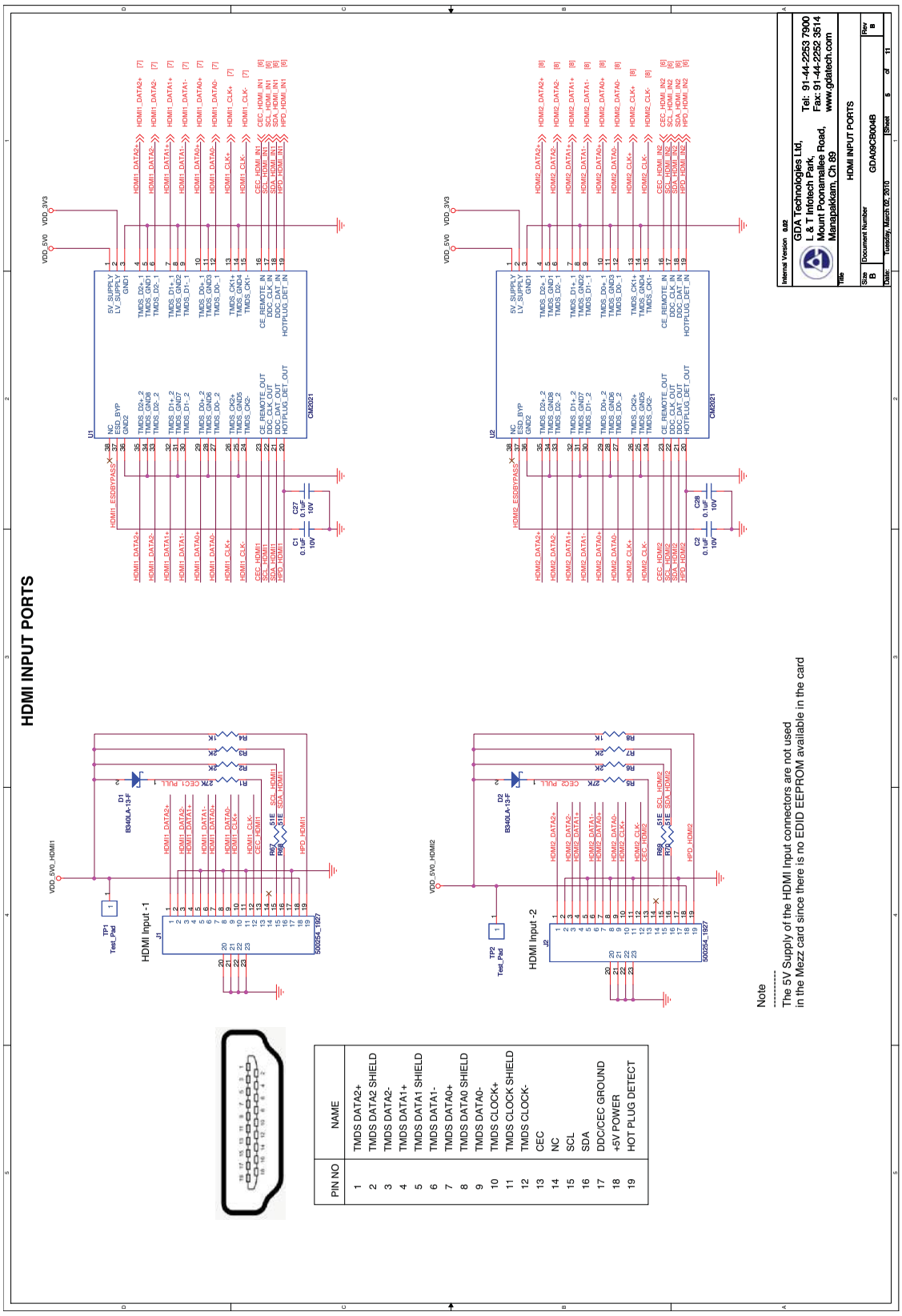


Figure 11. HDMI Input Ports



PIN NO	NAME
1	TMDS DATA2+
2	TMDS DATA2 SHIELD
3	TMDS DATA2-
4	TMDS DATA1+
5	TMDS DATA1 SHIELD
6	TMDS DATA1-
7	TMDS DATA0+
8	TMDS DATA0 SHIELD
9	TMDS DATA0-
10	TMDS CLOCK+
11	TMDS CLOCK SHIELD
12	TMDS CLOCK-
13	CEC
14	NC
15	SCL
16	SDA
17	DDC/CEC GROUND
18	+5V POWER
19	HOT PLUG DETECT

Figure 12. I²C, HPD, CEC Selection

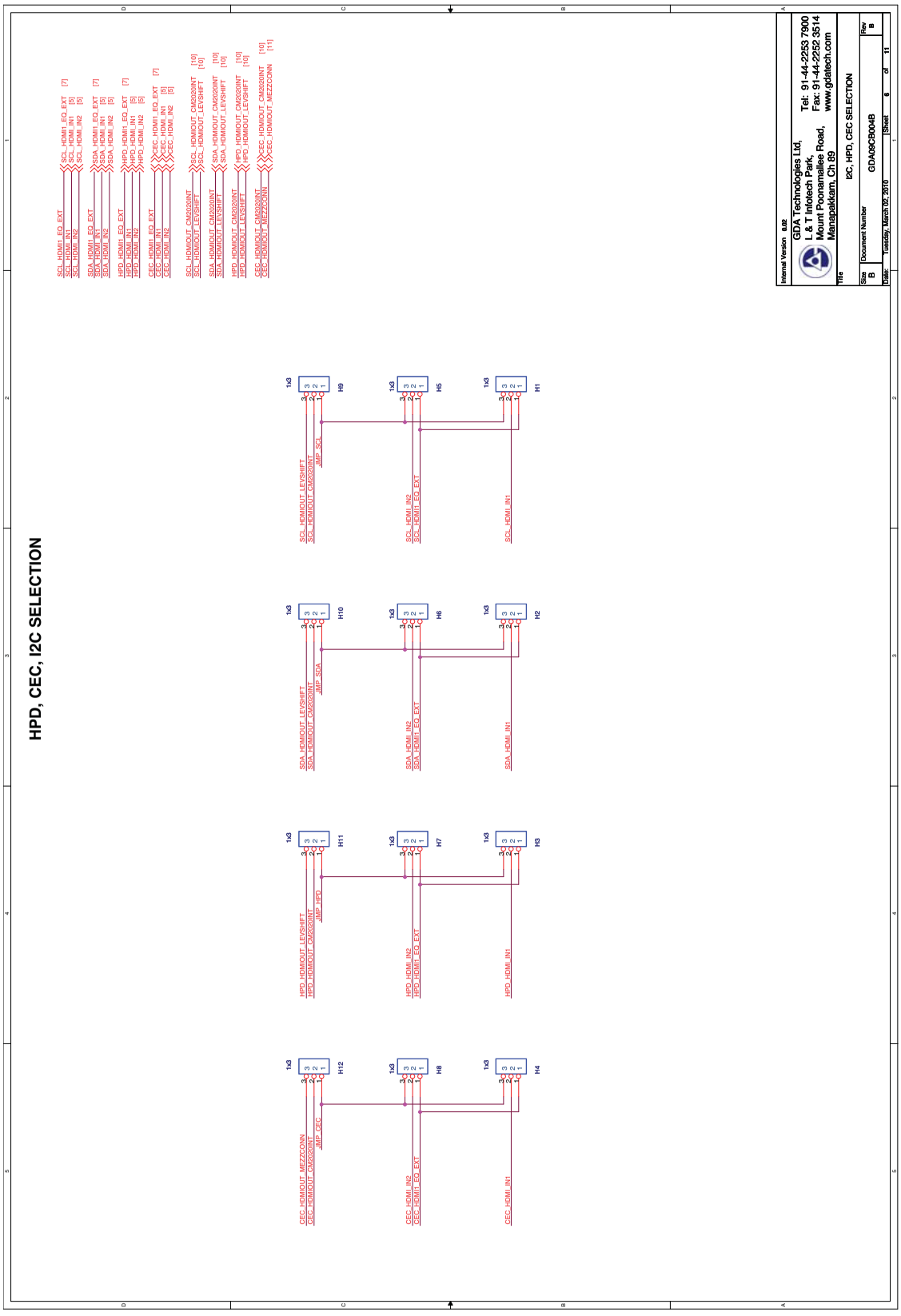


Figure 13. HDMI Equalizer

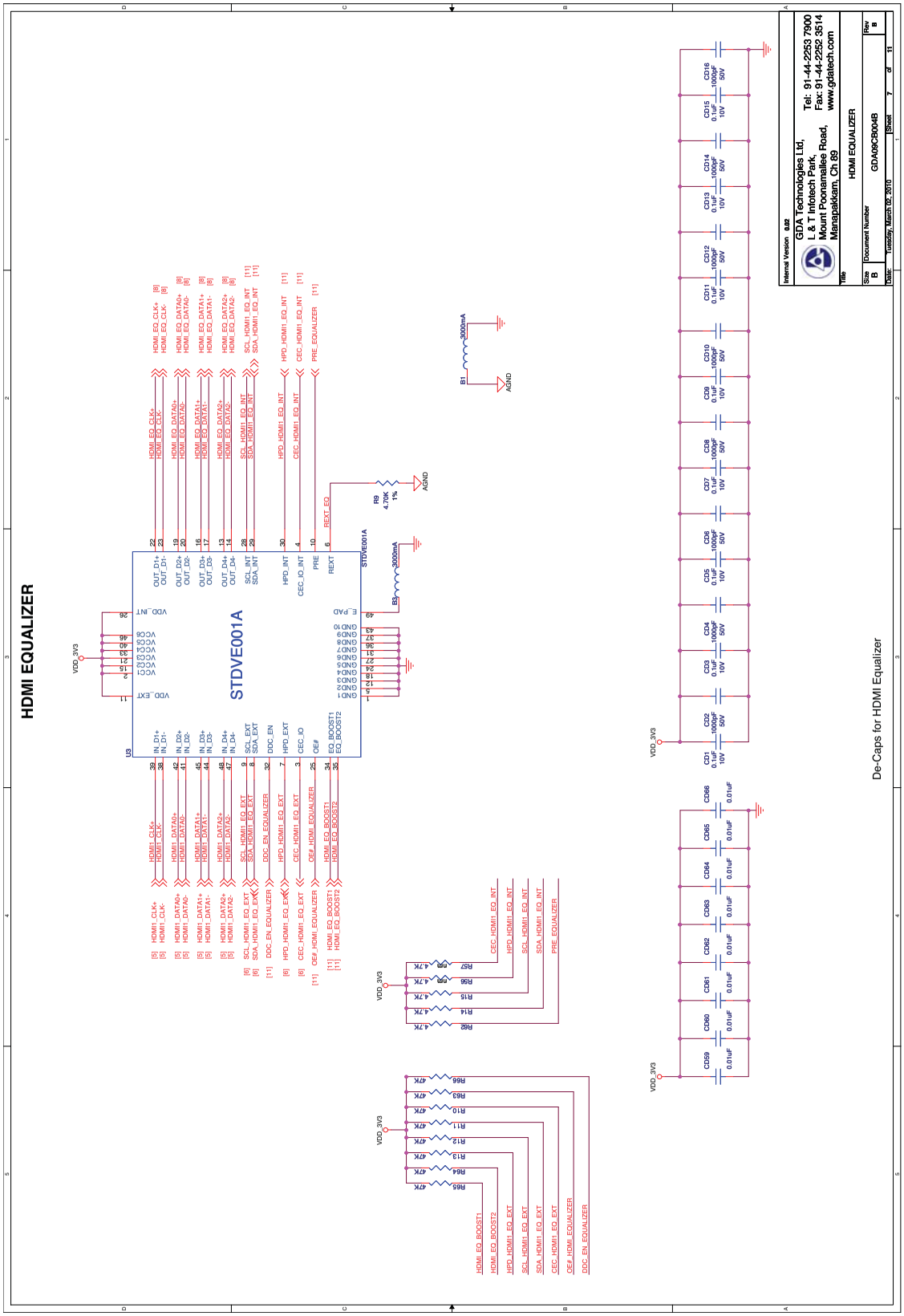


Figure 14. TMDS Switch

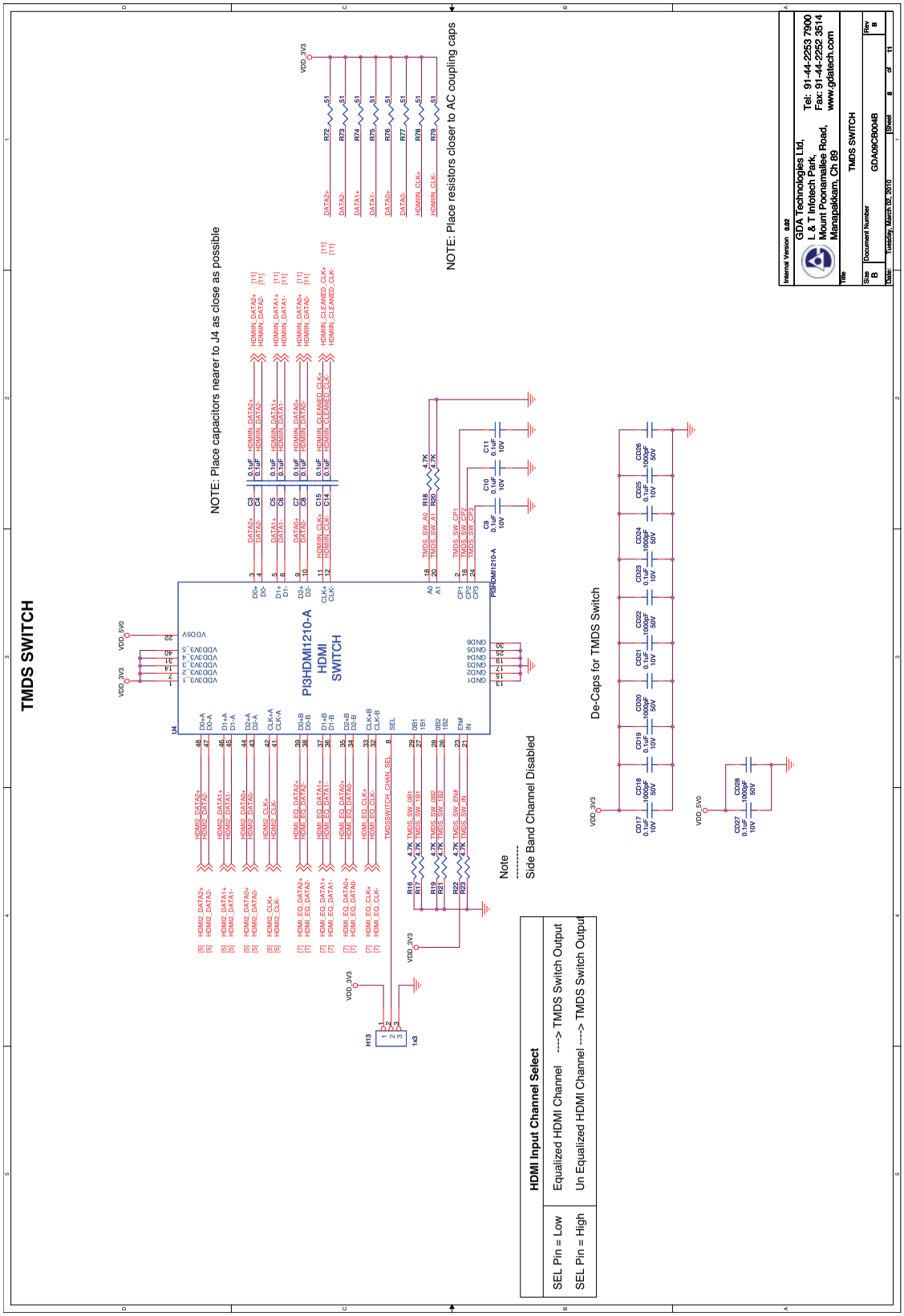


Figure 15. HDMI Output Port

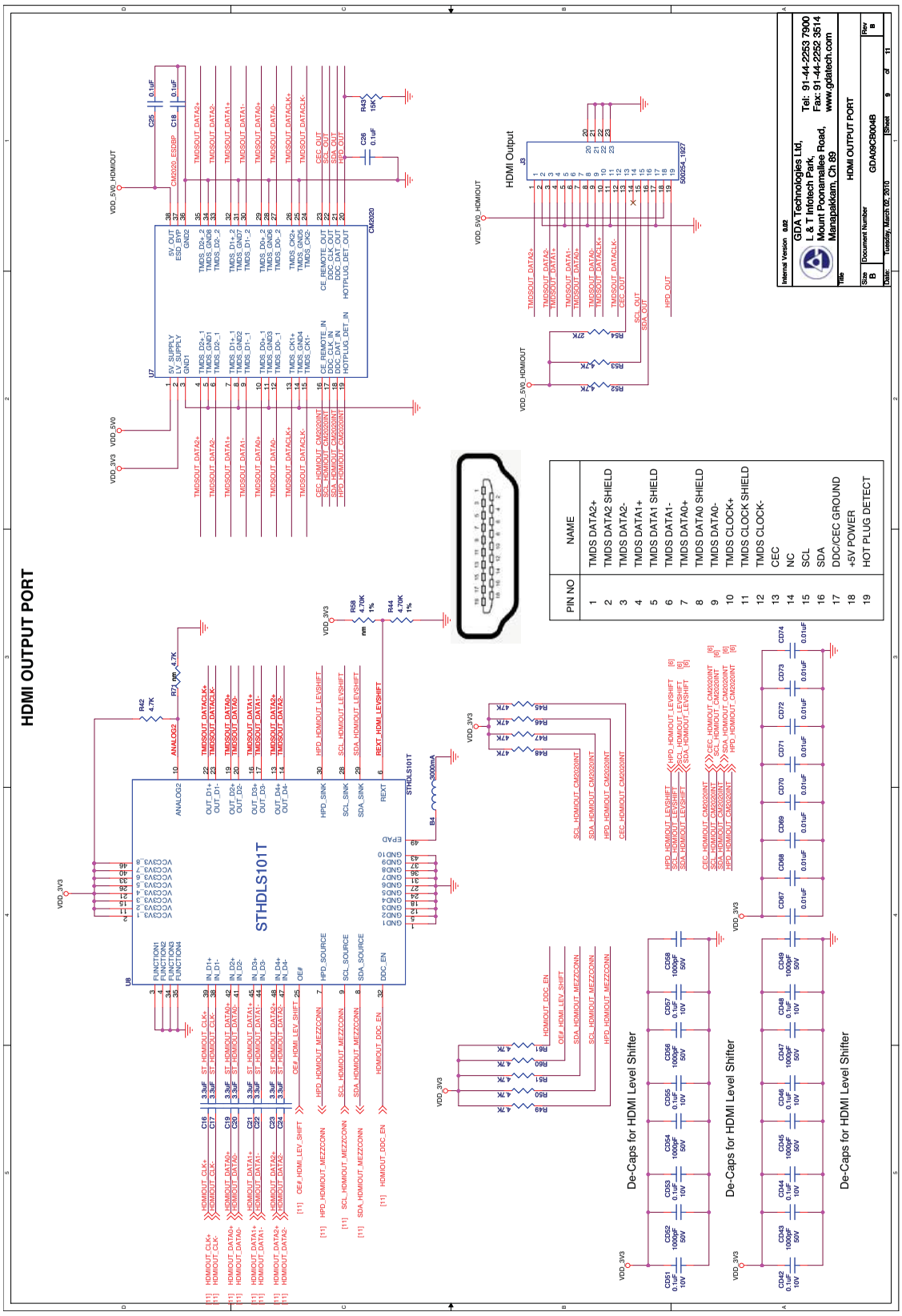


Figure 16. B to B Connectors and Audio In

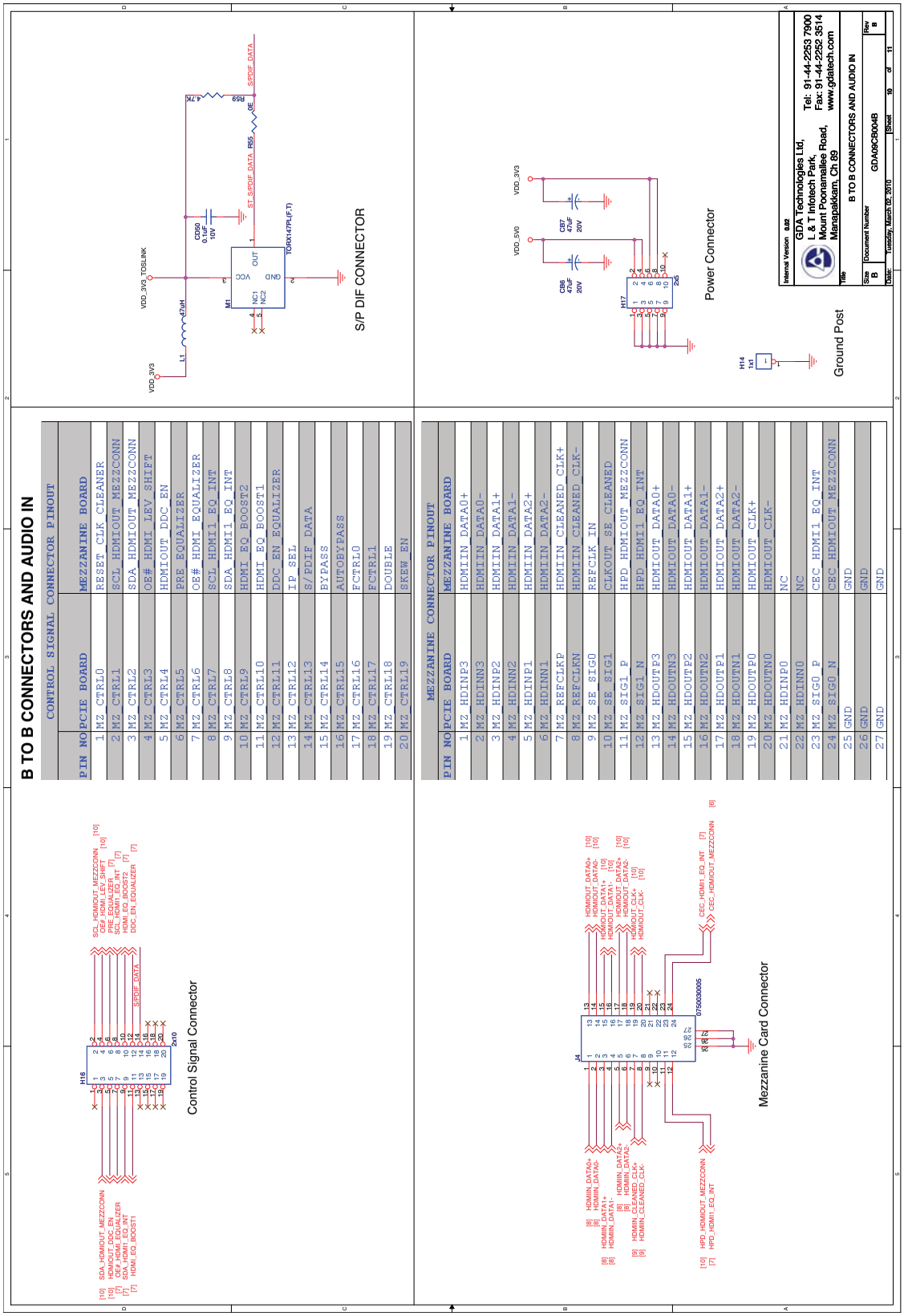
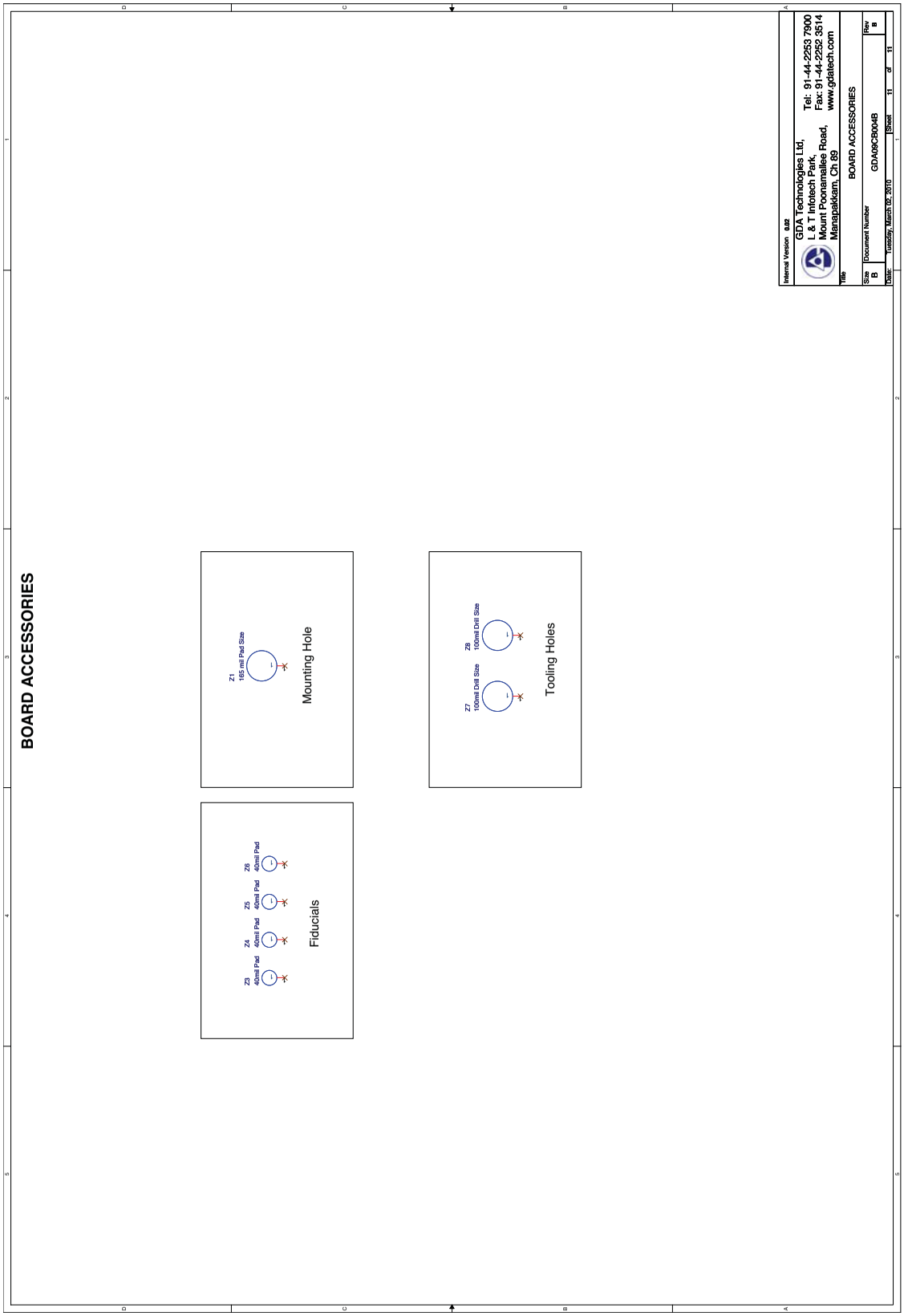


Figure 17. Board Accessories



Appendix B. Hardware Variants

Early versions of the HDMI Mezzanine Card Revision B were produced with U3 (STMicroelectronics STDVE001A Adaptive single 3.4 Gbps TMDS/HDMI signal equalizer) populated. On the current version of the HDMI Mezzanine Card Revision B, U3 is not populated.

To receive HDMI/DVI input when U3 is unpopulated:

- Connect the HDMI/DVI source using J2.
- Install a shunt between pin 2 and pin 3 of header H13 to route J2 HDMI/DVI signals to the FPGA via the Mezzanine connector.

On the current version of the board, the following additional changes were made:

- To support the Extended Display Identification Data (EDID) via the I^2C interface of the FPGA, two modification wires are installed in the following locations on the new HDMI Mezzanine Card Revision B:
  - R15 (pad nearest U3) to R12 (pad nearest U3)
  - R14 (pad nearest U3) to R11 (pad nearest U3)

  These wires bridge the I^2C bus around vacant U3.
- The resistors R2, R3, R6 and R7 are not populated (to reduce I^2C bus pull-up strength).
- The resistors R71 and R58 are not populated (to correct a pull-down contention).