EVQ1925-R-00A

100V, 4A, High-Frequency, Half-Bridge Gate Driver Evaluation Board

DESCRIPTION

The EVQ1925-RE-00A evaluation board is designed to demonstrate the capabilities of the MPQ1925, a high-frequency, half-bridge gate driver. The MPQ1925 has a 3A source current and a 4.5A sink current at 12V V_{DD}. The quiescent current (I_Q) is below 150µA.

The MPQ1925's integrated bootstrap (BST) diode reduces the external component count. The device's low-side MOSFET (LS-FET) and high-side MOSFET (HS-FET) driver channels are independently controlled, and are matched with less than 5ns in time delay. In the case of an insufficient supply, the device's HS-FET and LS-FET under-voltage lockout (UVLO) protection forces the outputs low.

The MPQ1925 is available in a small QFN-8 (4mmx4mm) package. It is designed for motor drivers and other power control applications, such as telecommunication half-bridge power supplies, avionics DC/DC converters, two-switch forward converters, and active-clamp forward converters.

The EVQ1925-R-00A is configured as a buck converter. INH and INL are independent signals that require complementary pulse-width modulations (PWMs) and a proper dead time (DT).

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Driver power supply voltage (V_{DD}) range		8V to 15V
Input power supply voltage (V_{POWER}) range		0V to 100V
Floating gate driver maximum source current (I_{OHH})	V_{DD} = 12V	2.6A
Floating gate driver maximum sink current (I_{OLH})	V_{DD} = 12V	4.5A
Low-side (LS) gate driver maximum source current (I_{OHL})	V_{DD} = 12V	3A
LS gate driver maximum sink current (I_{OLL})	V_{DD} = 12V	4.5A

EVQ1925-R-00A EVALUATION BOARD

LxWxH (6.35cmx6.35cmx2.5cm)

Board Number	MPS IC Number
EVQ1925-R-00A	MPQ1925HR

QUICK START GUIDE

1. Preset the driver power supply voltage (V_{DD}) between 8V and 15V.
2. Preset the input power supply voltage (V_{POWER}) range between 0V and 100V.
3. Connect two complementary pulse-width modulations (PWMs) with a proper dead time (DT) to CN4.
4. Connect the driver power supply terminals to:
   a. Positive (+): VDD
   b. Negative (-): GND
5. Connect the input power supply terminals to:
   a. Positive (+): V_{POWER}
   b. Negative (-): GND
6. Connect the load terminals to:
   a. Positive (+): V_{LOAD}
   b. Negative (-): GND
7. After making the connections, turn on the driver power supply.
8. Check the INH, INL, DRVH, and DRVL signals. Ensure that a sufficient DT for DRVH and DRVL has been established.
9. Turn on the input power supply.
10. Turn on the load, then check the output voltage (V_{OUT}) and current.
11. To shut down the system, turn off the load, V_{POWER}, and V_{DD}.

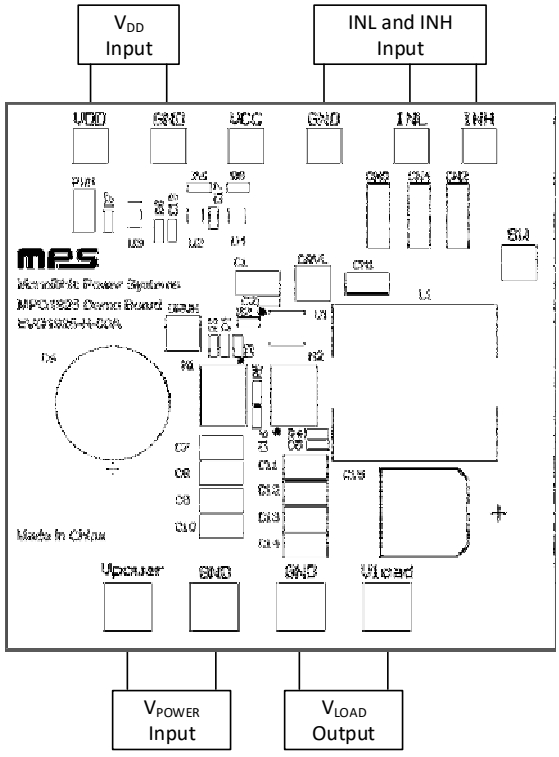


Figure 1: Test Set-Up for the EVQ1925-R-00A

EVALUATION BOARD SCHEMATIC

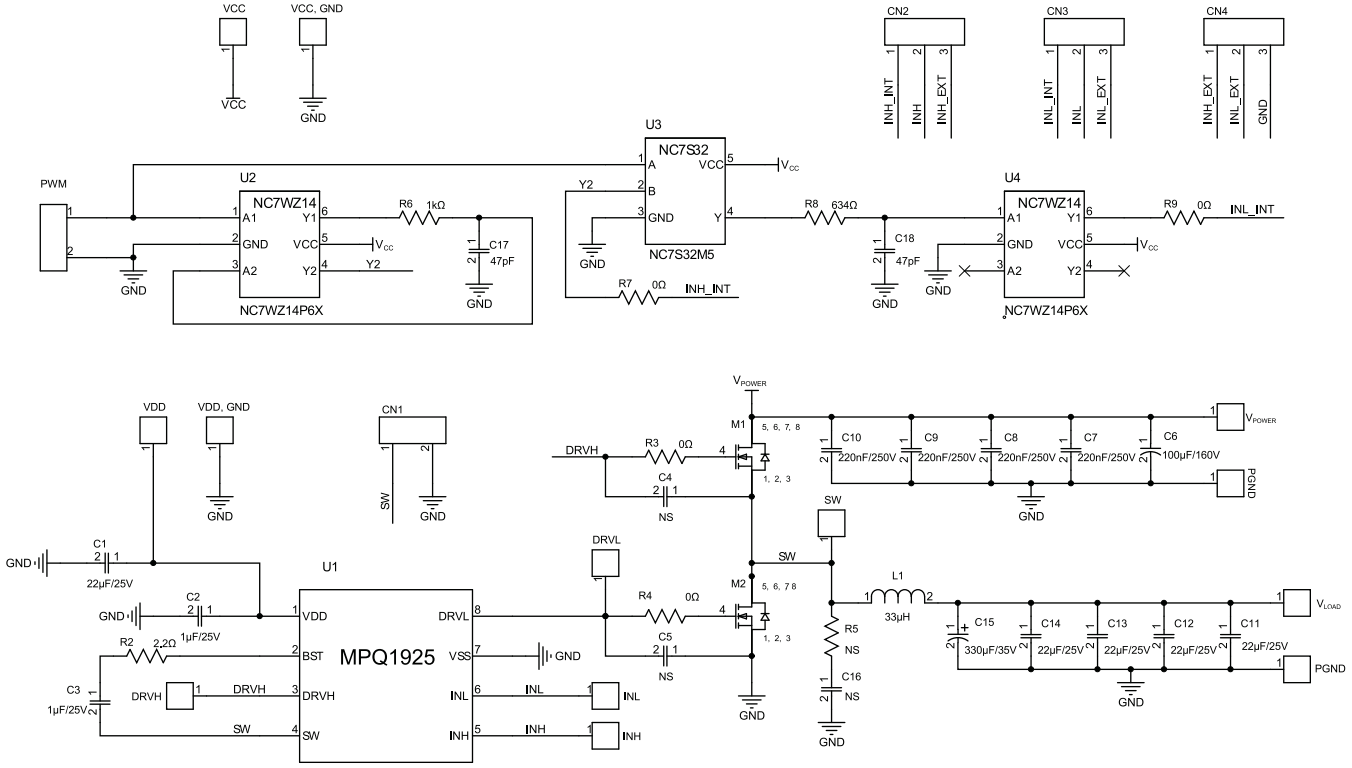


Figure 2: Evaluation Board Schematic

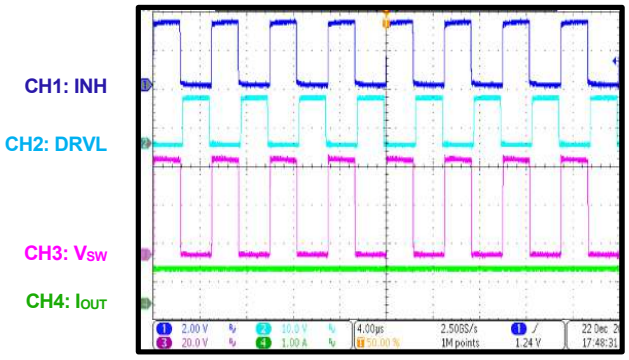
EVQ1925-R-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 50V, X7R	1210	Murata	GRM32ER71H106KA12L
2	C2, C3	1µF	Ceramic capacitor, 25V, X7R	0603	TDK	GCM188R71E105KA64D
3	C4, C5, C16	NS				
1	C6	100µF	Electrolytic capacitor, 160V	DIP	Jianghai	CD110-160V100
4	C7, C8, C9, C10	220nF	Ceramic capacitor, 250V, X7R	1210	Murata	GRM32DR72E224KW01L
1	C15	330µF	Electrolytic capacitor, 35V	SMD	Jianghai	VZ2-35V330
1	L1	33µH	Inductor, 8.5A	SMD	Wurth	74435573300
1	R5	NS				
3	R2, R3, R4	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
2	M1, M2	100V	N-channel MOSFET, 9A	SO-8	Analog Power	AM4492N
4	V_{POWER}, V_{LOAD}, GND, GND	2mm	Needle	Custom	Custom	
9	VDD, GND, VCC, GND, INL, INH, DRVH, DRVL, SW	1mm	Needle	Custom	Custom	
1	U1	MPQ1925	Integrated gate driver	QFN-8 (4mmx 4mm)	MPS	MPQ1925HR

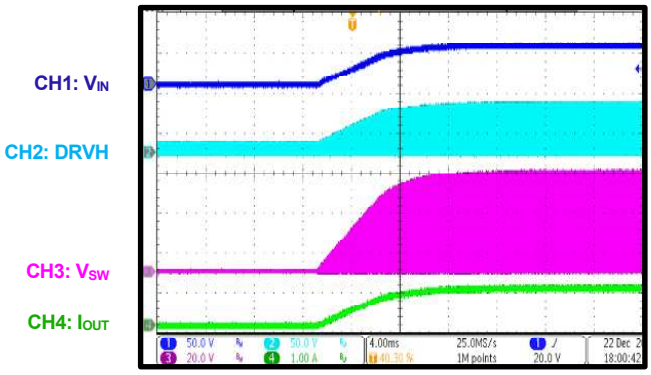
EVB TEST RESULTS

V_{DD} = 12V, V_{POWER} = 48V, INH/INL = 200kHz, dead time = 200ns, I_{LOAD} = 1A, T_A = 25°C, unless otherwise noted.

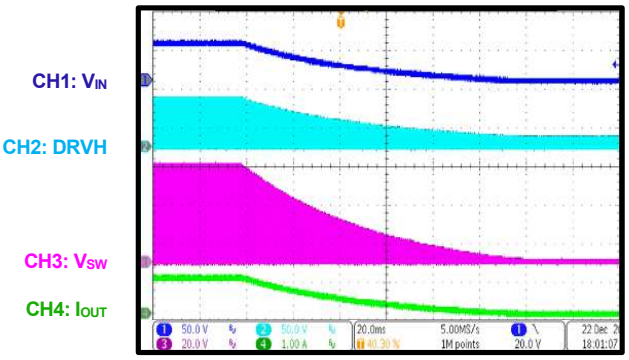
Normal Operation



Start-Up through VIN



Shutdown through VIN



PCB LAYOUT

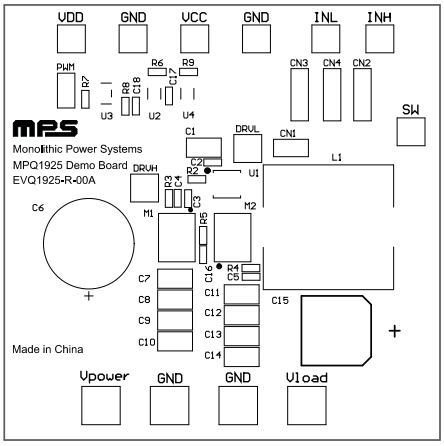


Figure 3: Top Silk

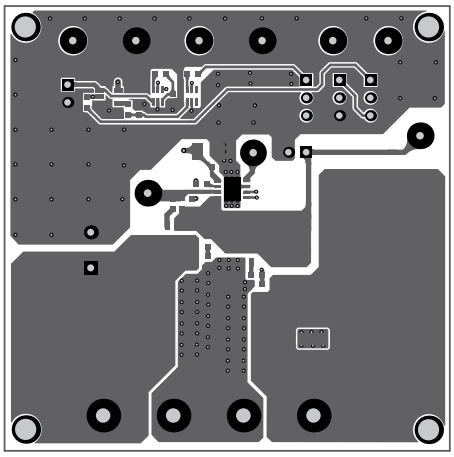


Figure 4: Top Layer

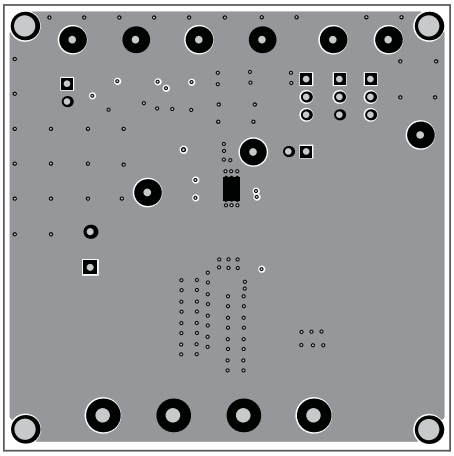


Figure 5: Mid-Layer 1

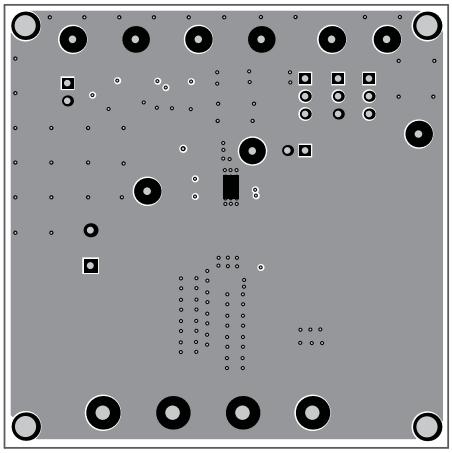


Figure 6: Mid-Layer 2

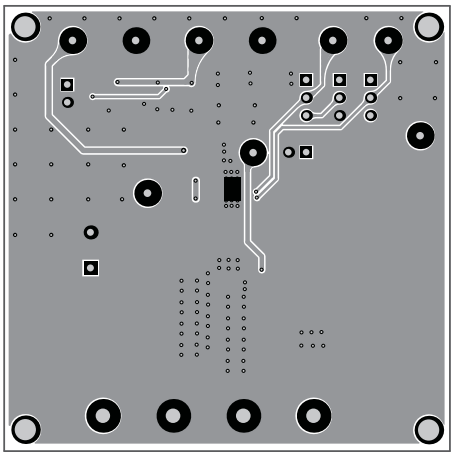


Figure 7: Bottom Layer

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/25/2022	Initial Release	-