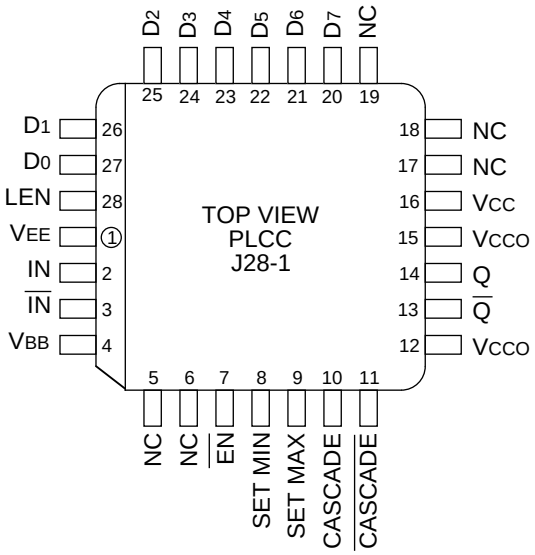
- **Up to 2ns delay range**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **≈20ps/digital step resolution**
- **>1GHz bandwidth**
- **On-chip cascade circuitry**
- **75KkΩ input pulldown resistor**
- **Fully compatible with Motorola MC10E/100E195**
- **Available in 28-pin PLCC package**



The SY10/100E195 are programmable delay chips (PDCs) designed primarily for clock de-skewing and timing adjustment. They provide variable delay of a differential ECL input transition.

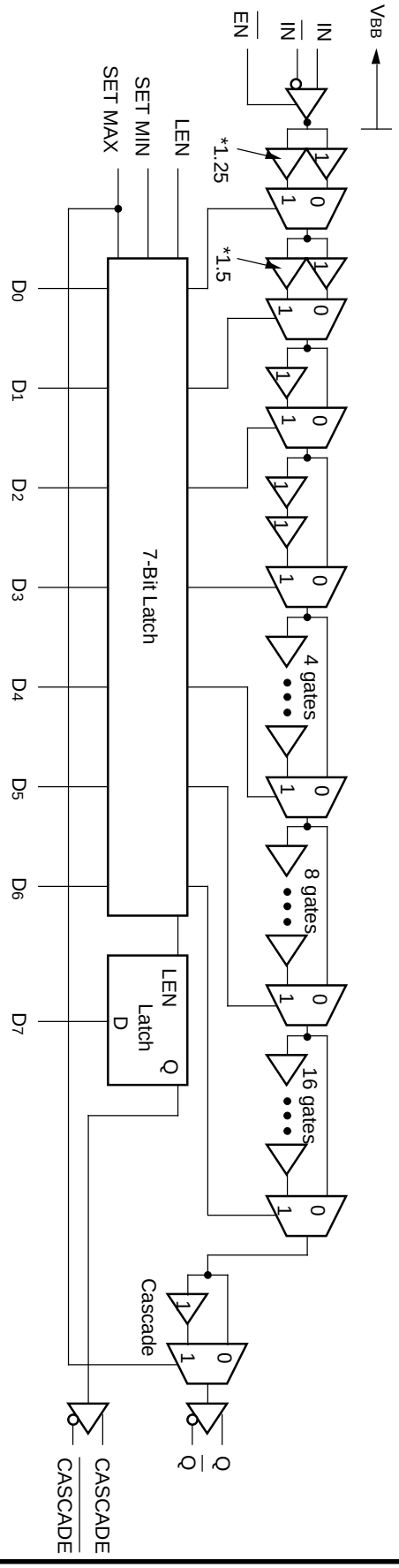
The delay section consists of a chain of gates organized as shown in the logic diagram. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80ps. These two elements provide the E195 with a digitally-selectable resolution of approximately 20ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on-chip by a high signal on the latch enable (LEN) control. If the LEN signal is either LOW or left floating, then the latch is transparent.

Because the delay programmability of the E195 is achieved by purely differential ECL gate delays, the device will operate at frequencies of >1GHz, while maintaining over 600mV of output swing.

The E195 thus offers very fine resolution, at very high frequencies, selectable entirely from a digital input, allowing for very accurate system clock timing.

An eighth latched input, D_7, is provided for cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Minimum Delay Set
SET MAX	Maximum Delay Set
CASCADE	Cascade Signal



***Delays are 25% or 50% longer than standard (standard = 80ps).**

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	130	156	—	130	156	—	130	156		
	100E	—	130	156	—	130	156	—	150	179		

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output IN to Q; Tap = 0 IN to Q; Tap = 127 $\overline{EN}$ to Q; Tap = 0 D_7 to CASCADE	 1210 3320 1250 300	 1360 3570 1450 450	 1510 3820 1650 700	 1240 3380 1275 300	 1390 3630 1475 450	 1540 3880 1675 700	 1440 3920 1350 300	 1590 4270 1650 450	 1765 4720 1950 700	ps	—
t_{RANGE}	Programmable Range t_{PD} (max.) – t_{PD} (min.)	2000	2175	—	2050	2240	—	2375	2580	—	ps	—
Δt	Step Delay D_0 High D_1 High D_2 High D_3 High D_4 High D_5 High D_6 High	 — — 55 115 250 505 1000	 17 34 68 136 272 544 1088	 — — 105 180 325 620 1190	 — — 55 115 250 515 1030	 17.5 35 70 140 280 560 1120	 — — 105 180 325 620 1220	 — — 65 140 305 620 1240	 21 42 84 168 336 672 1344	 — — 120 205 380 740 1450	ps	6
Lin	Linearity	D_1	D_0	—	D_1	D_0	—	D_1	D_0	—	—	7
t_{skew}	Duty Cycle Skew, t_{PHL}–t_{PLH}	—	±30	—	—	±30	—	—	±30	—	ps	1
t_S	Set-up Time D to LEN D to IN EN to IN	 200 800 200	 0 — —	 — — —	 200 800 200	 0 — —	 — — —	 200 800 200	 0 — —	 — — —	ps	 2 3
t_H	Hold Time LEN to D IN to $\overline{EN}$	 500 0	 250 —	 — —	 500 0	 250 —	 — —	 500 0	 250 —	 — —	ps	 4
t_R	Release Time $\overline{EN}$ to IN SET MAX to LEN SET MIN to LEN	 300 800 800	 — — —	 — — —	 300 800 800	 — — —	 — — —	 300 800 800	 — — —	 — — —	ps	 5
t_{jit}	Jitter	—	<5	—	—	<5	—	—	<5	—	ps	8
t_r t_f	Rise/Fall Times 20–80% (Q) 20–80% (CASCADE)	 125 300	 225 450	 325 650	 125 300	 225 450	 325 650	 125 300	 225 450	 325 650	ps	—

NOTES:

2. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
3. This set-up time defines the amount of time prior to the input signal the delay tap of the device must be set.
4. This set-up time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75mV to that IN/IN transition.
5. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75mV to that IN/$\overline{IN}$ transition.
6. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
7. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D_0 resolution steps across the specified programmable range.
8. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs D_n). Typically, the device will be monotonic to the D_0 input, however, under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D_0 input is the LSB. With the D_1 input as the LSB, the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
9. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

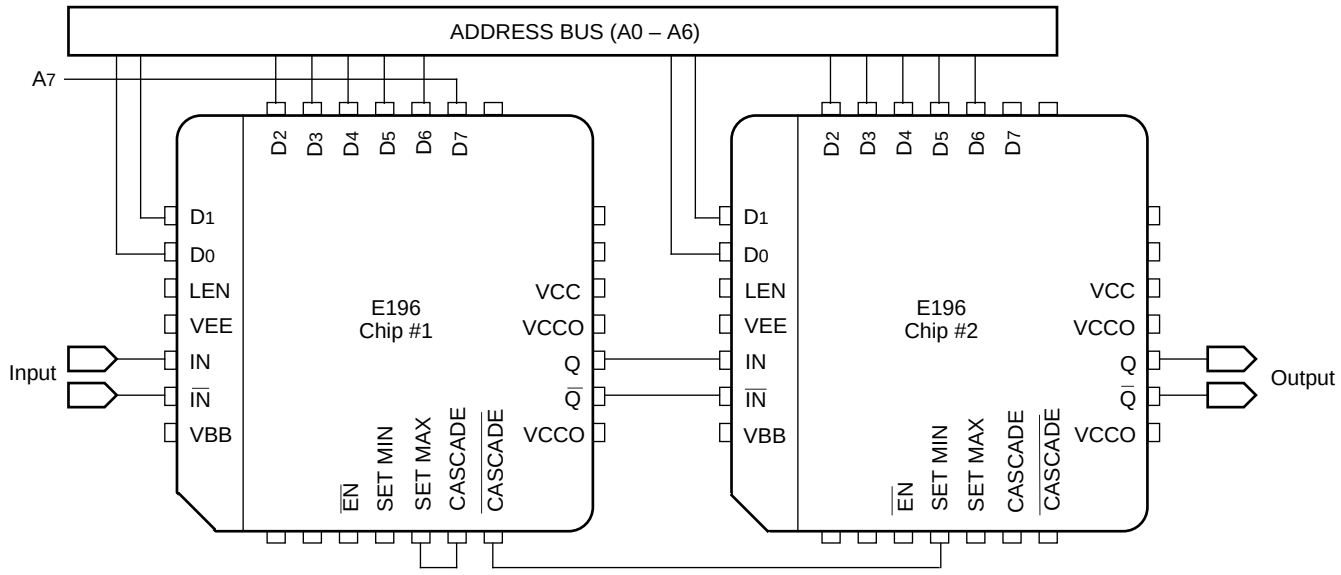


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E195s

To increase the programmable range of the E195, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195s without the need for any external gating. Furthermore, this capability requires only one more address line per added E195. Obviously, cascading multiple PDCs will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195s. As can be seen, this scheme can easily be expanded for larger E195 chains. The D_7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1, when D_7 is asserted, it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D_7 of chip #1 above is low, the cascade output will also be low, while the cascade bar output will be a logical high. In this condition, the SET MIN pin of chip #2 will be asserted and, thus, all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding, any changes on the A_0–A_6 address bus will not affect the operation of chip #2.

Chip #1, on the other hand, will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A_0–A_6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A_0–A_6 address bus), D_7 will be asserted to signal the need to cascade the delay to the next E195 device. When D_7 is asserted, the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A_0–A_6 address bus. Chip #1, on the other hand, will have its SET MAX pin asserted, resulting in the device delay to be independent of the A_0–A_6 address bus.

When the SET MAX pin of chip #1 is asserted, the D_0 and D_1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity, an additional gate delay is selected in the cascade circuitry. As a result, when D_7 of chip #1 is asserted, the delay increases from 31.75 gates to 32 gates. A 32-gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices, one simply needs to connect the D_7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

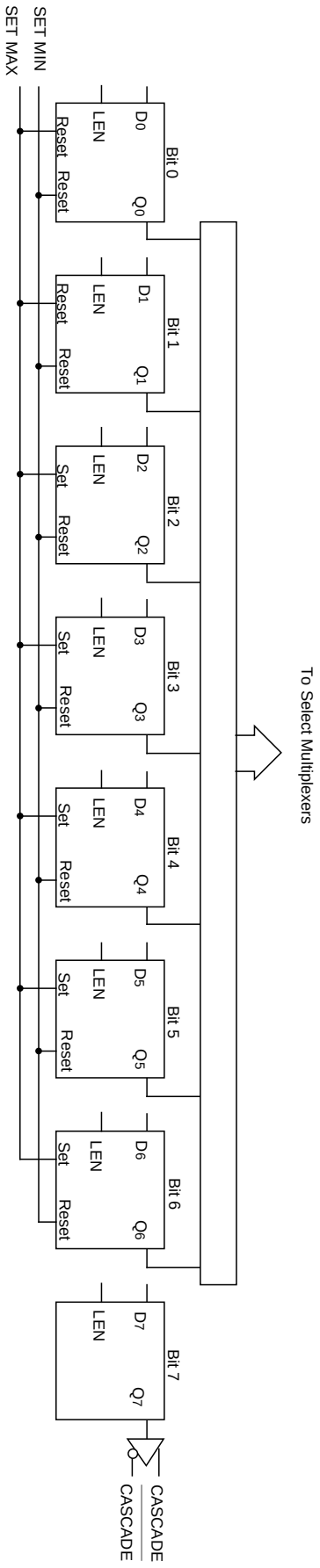
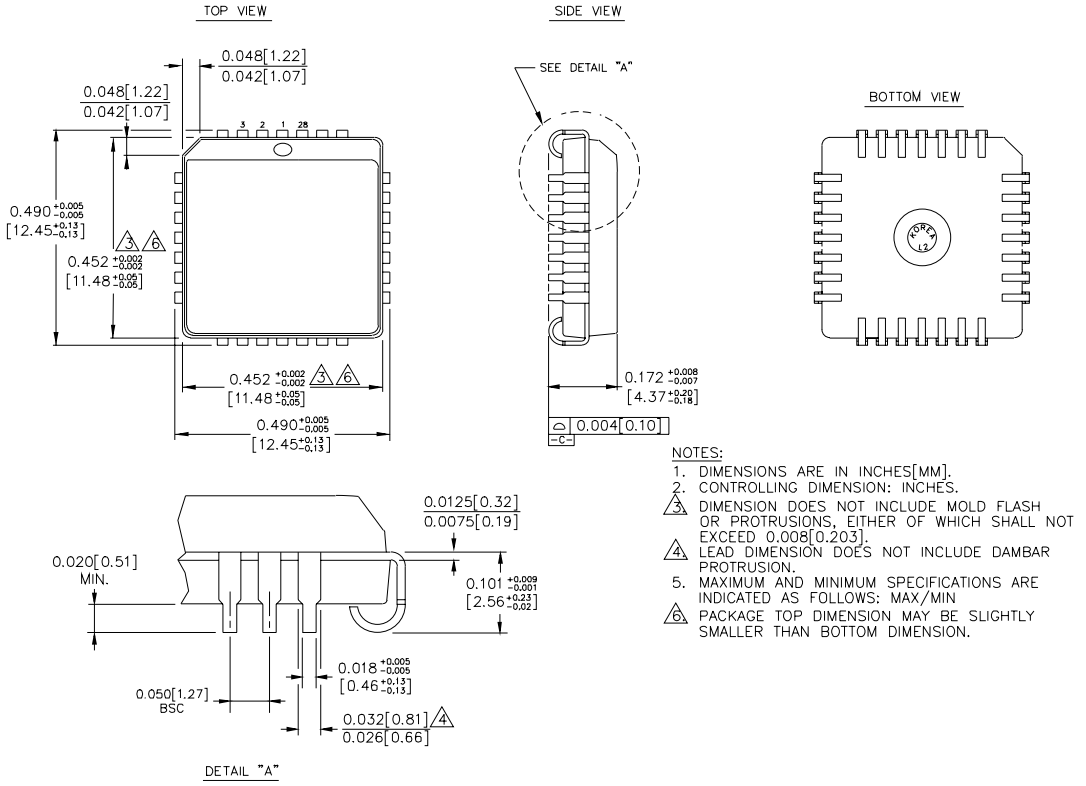


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

Ordering Code	Package Type	Operating Range
SY10E195JC	J28-1	Commercial
SY10E195JCTR	J28-1	Commercial
SY100E195JC	J28-1	Commercial
SY100E195JCTR	J28-1	Commercial



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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