ESD10201

Low Capacitance ESD Protection Diodes

Micro−package Diodes for ESD Protection

The ESD10201 is designed to protect voltage sensitive components that require ultra−low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for RF applications.

Features

- Low Capacitance 0.3 pF (Typical)
- Low Clamping Voltage
- Small Body Outline Dimensions: (0.62 x 0.32 mm) − 0201
- Low Body Height: 0.3 mm
- Working Voltage: ±21 V
- IEC61000−4−2 Level 4 ESD Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- Wireless Charger
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) (Note 1) Air		15	kV
IEC 61000−4−2 (ESD) (Note 1) Contact		12	kV
IEC 61000−4−5 (ESD) (Note 2)		1	A
Total Power Dissipation (Note 3) @ T_A = 25°C Thermal Resistance, Junction−to−Ambient	P_D $R_{\theta JA}$	250 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−2 waveform.
2. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.
3. Mounted with recommended minimum pad size, DC board FR−4

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MARKING DIAGRAM

X3DFN2
CASE 152AF

PIN 1

Y M

Y = Specific Device Code
M = Date Code

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
ESD10201MUT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel

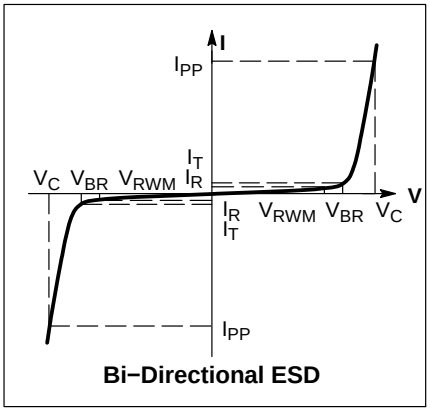
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional ESD

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, For min/max values T_A = 0°C to 60°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Working Voltage	V_{RWM}				21	V
Breakdown Voltage (Note 4)	V_{BR}	I_T = 1 mA	21.2			V
Reverse Current	I_R	V_{RVM} = 21 V			200	nA
Clamping Voltage (Note 5)	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 1 and 2			
Clamping Voltage TLP (Note 6)	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		37.7 40.4 −38.4 −41.1		V
Clamping Voltage (Note 6)	Vc	I_{PP} = 1 A @ 8/20 μs		35		V
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		0.3		pF
Dynamic Resistance	R_{DYN}	TLP Pulse		0.44		Ω
Insertion Loss		f = 1 MHz f = 8.5 GHz		−0.045 −0.335		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
5. For test procedure see Figures 3 and 4 and application note AND8307/D.
6. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

TYPICAL CHARACTERISTICS

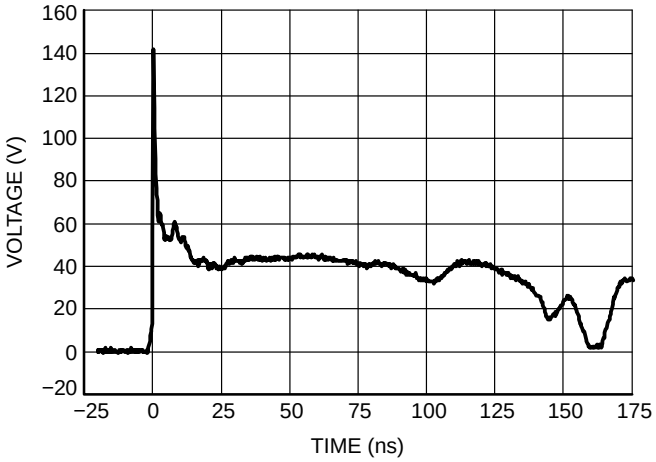


Figure 1. Typical IEC61000−4−2 + 8 kV Contact ESD Clamping Voltage

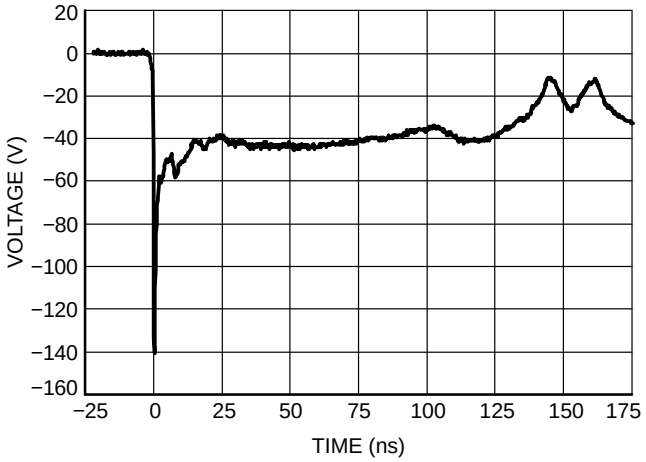


Figure 2. Typical IEC61000−4−2 − 8 kV Contact ESD Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

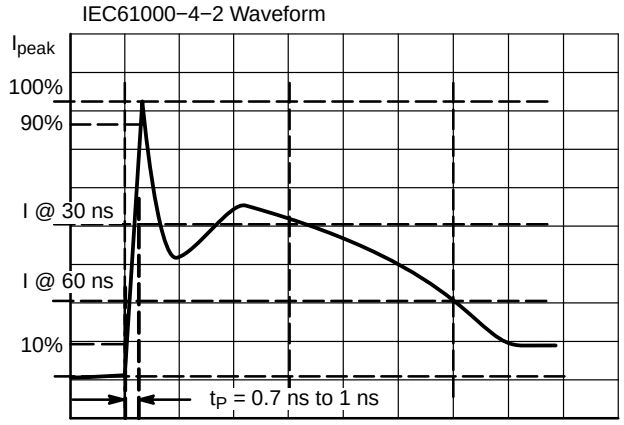


Figure 3. IEC61000−4−2 Spec

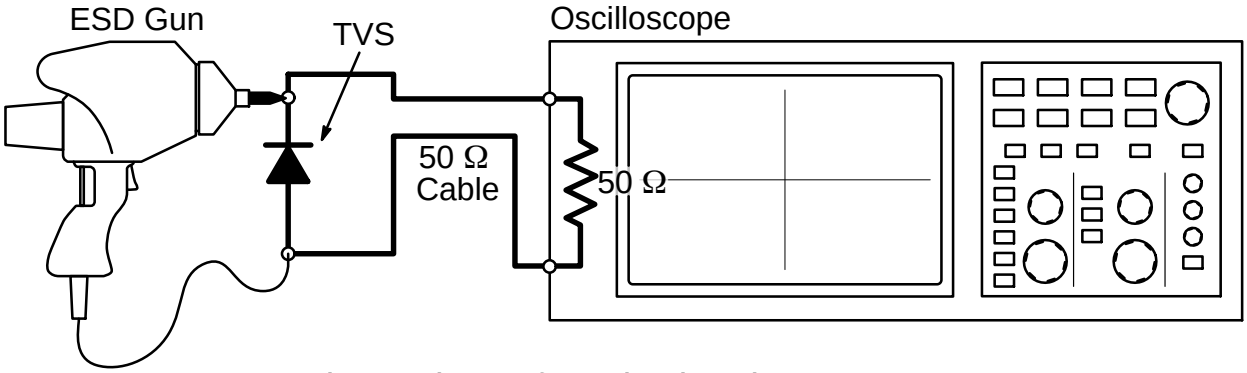


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

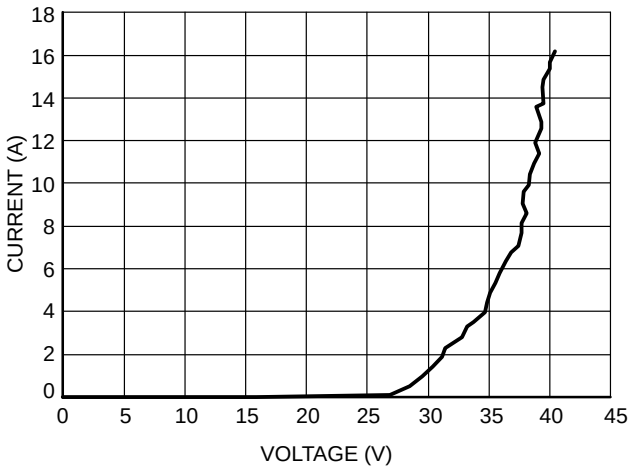


Figure 5. Typical Positive TLP IV Curve

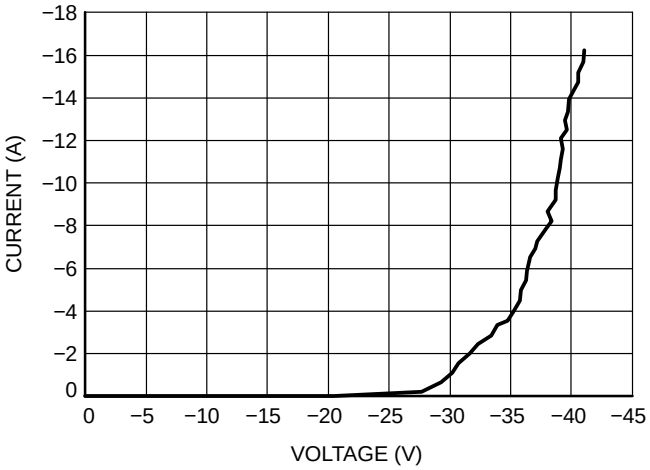


Figure 6. Typical Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

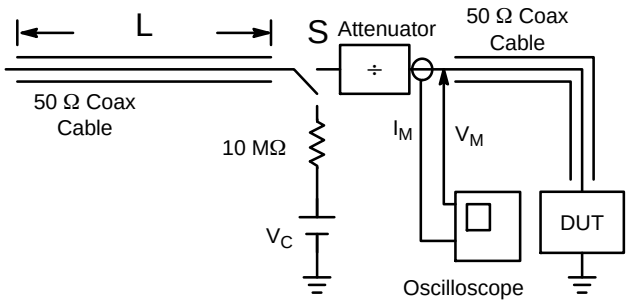


Figure 7. Simplified Schematic of a Typical TLP System

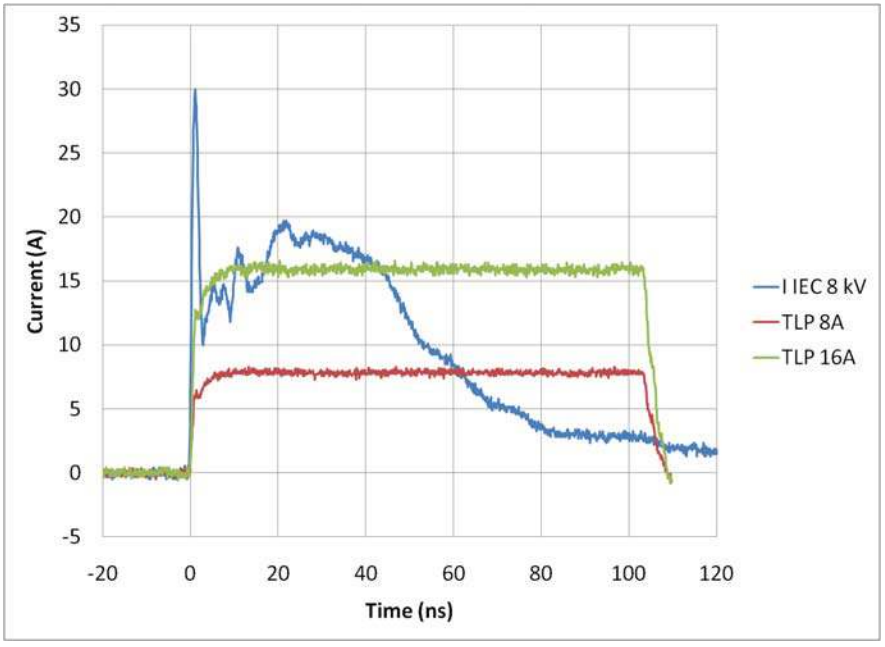


Figure 8. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

TYPICAL CHARACTERISTICS

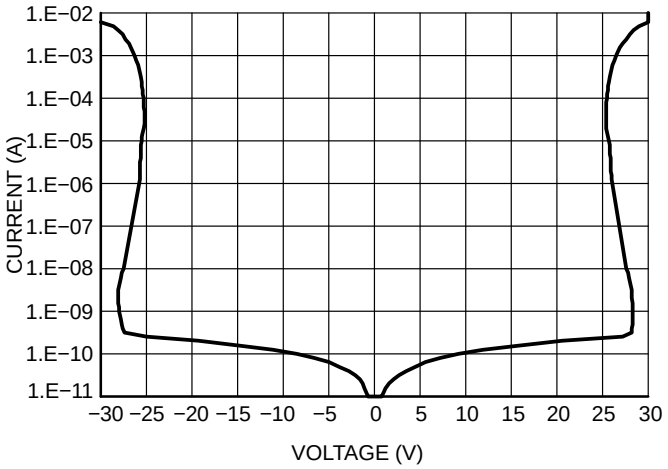


Figure 9. Typical IV Characteristics

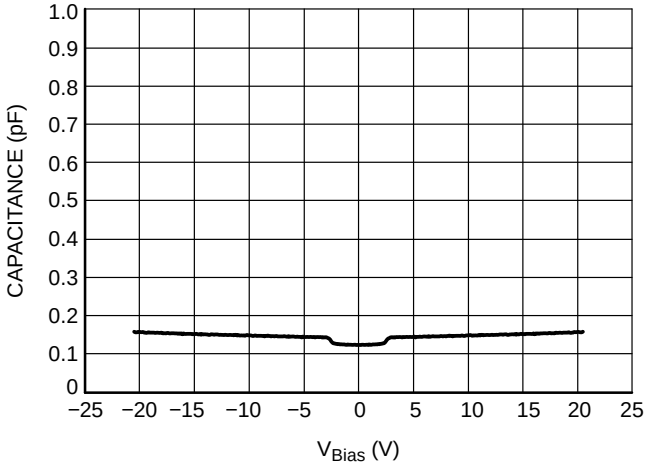


Figure 10. Typical CV Characteristics

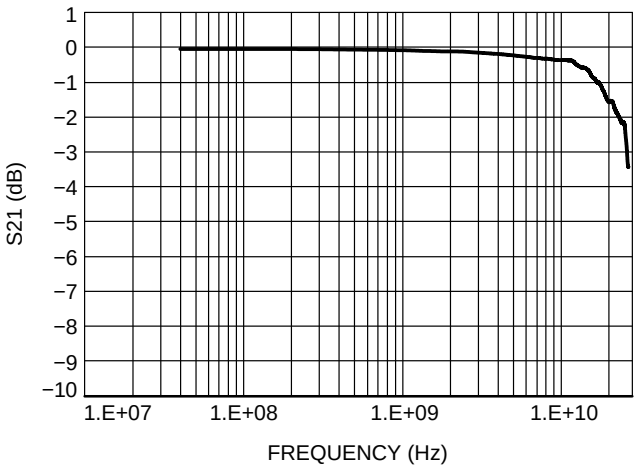


Figure 11. Typical Insertion Loss

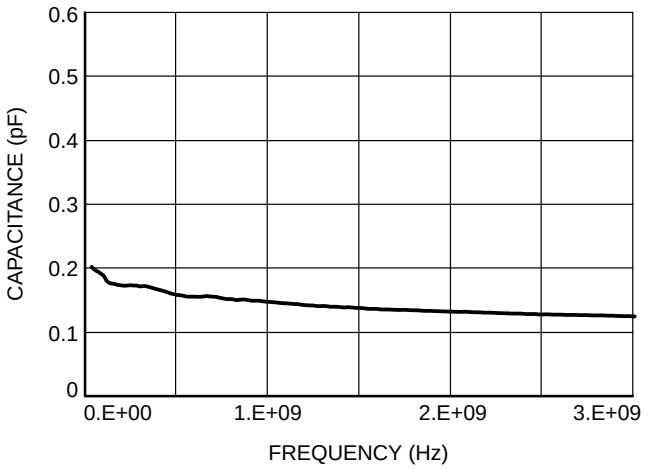
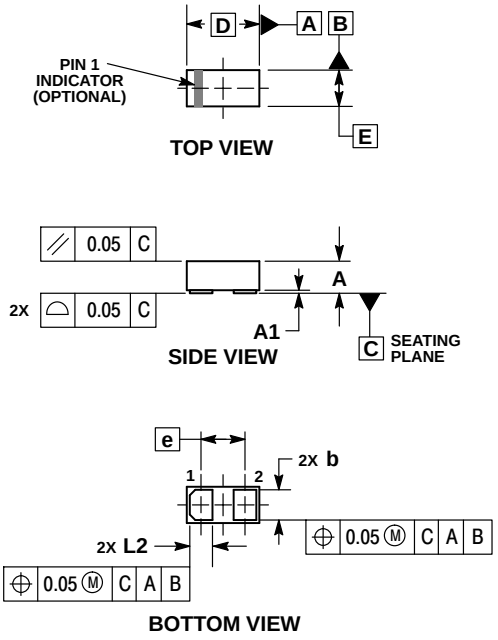


Figure 12. Typical Capacitance over Frequency

ESD10201

PACKAGE DIMENSIONS

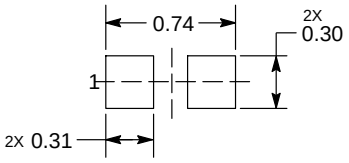
X3DFN2, 0.62x0.32, 0.355P, (0201)
CASE 152AF
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.25	0.33
A1	−−−	0.05
b	0.22	0.28
D	0.58	0.66
E	0.28	0.36
e	0.355 BSC	
L2	0.17	0.23

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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