



March 2015



FDD8874 / FDU8874

FDD8874 / FDU8874

N-Channel PowerTrench[®] MOSFET 30V, 116A, 5.1mΩ

General Description

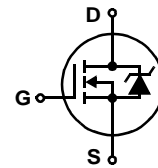
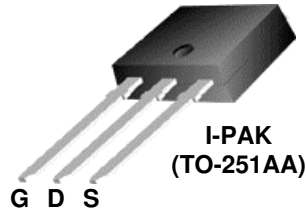
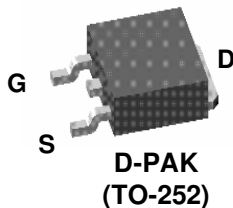
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

Features

- $r_{DS(ON)} = 5.1m\Omega$, $V_{GS} = 10V$, $I_D = 35A$
- $r_{DS(ON)} = 6.4m\Omega$, $V_{GS} = 4.5V$, $I_D = 35A$
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant

Applications

- DC/DC converters



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$) (Note 1)	116	A
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 4.5V$) (Note 1)	103	A
	Continuous ($T_{amb} = 25^\circ C$, $V_{GS} = 10V$, with $R_{\theta JA} = 52^\circ C/W$)	18	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	240	mJ
P_D	Power dissipation	110	W
	Derate above $25^\circ C$	0.73	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252, TO-251	1.36	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, TO-251	100	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8874	FDD8874	TO-252AA	13"	16mm	2500 units
FDU8874	FDU8874	TO-251AA	Tube	N/A (Tube)	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 35\text{A}, V_{GS} = 10\text{V}$	-	0.0042	0.0051	Ω
		$I_D = 35\text{A}, V_{GS} = 4.5\text{V}$	-	0.0052	0.0064	
		$I_D = 35\text{A}, V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$	-	0.0069	0.0083	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	2990	-	pF
C_{OSS}	Output Capacitance		-	585	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	340	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}, f = 1\text{MHz}$	-	2.0	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	-	54	72	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V to } 5\text{V}$	-	29	38	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 1\text{V}$	-	3.0	4.0	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$	-	8.0	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	5.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	10	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 35\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 4.7\Omega$	-	-	156	ns
$t_{d(ON)}$	Turn-On Delay Time		-	9	-	ns
t_r	Rise Time		-	96	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	47	-	ns
t_f	Fall Time		-	37	-	ns
t_{OFF}	Turn-Off Time		-	-	126	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 35\text{A}$	-	-	1.25	V
		$I_{SD} = 15\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	32	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	18	nC

Notes:

- Package current limitation is 35A.
- Starting $T_J = 25^\circ\text{C}, L = 0.61\text{mH}, I_{AS} = 28\text{A}, V_{DD} = 27\text{V}, V_{GS} = 10\text{V}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

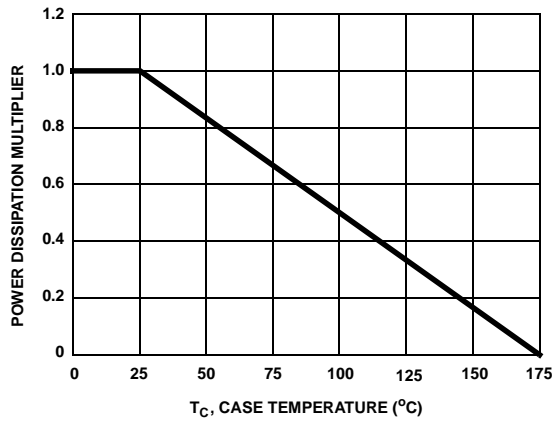


Figure 1. Normalized Power Dissipation vs Case Temperature

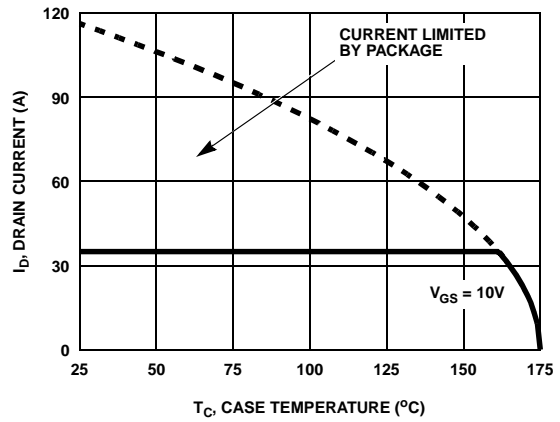


Figure 2. Maximum Continuous Drain Current vs Case Temperature

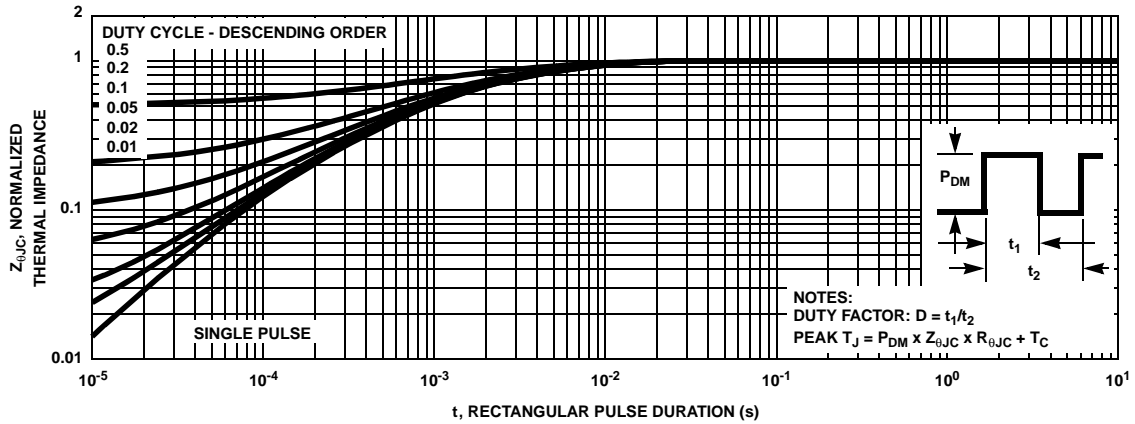


Figure 3. Normalized Maximum Transient Thermal Impedance

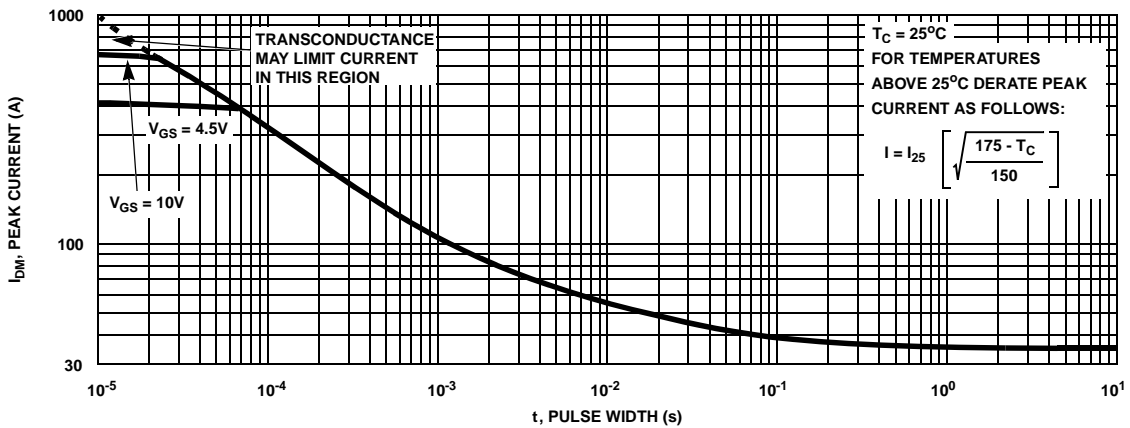


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

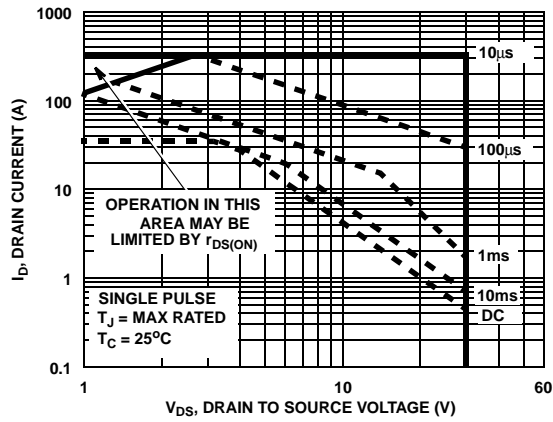
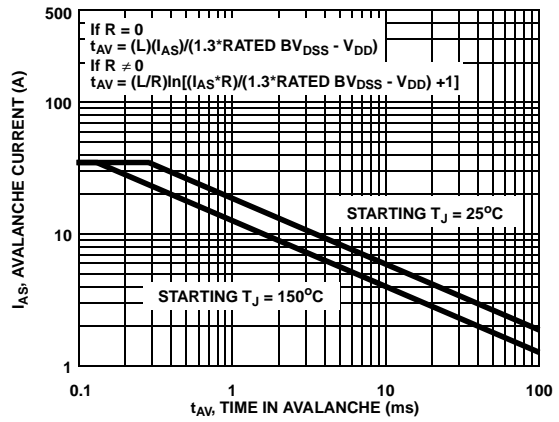


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 6. Unclamped Inductive Switching Capability

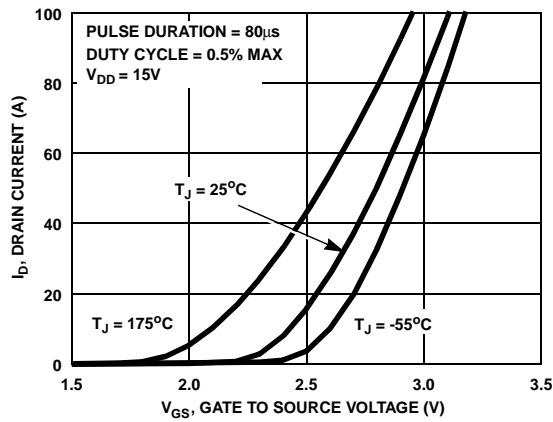


Figure 7. Transfer Characteristics

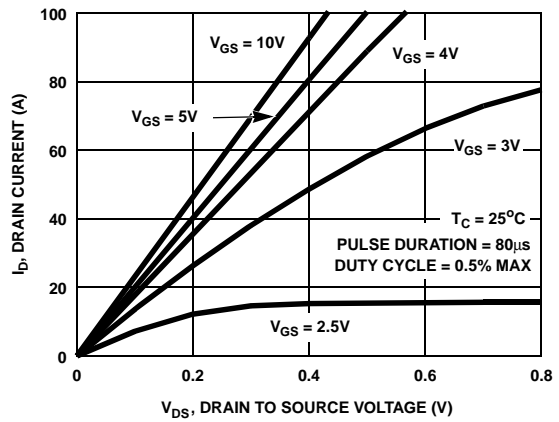


Figure 8. Saturation Characteristics

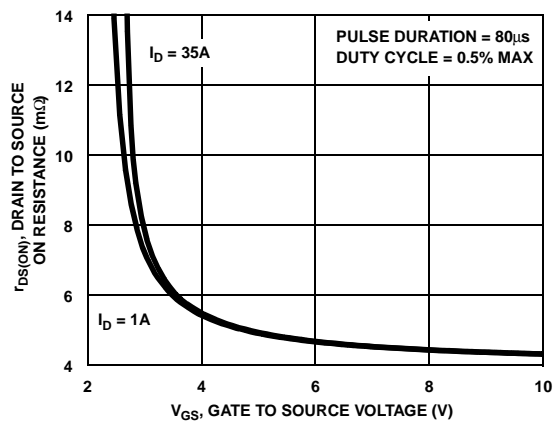


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

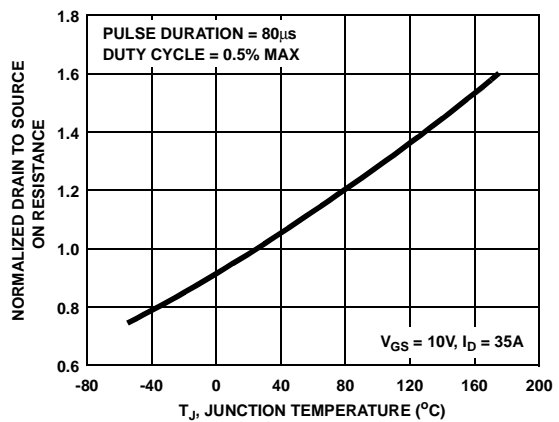


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

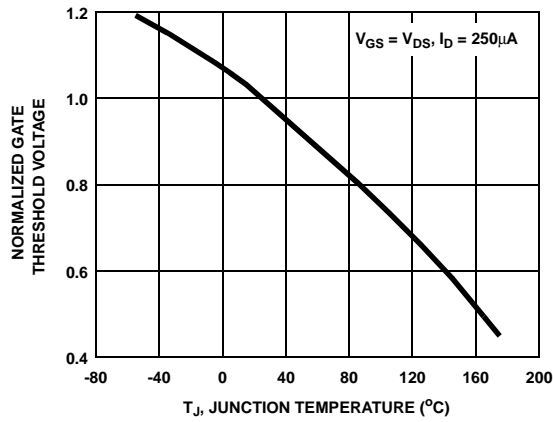


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

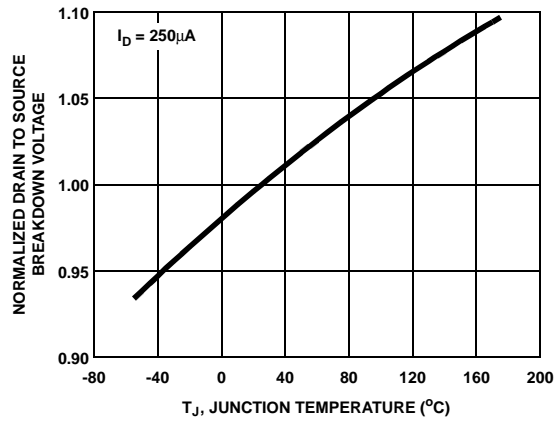


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

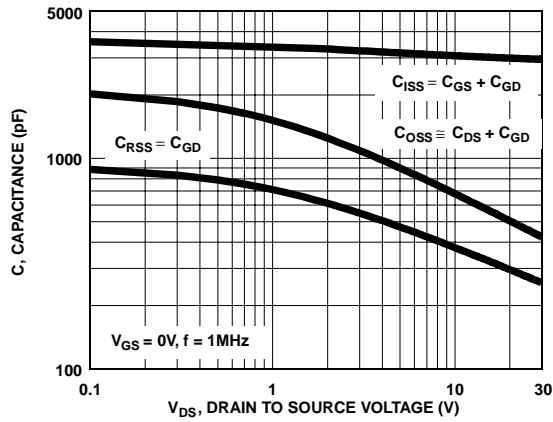


Figure 13. Capacitance vs Drain to Source Voltage

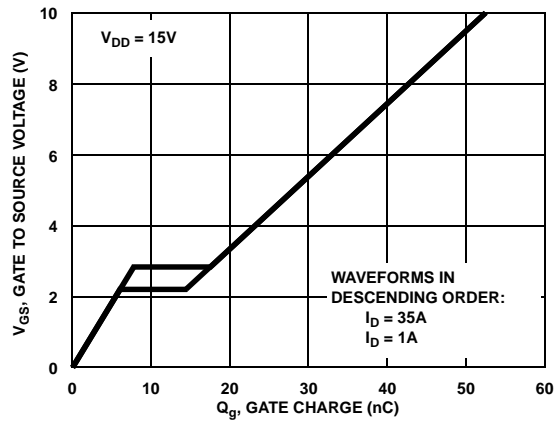


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

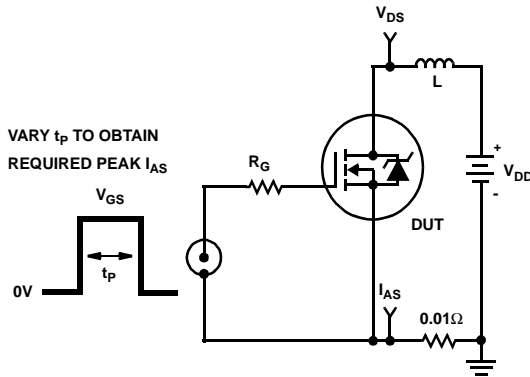


Figure 15. Unclamped Energy Test Circuit

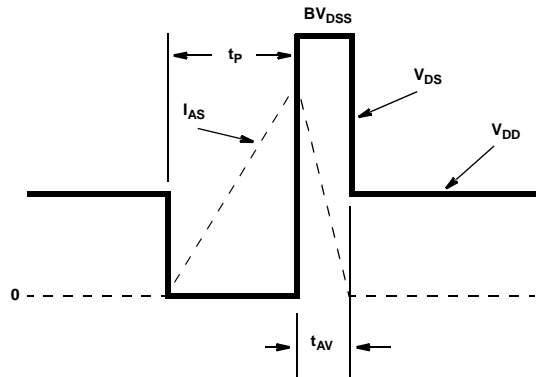


Figure 16. Unclamped Energy Waveforms

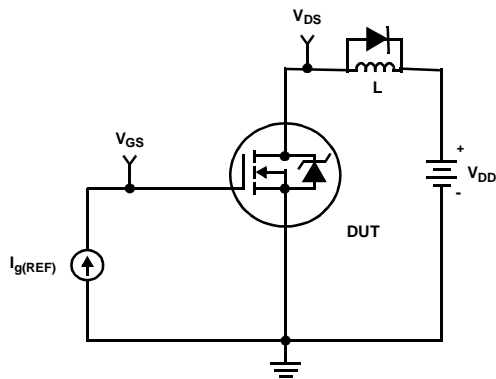


Figure 17. Gate Charge Test Circuit

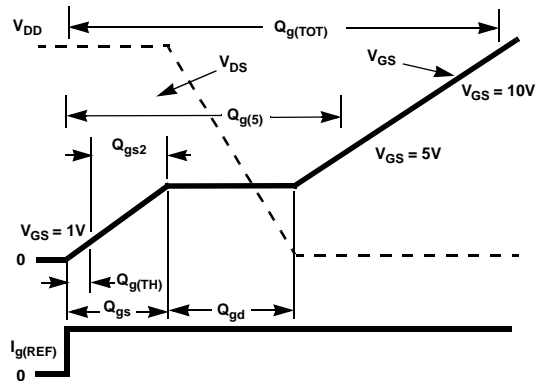


Figure 18. Gate Charge Waveforms

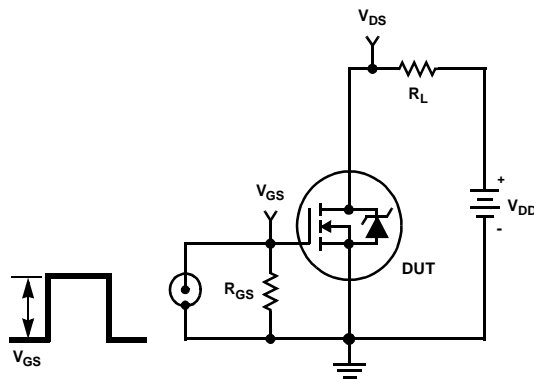


Figure 19. Switching Time Test Circuit

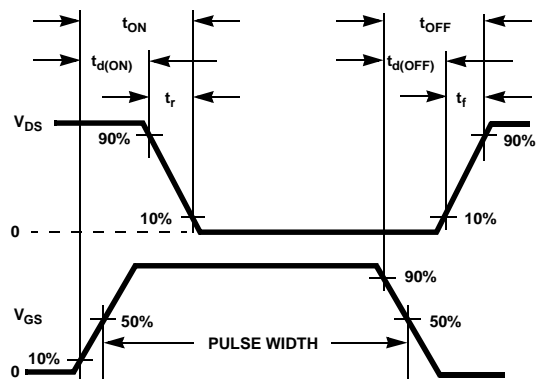


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}C$), and thermal resistance $R_{\theta JA}$ ($^{\circ}C/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (EQ. 1)$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \quad (EQ. 2)$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \quad (EQ. 3)$$

Area in Centimeters Squared

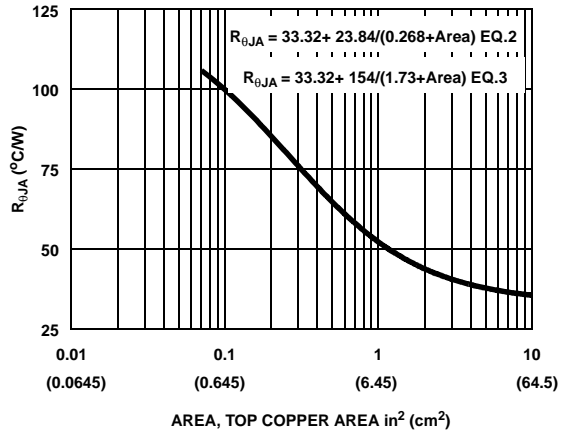


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDD8874 2 1 3 ; rev May 2004

Ca 12 8 2.1e-9

Cb 15 14 2.1e-9

Cin 6 8 2.7e-9

Dbody 7 5 DbodyMOD
 Dbreak 5 11 DbreakMOD
 Dplcap 10 5 DplcapMOD

Ebrcak 11 7 17 18 33.5
 Eds 14 8 5 8 1
 Egs 13 8 6 8 1
 Esg 6 10 6 8 1
 Evthres 6 21 19 8 1
 Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 6.5e-9
 Ldrain 2 5 1.0e-9
 Lsource 3 7 1.8e-9

RLgate 1 9 65
 RLdrain 2 5 10
 RLsource 3 7 18

Mmed 16 6 8 8 MmedMOD
 Mstro 16 6 8 8 MstroMOD
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
 Rdrain 50 16 RdrainMOD 2e-3
 Rgate 9 20 2.0
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 Rsource 8 7 RsourceMOD 2e-3
 Rvthres 22 8 RvthresMOD 1
 Rvtemp 18 19 RvtempMOD 1
 S1a 6 12 13 8 S1AMOD
 S1b 13 12 13 8 S1BMOD
 S2a 6 15 14 13 S2AMOD
 S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))/(1e-6*500),10)}}

.MODEL DbodyMOD D (IS=7E-12 IKF=10 N=1.01 RS=2.5e-3 TRS1=8e-4 TRS2=2e-7
 + CJO=1.2e-9 M=0.57 TT=1e-15 XTl=1.2)

.MODEL DbreakMOD D (RS=8e-2 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=9.2e-10 IS=1e-30 N=10 M=0.37)

.MODEL MmedMOD NMOS (VTO=1.8 KP=9 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.0)

.MODEL MstroMOD NMOS (VTO=2.2 KP=380 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=-1.49 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=20 RS=0.1)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-8e-7)

.MODEL RdrainMOD RES (TC1=6.7e-3 TC2=7e-6)

.MODEL RSLCMOD RES (TC1=1e-4 TC2=1e-6)

.MODEL RsourceMOD RES (TC1=1e-4 TC2=1e-6)

.MODEL RvthresMOD RES (TC1=-2.1e-3 TC2=-8e-6)

.MODEL RvtempMOD RES (TC1=-1.8e-3 TC2=2e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3)

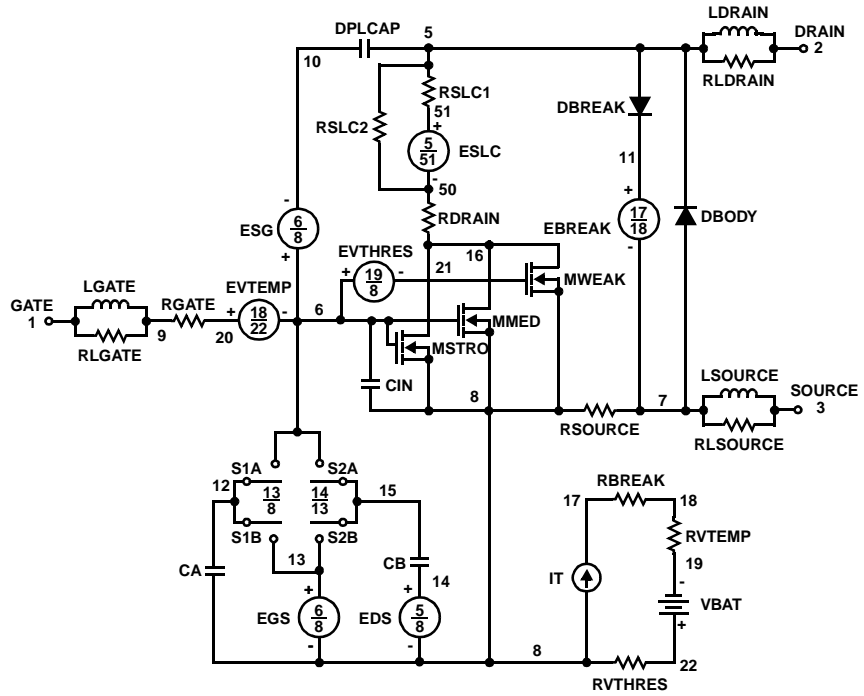
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-2)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

rev May 2004
 template FDD8874 n2,n1,n3
 electrical n2,n1,n3

```

{
var i iscl
dp..model dbodymod = (isl=7e-12,ikf=10,nl=1.01,rs=2.5e-3,trs1=8e-4,trs2=2e-7,cjo=1.2e-9,m=0.57,tt=1e-15,xti=1.2)
dp..model dbreakmod = (rs=8e-2,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=9.2e-10,isl=10e-30,nl=10,m=0.37)
m..model mmedmod = (type=_n,vto=1.8,kp=9,is=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=2.2,kp=380,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=1.49,kp=0.05,is=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2)
c.ca n12 n8 = 2.1e-9
c.cb n15 n14 = 2.1e-9
c.cin n6 n8 = 2.7e-9
  
```

```

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
  
```

```

spe.ebreak n11 n7 n17 n18 = 33.5
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
  
```

```
i.it n8 n17 = 1
```

```

l.lgate n1 n9 = 6.5e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 1.8e-9
  
```

```

res.rlgate n1 n9 = 65
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 18
  
```

```

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
  
```

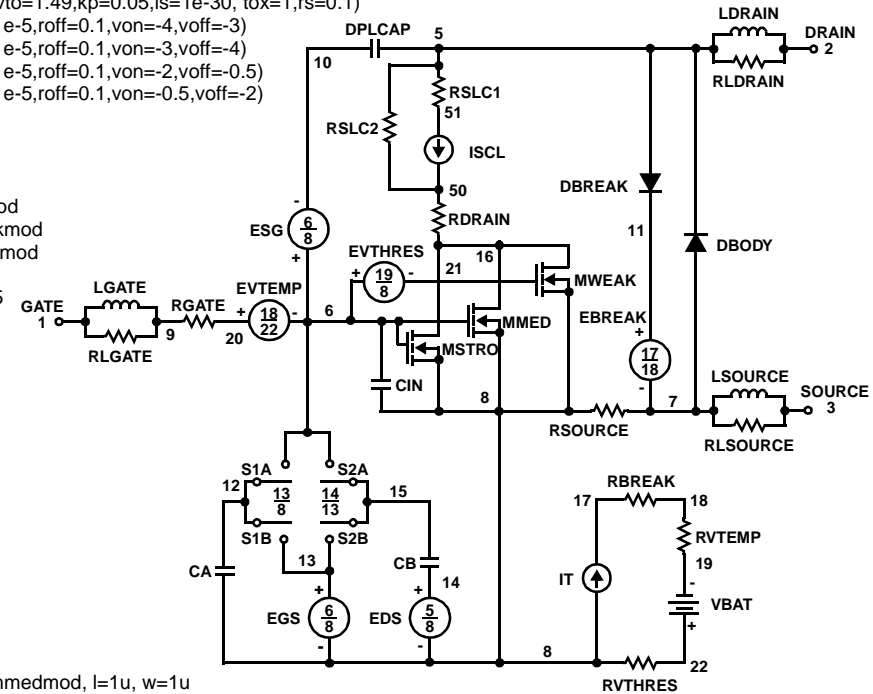
```

res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-8e-7
res.rdrain n50 n16 = 2e-3, tc1=6.7e-3,tc2=7e-6
res.rgate n9 n20 = 2.0
res.rslc1 n5 n51 = 1e-6, tc1=1e-4,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 2e-3, tc1=1e-4,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-2.1e-3,tc2=-8e-6
res.rvtemp n18 n19 = 1, tc1=-1.8e-3,tc2=2e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
  
```

```
v.vbat n22 n19 = dc=1
```

```

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51)))))*((abs(v(n5,n51))*1e6/500)** 10)
}
}
  
```



PSPICE Thermal Model

REV 23 May 2004

FDD8874T

CTHERM1 TH 6 1.9e-3
 CTHERM2 6 5 2.8e-3
 CTHERM3 5 4 3.5e-3
 CTHERM4 4 3 3.6e-3
 CTHERM5 3 2 4.0e-3
 CTHERM6 2 TL 1.6e-2

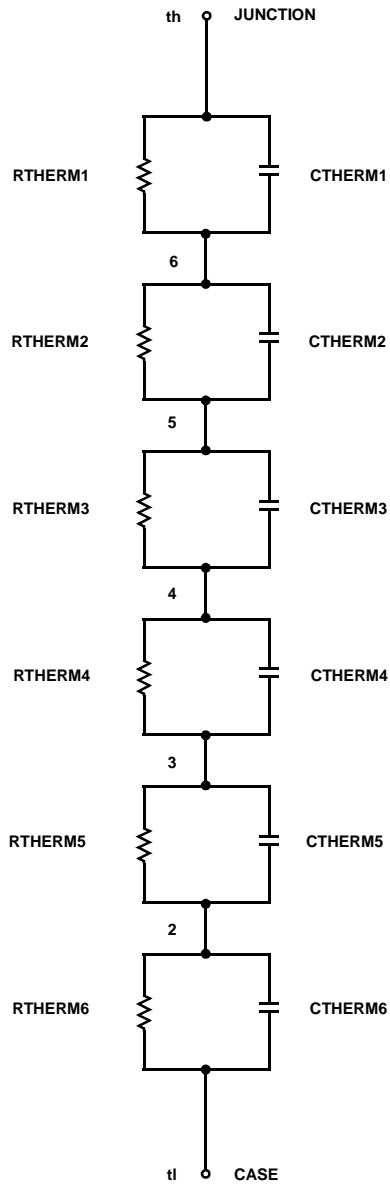
RTHERM1 TH 6 3.8e-2
 RTHERM2 6 5 5.0e-2
 RTHERM3 5 4 1.0e-1
 RTHERM4 4 3 1.8e-1
 RTHERM5 3 2 3.5e-1
 RTHERM6 2 TL 3.7e-1

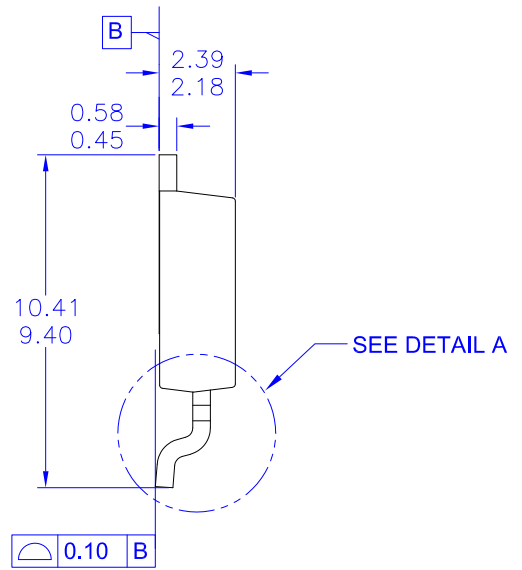
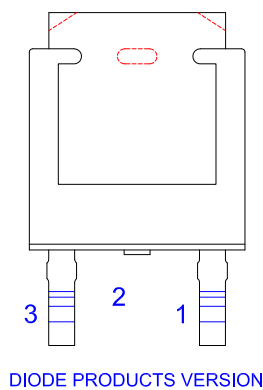
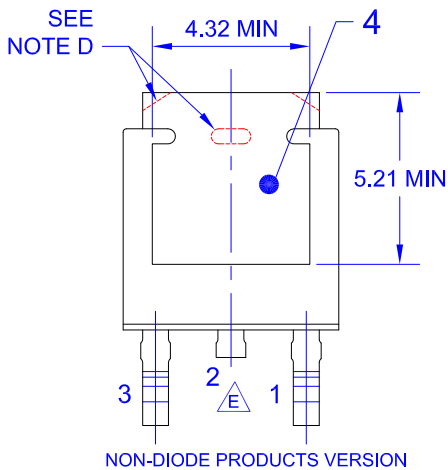
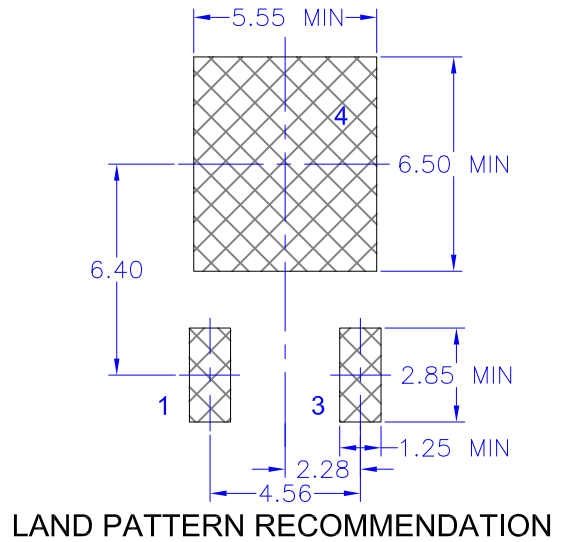
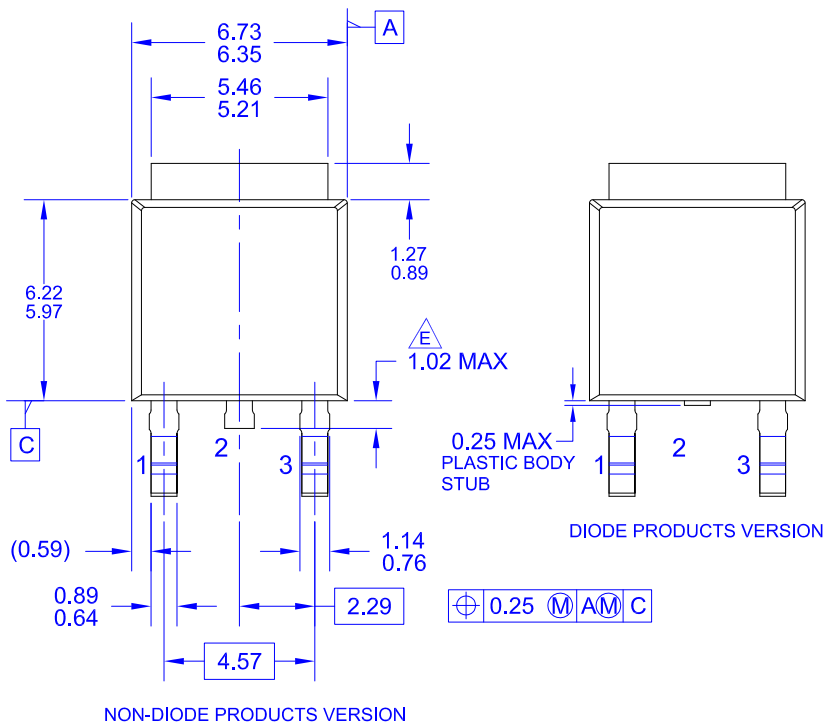
SABER Thermal Model

SABER thermal model FDD8874T
 template thermal_model th tl
 thermal_c th, tl

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{
ctherm.ctherm1 th 6 =1.9e-3
ctherm.ctherm2 6 5 =2.8e-3
ctherm.ctherm3 5 4 =3.5e-3
ctherm.ctherm4 4 3 =3.6e-3
ctherm.ctherm5 3 2 =4.0e-3
ctherm.ctherm6 2 tl =1.6e-2
```

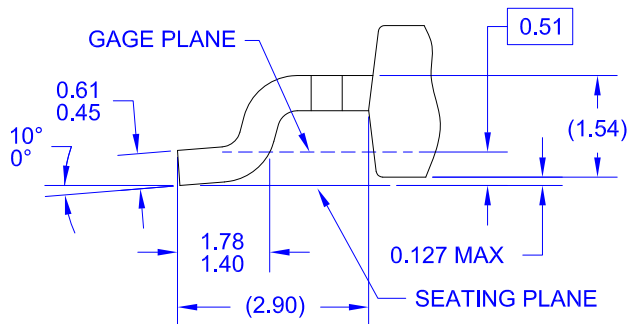
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rtherm.rtherm1 th 6 =3.8e-2
rtherm.rtherm2 6 5 =5.0e-2
rtherm.rtherm3 5 4 =1.0e-1
rtherm.rtherm4 4 3 =1.8e-1
rtherm.rtherm5 3 2 =3.5e-1
rtherm.rtherm6 2 tl =3.7e-1
}
```





NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10








DETAIL A
(ROTATED -90°)
SCALE: 12X





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FACT®	MTX®	SuperSOT™-6	XS™
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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