Low Power Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

Low Power CK505 Programmable clock

Output Features:

- 2 - 0.8V differential push-pull CPU pairs
- 1 - 25 MHz
- 5 - PCI (33MHz)
- 1 - USB, 48MHz
- 1 - 24/48MHz
- 1 - REF, 14.318MHz
- 8 - PCIEX 0.8V differential push-pull pairs
- 1 - PCIEX/DOT96MHz selectable pairs
- 1 - SATACLK differential pair
- 1 - 24.576MHz output

Features/Benefits:

- Programmable output frequencies
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Programmable watch dog safe frequency.
- Supports tight ppm accuracy clocks for Serial-ATA
- Supports spread spectrum modulation, ±0.25% center spread.
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Low Power differential outputs (50ohm resistor to GND not needed)
- Integrated 33Ω series resistor on all differential outputs

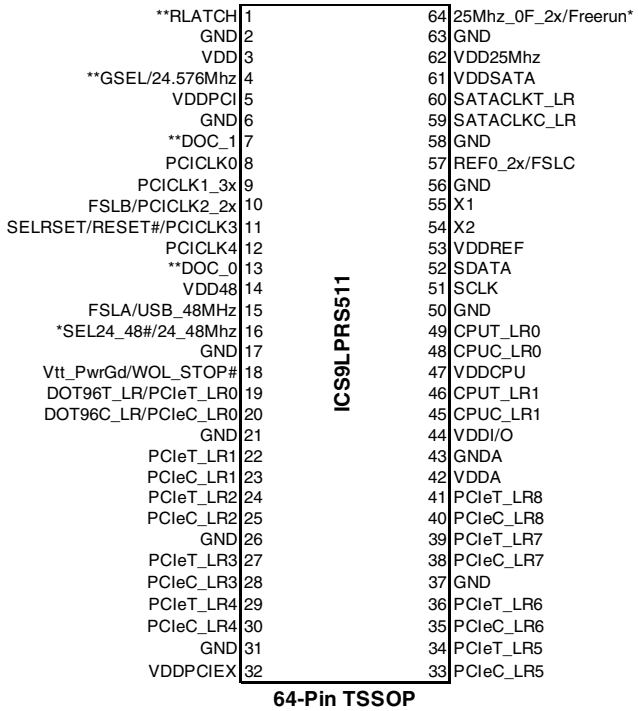
Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- PCIEX outputs cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 300ppm frequency accuracy on CPU & PCIEX clocks

Functionality Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	PCIEX	PCI	SATA
		FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	0	0	266.66	100.00	33.33	100.00
0	0	0	0	1	133.33	100.00	33.33	100.00
0	0	0	1	0	200.00	100.00	33.33	100.00
0	0	0	1	1	166.66	100.00	33.33	100.00
0	0	1	0	0	333.33	100.00	33.33	100.00
0	0	1	0	1	100.00	100.00	33.33	100.00
0	0	1	1	0	400.00	100.00	33.33	100.00
0	0	1	1	1	200.00	100.00	33.33	100.00
0	1	0	0	0	266.66	100.00	33.33	100.00
0	1	0	0	1	133.33	100.00	33.33	100.00
0	1	0	1	0	200.00	100.00	33.33	100.00
0	1	0	1	1	166.66	100.00	33.33	100.00
0	1	1	0	0	333.33	100.00	33.33	100.00
0	1	1	0	1	100.00	100.00	33.33	100.00
0	1	1	1	0	400.00	100.00	33.33	100.00
0	1	1	1	1	200.00	100.00	33.33	100.00
1	0	0	0	0	269.33	101.00	33.66	100.00
1	0	0	0	1	134.66	101.00	33.66	100.00
1	0	0	1	0	202.00	101.00	33.66	100.00
1	0	0	1	1	168.33	101.00	33.66	100.00
1	0	1	0	0	274.66	103.00	34.33	100.00
1	0	1	0	1	137.33	103.00	34.33	100.00
1	0	1	1	0	206.00	103.00	34.33	100.00
1	0	1	1	1	N/A	N/A	34.33	100.00
1	1	0	0	0	279.99	105.00	35.00	100.00
1	1	0	0	1	140.00	105.00	35.00	100.00
1	1	0	1	0	210.00	105.00	35.00	100.00
1	1	0	1	1	N/A	N/A	35.00	100.00
1	1	1	0	0	285.33	107.00	35.66	100.00
1	1	1	0	1	142.66	107.00	35.66	100.00
1	1	1	1	0	214.00	107.00	35.66	100.00
1	1	1	1	1	N/A	N/A	35.66	100.00

Pin Configuration



64-Pin TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

RESET pin is 3.3V tolerant

Pin Description

Pin#	Pin Name	Type	Pin Description
1	**RLATCH	IN	Asynchronous input pin used in combination with VTTPWRGD signal to determine whether to reset I2c.
2	GND	PWR	Ground pin.
3	VDD	PWR	Power supply, nominal 3.3V
4	**GSEL/24.576Mhz	I/O	Latch input to select PCIEX0 and DOT96 output. GSEL = 1, selects DOT 96Mhz ; GSEL = 0, selects PCIEX0. / 24.576Mhz clock output
5	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
6	GND	PWR	Ground pin.
7	**DOC_1	IN	Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2c.
8	PCICLK0	OUT	PCI clock output.
9	PCICLK1_3x	OUT	Programmable 3x strength PCICLK, default 2x
10	FSLB/PCICLK2_2x	I/O	3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values. / 3.3V PCI clock output.
11	SELRSET/RESET#/PCICLK3	I/O	Latch select input pin. SELRSET = 0, selects PCICLK, SELRSET = 1 selects RESET#
12	PCICLK4	OUT	PCI clock output.
13	**DOC_0	IN	Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2c.
14	VDD48	PWR	Power pin for the 48MHz output.3.3V
15	FSLA/USB_48MHz	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
16	*SEL24_48#/24_48Mhz	I/O	Latched select input for 24/48MHz output / 24/48MHz clock output. 1=24MHz, 0 = 48MHz.
17	GND	PWR	Ground pin.
18	Vtt_PwrGd/WOL_STOP#	IN	This active high 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled / Asynchronous active low input pin that stops all outputs except free running 25Mhz
19	DOT96T_LR/PCIeT_LR0	OUT	True clock of differential pair for 96.00MHz non-spreading DOT clock/ True clock of PCIEX0 Clock pair - selectable by GSEL; both 0.75V differential pairs are 0.75V push-pull outputs with integrated 33ohm series resistor.
20	DOT96C_LR/PCIeC_LR0	OUT	Complementary clock of differential pair for 96.00MHz non-spreading DOT clock/ Complementary clock of PCIEX0 Clock pair - selectable by GSEL; both 0.75V differential pairs are 0.75V push-pull outputs with integrated 33ohm series resistor.
21	GND	PWR	Ground pin.
22	PCIeT_LR1	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
23	PCIeC_LR1	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
24	PCIeT_LR2	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
25	PCIeC_LR2	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
26	GND	PWR	Ground pin.
27	PCIeT_LR3	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
28	PCIeC_LR3	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
29	PCIeT_LR4	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
30	PCIeC_LR4	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
31	GND	PWR	Ground pin.
32	VDDPCIEX	PWR	Power supply for PCI Express clocks, nominal 3.3V

Pin Description (Continued)

Pin#	Pin Name	Type	Pin Description
33	PCIeC_LR5	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
34	PCIeT_LR5	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
35	PCIeC_LR6	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
36	PCIeT_LR6	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
37	GND	PWR	Ground pin.
38	PCIeC_LR7	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
39	PCIeT_LR7	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
40	PCIeC_LR8	OUT	Complement clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
41	PCIeT_LR8	OUT	True clock of 0.75V differential push-pull PCI_Express pair with integrated 33ohm series resistor
42	VDDA	PWR	3.3V power for the PLL core.
43	GNDA	PWR	Ground pin for the PLL core.
44	VDDI/O	PWR	Power supply for differential outputs
45	CPUC_LR1	OUT	Complementary clock of differential pair 0.75V push-pull CPU outputs with integrated 33ohm series resistor.
46	CPUT_LR1	OUT	True clock of differential pair 0.75V push-pull CPU outputs with integrated 33ohm series resistor.
47	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
48	CPUC_LR0	OUT	Complementary clock of differential pair 0.75V push-pull CPU outputs with integrated 33ohm series resistor.
49	CPUT_LR0	OUT	True clock of differential pair 0.75V push-pull CPU outputs with integrated 33ohm series resistor.
50	GND	PWR	Ground pin.
51	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
52	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
53	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
54	X2	OUT	Crystal output, Nominally 14.318MHz
55	X1	IN	Crystal input, Nominally 14.318MHz.
56	GND	PWR	Ground pin.
57	REF0_2x/FSLC	I/O	2x strength 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
58	GND	PWR	Ground pin.
59	SATACLKC_LR	OUT	Complement clock of 0.75V push-pull differential SATA pair with integrated 33ohm series resistor.
60	SATACLKT_LR	OUT	True clock of 0.75V push-pull differential SATA pair with integrated 33ohm series resistor.
61	VDDSATA	PWR	Supply for SATA clocks, 3.3V nominal
62	VDD25Mhz	PWR	Power supply for 25MHz clocks, 3.3V nominal.
63	GND	PWR	Ground pin.
64	25Mhz_0F_2x/Freerun*	I/O	2x strength 25MHz clock output, 3.3V (free running by default) / Latch input to select if 25Mhz_0 is freerunning or stoppable on power up default. Freerun = 1, 25Mhz_0 is free running, Freerun = 0, 25Mhz_0 is stoppable.

General Description

ICS9LPRS511 follows the Intel CK505-compliant clock specification. This clock synthesizer provides a single chip solution for next generation P4 Intel processors and Intel chipsets. **ICS9LPRS511** is driven with a 14.318MHz crystal.

Block Diagram

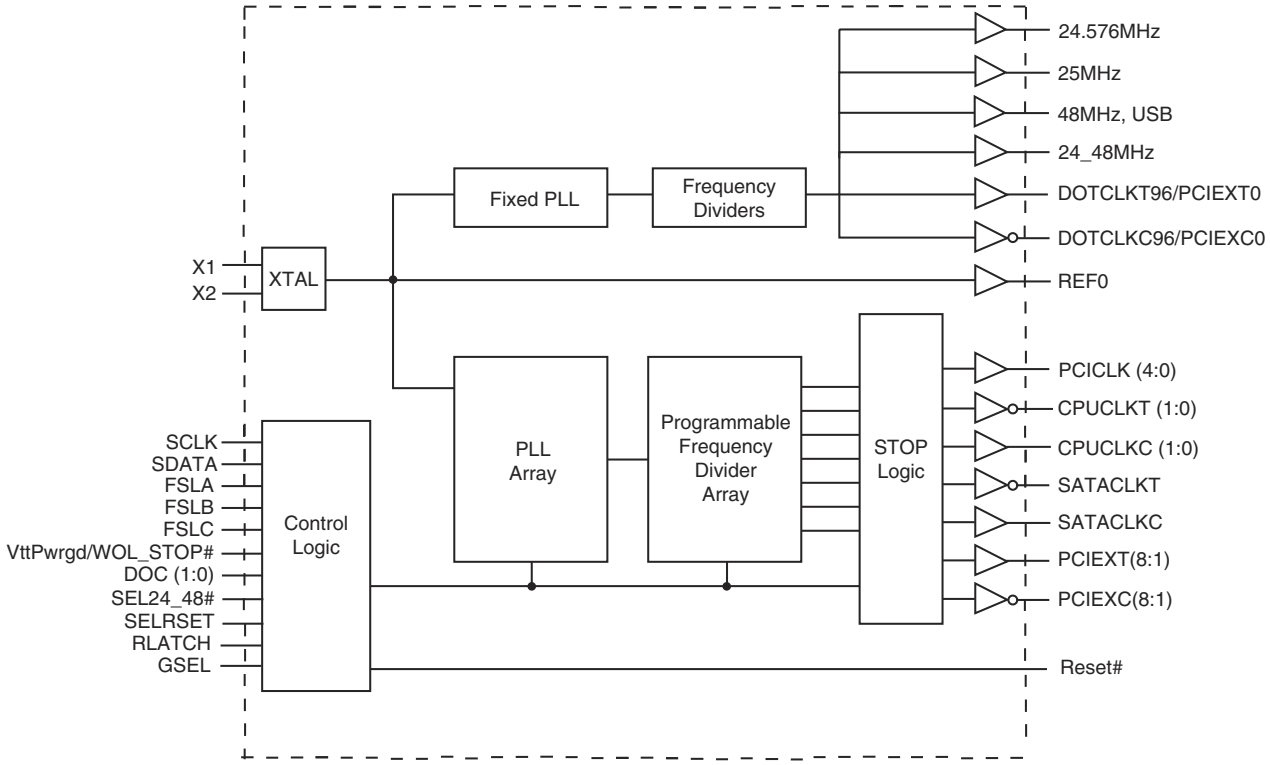


Table1: CPU PLL Frequency Selection Table

B0b4	B0b3	B0b2	B0b1	B0b0	CPU	PCIEX (B21b7 = 1)	Spread
		FSLC	FSLB	FSLA	MHz	MHz	%
0	0	0	0	0	266.66	100.00	0-0.5% Down
0	0	0	0	1	133.33	100.00	0-0.5% Down
0	0	0	1	0	200.00	100.00	0-0.5% Down
0	0	0	1	1	166.66	100.00	0-0.5% Down
0	0	1	0	0	333.33	100.00	0-0.5% Down
0	0	1	0	1	100.00	100.00	0-0.5% Down
0	0	1	1	0	400.00	100.00	0-0.5% Down
0	0	1	1	1	200.00	100.00	0-0.5% Down
0	1	0	0	0	266.66	100.00	+/-0.25% Center
0	1	0	0	1	133.33	100.00	+/-0.25% Center
0	1	0	1	0	200.00	100.00	+/-0.25% Center
0	1	0	1	1	166.66	100.00	+/-0.25% Center
0	1	1	0	0	333.33	100.00	+/-0.25% Center
0	1	1	0	1	100.00	100.00	+/-0.25% Center
0	1	1	1	0	400.00	100.00	+/-0.25% Center
0	1	1	1	1	200.00	100.00	+/-0.25% Center
1	0	0	0	0	269.33	101.00	+/- 0.3% Center
1	0	0	0	1	134.66	101.00	+/- 0.3% Center
1	0	0	1	0	202.00	101.00	+/- 0.3% Center
1	0	0	1	1	168.33	101.00	+/- 0.3% Center
1	0	1	0	0	274.66	103.00	+/- 0.3% Center
1	0	1	0	1	137.33	103.00	+/- 0.3% Center
1	0	1	1	0	206.00	103.00	+/- 0.3% Center
1	0	1	1	1	N/A	N/A	+/- 0.3% Center
1	1	0	0	0	279.99	105.00	+/- 0.3% Center
1	1	0	0	1	140.00	105.00	+/- 0.3% Center
1	1	0	1	0	210.00	105.00	+/- 0.3% Center
1	1	0	1	1	N/A	N/A	+/- 0.3% Center
1	1	1	0	0	285.33	107.00	+/- 0.3% Center
1	1	1	0	1	142.66	107.00	+/- 0.3% Center
1	1	1	1	0	214.00	107.00	+/- 0.3% Center
1	1	1	1	1	N/A	N/A	+/- 0.3% Center

Table2: PCIEX PLL Frequency Selection Table

B19b4	B19b3	B19b2	B19b1	B19b0	PCIEX (B21b7 = 0)	PCI	SATA (B21b6 = 0)	Spread
		FSLC	FSLB	FSLA	MHz	MHz	MHz	%
0	0	0	0	0	100.00	33.33	100.00	0-0.5% Down
0	0	0	0	1	100.00	33.33	100.00	0-0.5% Down
0	0	0	1	0	100.00	33.33	100.00	0-0.5% Down
0	0	0	1	1	100.00	33.33	100.00	0-0.5% Down
0	0	1	0	0	100.00	33.33	100.00	0-0.5% Down
0	0	1	0	1	100.00	33.33	100.00	0-0.5% Down
0	0	1	1	0	100.00	33.33	100.00	0-0.5% Down
0	0	1	1	1	100.00	33.33	100.00	0-0.5% Down
0	1	0	0	0	100.00	33.33	100.00	+/-0.25% Center
0	1	0	0	1	100.00	33.33	100.00	+/-0.25% Center
0	1	0	1	0	100.00	33.33	100.00	+/-0.25% Center
0	1	0	1	1	100.00	33.33	100.00	+/-0.25% Center
0	1	1	0	0	100.00	33.33	100.00	+/-0.25% Center
0	1	1	0	1	100.00	33.33	100.00	+/-0.25% Center
0	1	1	1	0	100.00	33.33	100.00	+/-0.25% Center
0	1	1	1	1	100.00	33.33	100.00	+/-0.25% Center
1	0	0	0	0	101.00	33.66	101.00	+/- 0.3% Center
1	0	0	0	1	101.00	33.66	101.00	+/- 0.3% Center
1	0	0	1	0	101.00	33.66	101.00	+/- 0.3% Center
1	0	0	1	1	101.00	33.66	101.00	+/- 0.3% Center
1	0	1	0	0	103.00	34.33	103.00	+/- 0.3% Center
1	0	1	0	1	103.00	34.33	103.00	+/- 0.3% Center
1	0	1	1	0	103.00	34.33	103.00	+/- 0.3% Center
1	0	1	1	1	103.00	34.33	103.00	+/- 0.3% Center
1	1	0	0	0	105.00	35.00	105.00	+/- 0.3% Center
1	1	0	0	1	105.00	35.00	105.00	+/- 0.3% Center
1	1	0	1	0	105.00	35.00	105.00	+/- 0.3% Center
1	1	0	1	1	105.00	35.00	105.00	+/- 0.3% Center
1	1	1	0	0	107.00	35.66	107.00	+/- 0.3% Center
1	1	1	0	1	107.00	35.66	107.00	+/- 0.3% Center
1	1	1	1	0	107.00	35.66	107.00	+/- 0.3% Center
1	1	1	1	1	107.00	35.66	107.00	+/- 0.3% Center

General I²C serial interface information for the ICS9LPRS511

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

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I2C Table: Frequency Select Register

Byte 0	Name	Control Function	Type	0	1	PWD A/B	PWD C/D/E/H/J
Bit 7	ROD	Reset on Demand	RW	Disable	Enable	0	0
Bit 6	PCIEX_SS	PCIEX PLL Spread Enable	RW	OFF	ON	1	0
Bit 5	CPU_SS	CPU PLL Spread Enable	RW	OFF	ON	1	1
Bit 4	FS4	Freq Select Bit 4	RW	See Table 1: Frequency Selection Table		0	0
Bit 3	FS3	Freq Select Bit 3	RW			0	0
Bit 2	FSLC	Freq Select Bit 2	RW			Latch	Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch	Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch	Latch

I2C Table: Frequency Select Register

Byte 1	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	SEL24_48	Select 24_48Mhz	RW	48	24	latch
Bit 6	I2c RB	Select I2c readback from	RW	Shadow RAM	Active RAM	1
Bit 5	SELRSET	Select RESET	RW	PCICLK4	Reset#	latch
Bit 4	PCIEX PLL MNEN	PCIEX PLL M/N Enable	RW	Disable	Enable	0
Bit 3	CPU PLL MNEN	CPU PLL M/N Enable	RW	Disable	Enable	0
Bit 2	25Mhz_0F	Free-running control during WOL_STOP	RW	Stoppable	Free-running	latch
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	GSEL	GSEL selection	RW	PCIEX0	DOT96Mhz	latch

I2C Table: Output Control Register

Byte 2	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	USB_48Mhz	Output Control	RW	Disable	Enable	1
Bit 6	PCIEXT/C8	Output Control	RW	Disable	Enable	1
Bit 5	SATACLK	Output Control	RW	Disable	Enable	1
Bit 4	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 3	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 2	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 1	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 0	Reserved	Reserved	RW	-	-	1

I2C Table: Output Control Register

Byte 3	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 6	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 5	PCIEXT/C7	Output Control	RW	Disable	Enable	1
Bit 4	PCIEXT/C6	Output Control	RW	Disable	Enable	1
Bit 3	PCIEXT/C5	Output Control	RW	Disable	Enable	1
Bit 2	PCIEXT/C4	Output Control	RW	Disable	Enable	1
Bit 1	PCIEXT/C3	Output Control	RW	Disable	Enable	1
Bit 0	PCIEXT/C2	Output Control	RW	Disable	Enable	1

I2C Table: Output Control Register

Byte 4	Name	Control Function		0	1	PWD A/B/C/D/E/H/J
Bit 7	PCIEXT/C1	Output Control	RW	Disable	Enable	1
Bit 6	REF0	Output Control	RW	Disable	Enable	1
Bit 5	CPUCLK1	Output Control	RW	Disable	Enable	1
Bit 4	CPUCLK0	Output Control	RW	Disable	Enable	1
Bit 3	24.576Mhz	Output Control	RW	Disable	Enable	1
Bit 2	Dot96Mhz/PCIEXT/C0	Output Control	RW	Disable	Enable	1
Bit 1	25Mhz_0F	Output Control	RW	Disable	Enable	1
Bit 0	Reserved	Reserved	RW	-	-	1

I2C Table: Output Control Register

Byte 5	Name	Control Function		0	1	PWD A/B/C/D/E/H/J
Bit 7	24_48Mhz	Output Control	RW	Disable	Enable	1
Bit 6	Diff AMP	Differential output Amplitude Control	RW	00 = 600mV	01 = 900mV	1
Bit 5	Diff AMP		RW	10 = 800mV	11 = 700mV	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	iAMT EN (only applicable to revisions H and J, otherwise this is a reserved bit)	iAMT Enable Control	RW	Stoppable	Free-running	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Load Control	IIC Load control	RW	Load	Do not Load	0

I2C Table: Reserved Register

Byte 6	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	Reserved	Reserved	RW		-	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	Reserved	Reserved	RW	-	-	0

I2C Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	PWD A/B	PWD C/D	PWD E	PWD H	PWD J
Bit 7	RID3	Revision ID	R	-	-	0	0	0	0	0
Bit 6	RID2		R	-	-	0	0	1	1	1
Bit 5	RID1		R	-	-	0	1	0	0	1
Bit 4	RID0		R	-	-	0	0	0	1	0
Bit 3	VID3	VENDOR ID	R	-	-	0	0	0	0	0
Bit 2	VID2		R	-	-	0	0	0	0	0
Bit 1	VID1		R	001 = ICS	-	0	0	0	0	0
Bit 0	VID0		R	-	-	1	1	1	1	1

I2C Table: Byte Count Register

Byte 8	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	BC7	Byte Count Programming b(7:0)	R	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.		0
Bit 6	BC6		R			0
Bit 5	BC5		R			0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			1
Bit 1	BC1		RW			1
Bit 0	BC0		RW			1

I2C Table: Watch Dog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable	Enable	0
Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW			1

I2C Table: WD Safe Frequency Control Register

Byte 10	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW			1
Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW			1
Bit 4	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte10 bit (4:0).		0
Bit 3	WD SF3		RW			0
Bit 2	WD SF2		RW			0
Bit 1	WD SF1		RW			0
Bit 0	WD SF0		RW			0

I²C Table: CPU PLL Frequency Control Register

Byte 11	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

I2C Table: CPU PLL Frequency Control Register (DOC0 = 0)

Byte 12	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	N Div10	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 12 will configure the CPU PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

I2C Table: CPU PLL Spread Spectrum Control Register

Byte 13	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of CPU PLL		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

I2C Table: CPU PLL Spread Spectrum Control Register

Byte 14	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	SSP15	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of CPU PLL		0
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

I2C Table: PCIEX PLL Frequency Control Register

Byte 15	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 15 and 16 will configure the PCIEX PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div1	N Divider Prog bit 1	RW			X
Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	M Div4		RW			X
Bit 3	M Div3		RW			X
Bit 2	M Div2		RW			X
Bit 1	M Div1		RW			X
Bit 0	M Div0		RW			X

I2C Table: PCIEX PLL Frequency Control Register (DOC0 = 0)

Byte 16	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	N Div10	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 15 and 16 will configure the PCIEX PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

I2C Table: PCIEX PLL Spread Spectrum Control Register

Byte 17	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of PCIEX PLL		X
Bit 6	SSP6		RW			X
Bit 5	SSP5		RW			X
Bit 4	SSP4		RW			X
Bit 3	SSP3		RW			X
Bit 2	SSP2		RW			X
Bit 1	SSP1		RW			X
Bit 0	SSP0		RW			X

I2C Table: PCIEX PLL Spread Spectrum Control Register

Byte 18	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	SSP15	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread percentage of PCIEX PLL		0
Bit 6	SSP14		RW			X
Bit 5	SSP13		RW			X
Bit 4	SSP12		RW			X
Bit 3	SSP11		RW			X
Bit 2	SSP10		RW			X
Bit 1	SSP9		RW			X
Bit 0	SSP8		RW			X

I2C Table: PCIEX PLL Frequency Select Register

Byte 19	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	Reserved	Reserved	RW	-	-	1
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	FS4	Freq Select Bit 4	RW	See Table 2: PCIEX PLL Frequency Selection Table		0
Bit 3	FS3	Freq Select Bit 3	RW			0
Bit 2	FSLC	Freq Select Bit 2	RW			Latch
Bit 1	FSLB	Freq Select Bit 1	RW			Latch
Bit 0	FSLA	Freq Select Bit 0	RW			Latch

I2C Table: Output Control Register

Byte 20	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	Reserved	Reserved	RW	-	-	0
Bit 6	Reserved	Reserved	RW	-	-	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	PCIEX PLL TBEN	PCIEX PLL Turbo Enable	RW	Disable	Enable	0
Bit 2	CPU PLL TBEN	CPU PLL Turbo Enable	RW	Disable	Enable	0
Bit 1	Reserved	Reserved	RW	-	-	0
Bit 0	RESET Sync	Reset Synchronization upon Reset (Byte 21)	RW	Disable	Enable	0

I2C Table: Synchronization Control Register

Byte 21	Name	Control Function	Type	0	1	PWD A/B	PWD C/D/E/H	PWD J
Bit 7	PCIEX Source	PCIEX Source	RW	PCIEX PLL	CPU PLL	0	1	0
Bit 6	SATA Source	SATA Source	RW	PCIEX PLL	Fixed PLL	1	1	1
Bit 5	Reserved	Reserved	RW	-	-	1	1	1
Bit 4	Reserved	Reserved	RW	-	-	1	1	1
Bit 3	Reserved	Reserved	RW	-	-	1	1	1
Bit 2	Reserved	Reserved	RW	-	-	1	1	1
Bit 1	Reserved	Reserved	RW	-	-	1	1	1
Bit 0	Reserved	Reserved	RW	-	-	1	1	1

I2C Table: DOC pin control register

Byte 22	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	PCIEX	PCIEX PLL DOC0 pin control	RW	Enabled	Disabled	1
Bit 6	CPU	CPU PLL DOC0 pin control	RW	Enabled	Disabled	0
Bit 5	Reserved	Reserved	RW	-	-	0
Bit 4	Reserved	Reserved	RW	-	-	0
Bit 3	Reserved	Reserved	RW	-	-	0
Bit 2	Reserved	Reserved	RW	-	-	0
Bit 1	Reserved	Reserved	RW	-	-	1
Bit 0	Reserved	Reserved	RW	-	-	1

I2C Table: CPU PLL DOC 1 N programming Register (DOC0 = 1)

Byte 23	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	N Div10	N Divider Programming Byte23 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 11 and 23 will configure the CPU PLL VCO frequency. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

Bytes 24 and 25 are reserved

I2C Table: PCIEX PLL DOC 1 N programming Register (DOC0 = 1)

Byte 26	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	N Div10	N Divider Programming Byte26 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 15 and 26 will configure the PCIEX PLL VCO frequency. VCO Frequency = 14.318 x Ndiv(10:0)/Mdiv(5:0)		X
Bit 6	N Div9		RW			X
Bit 5	N Div8		RW			X
Bit 4	N Div7		RW			X
Bit 3	N Div6		RW			X
Bit 2	N Div5		RW			X
Bit 1	N Div4		RW			X
Bit 0	N Div3		RW			X

Bytes 27 and 28 are reserved

I2C Table: Programmable output divider Register

Byte 29	Name	Control Function	Type	0		1		PWD A/B/C/D/E/H/J
Bit 7	CPUDiv3	CPU Divider Ratio Programming Bits	RW	0000:/2	0100:/4	1000:/8	1100:/16	X
Bit 6	CPUDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	CPUDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/20	X
Bit 4	CPUDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X
Bit 3	PCIEXDiv3	PCIEX Divider Ratio Programming Bits for CPU PLL	RW	0000:/2	0100:/4	1000:/8	1100:/10	X
Bit 2	PCIEXDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	PCIEXDiv1		RW	0010:/5	0110:/10	1010:/20	1110:/20	X
Bit 0	PCIEXDiv0		RW	0011:/7	0111:/14	1011:/28	1111:/56	X

I2C Table: Programmable output divider Register

Byte 30	Name	Control Function	Type	0		1		PWD A/B/C/D/E/H/J
Bit 7	PCIEXDiv3	PCIEX Divider Ratio Programming Bits for PCIEX PLL	RW	0000:/5	0100:/10	1000:/20	1100:/40	X
Bit 6	PCIEXDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 5	PCIEXDiv1		RW	0010:/N/A	0110:/N/A	1010:/N/A	1110:/N/A	X
Bit 4	PCIEXDiv0		RW	0011:/N/A	0111:/N/A	1011:/N/A	1111:/N/A	X
Bit 3	PCIDiv3	PCI Divider Ratio Programming Bits	RW	0000:/N/A	0100:/N/A	1000:/N/A	1100:/N/A	X
Bit 2	PCIDiv2		RW	0001:/3	0101:/6	1001:/12	1101:/24	X
Bit 1	PCIDiv1		RW	0010:/9	0110:/18	1010:/36	1110:/72	X
Bit 0	PCIDiv0		RW	0011:/N/A	0111:/N/A	1011:/N/A	1111:/N/A	X

I2C Table: Strength Control Register

Byte 31	Name	Control Function	Type	0	1	PWD A/B/C/D/E/H/J
Bit 7	25Str_1	25Mhz_0 Strength Control	RW	00 = tristated	10 = 1.00x	1
Bit 6	25Str_0		RW	01 = 0.1x	11 = 2.00x	1
Bit 5	REFStr_1	REFCLK0 Strength Control	RW	00 = tristated	10 = 1.00x	1
Bit 4	REFStr_0		RW	01 = 0.1x	11 = 2.00x	1
Bit 3	PCIStr_1	PCICLK1 Strength Control	RW	00 = tristated	10 = 1.00x	0
Bit 2	PCIStr_0		RW	01 = 2.00x	11 = 3.00x	1
Bit 1	PCIStr_1	PCICLK2 Strength Control	RW	00 = tristated	10 = 1.00x	1
Bit 0	PCIStr_0		RW	01 = 0.1x	11 = 2.00x	1

I2C Table: Skew programming Register

Byte 32	Name	Control Function	Type	0		1		PWD A/B/C/D/E/H/J
Bit 7	CPUSkw3	CPUCLK0 Skew Control (ps)	RW	0000:0	0100:400	1000:800	1100:1200	0
Bit 6	CPUSkw2		RW	0001:100	0101:500	1001:900	1101:1300	0
Bit 5	CPUSkw1		RW	0010:200	0110:600	1010:1000	1110:1400	0
Bit 4	CPUSkw0		RW	0011:300	0111:700	1011:1100	1111:1500	0
Bit 3	CPUSkw3	CPUCLK1 Skew Control (ps)	RW	0000:0	0100:400	1000:800	1100:1200	0
Bit 2	CPUSkw2		RW	0001:100	0101:500	1001:900	1101:1300	0
Bit 1	CPUSkw1		RW	0010:200	0110:600	1010:1000	1110:1400	0
Bit 0	CPUSkw0		RW	0011:300	0111:700	1011:1100	1111:1500	0

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage		4.6	V	1,7
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply		3.8	V	1,7
Maximum Input Voltage	V_{IH}	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5		V	1,7
Storage Temperature	Ts	-	-65	150	˚C	1,7
Case Temperature	Tcase	-		115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	1
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	1.05	3.465	V	1
Input High Voltage	V_{IHSE}	Single-ended inputs	2	V_{DD} + 0.3	V	1
Input Low Voltage	V_{ILSE}	Single-ended inputs	V_{SS} - 0.3	0.8	V	1
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	1
Input Leakage Current	I_{INRES}	Inputs with pull or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	1
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1
Output High Voltage	V_{OHDIF}	Differential Outputs, I_{OH} = TBD mA	0.7	0.9	V	1
Output Low Voltage	V_{OLDIF}	Differential Outputs, I_{OL} = TBD mA		0.4	V	1
Low Threshold Input-High Voltage (Test Mode)	$V_{IH\_FS\_TEST}$	3.3 V +/-5%	2	V_{DD} + 0.3	V	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7	1.5	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	1
Operating Supply Current	$I_{DD\_DEFAULT}$	3.3V supply, PLL3 off		TBD	mA	1
	$I_{DD\_PLL3DIF}$	3.3V supply, PLL3 Differential Out		TBD	mA	1
	I_{DD_PLL3SE}	3.3V supply, PLL3 Single-ended Out		TBD	mA	1
	I_{DD_IO}	0.8V supply, Differential IO current, all outputs enabled		TBD	mA	1
Power Down Current	$I_{DD\_PD3.3}$	3.3V supply, Power Down Mode		TBD	mA	1
	I_{DD_PDIO}	0.8V IO supply, Power Down Mode		TBD	mA	1
iAMT Mode Current	$I_{DD\_iAMT3.3}$	3.3V supply, iAMT Mode		TBD	mA	1
	$I_{DD\_iAMT0.8}$	0.8V IO supply, iAMTMode		TBD	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		TBD	MHz	2
Pin Inductance	L_{pin}			7	nH	1
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	1
	C_{OUT}	Output pin capacitance		6	pF	1
	C_{INX}	X1 & X2 pins		TBD	pF	1
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	33	kHz	1

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AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock		1.8	ms	1
Tdrive_SRC	T_{DRSRC}	SRC output enable after PCI_STOP# de-assertion		15	ns	1
Tdrive_PD#	T_{DRPD}	Differential output enable after PD# de-assertion		300	us	1
Tdrive_CPU	T_{DRSRC}	CPU output enable after CPU_STOP# de-assertion		10	ns	1
Tfall_PD#	T_{FALL}	Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs		5	ns	1
Trise_PD#	T_{RISE}			5	ns	1

AC Electrical Characteristics - (CPU, PCIEX, SATACLK, DOT96Mhz) Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5	8	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5	8	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		250	ps	1
CPU[1:0] Skew	CPU_{SKEW10}	Differential Measurement		100	ps	1
CPU[2_ITP:0] Skew	CPU_{SKEW20}	Differential Measurement		150	ps	1
SRC[10:0] Skew	SRC_{SKEW}	Differential Measurement		TBD	ps	1

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,6
Clock period	T_{period}	33.33MHz output nominal	29.99100	30.00900	ns	6
		33.33MHz output spread		30.15980	ns	6
Absolute min/max period	T_{abs}	33.33MHz output nominal/spread	29.49100	30.65980	ns	6
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33		mA	1
		V_{OH}@MAX = 3.135 V		-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30		mA	1
		V_{OL} @ MAX = 0.4 V		38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1
Skew	t_{skew}	V_T = 1.5 V		250	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		500	ps	1

Electrical Characteristics - USB48MHz, 24_48Mhz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.83125	20.83542	ns	2
Absolute min/max period	T_{abs}	48.00MHz output nominal	20.48130	21.18540	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29		mA	1
		V_{OH}@MAX = 3.135 V		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29		mA	1
		V_{OL} @ MAX = 0.4 V		27	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		350	ps	1

Electrical Characteristics - SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	1
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	F_{SMBUS}	Block Mode		100	kHz	1

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8203	69.8622	ns	2
Absolute min/max period	T_{abs}	14.318MHz output nominal	69.8203	70.86224	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-33	-33	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	30	38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	1
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V		1000	ps	1

Notes on Electrical Characteristics:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

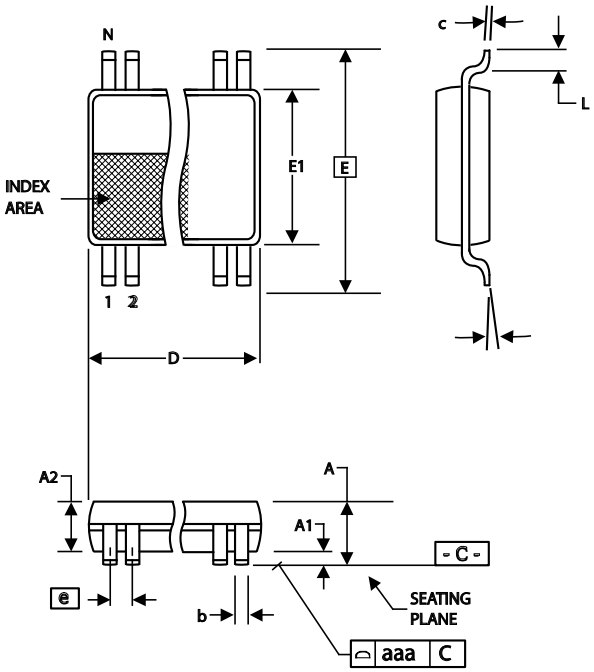
[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Maximum input voltage is not to exceed maximum VDD



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS9LPRS511yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

1137—09/05/08

Revision History

Rev.	Issue Date	Description	Page #
0.1	8/3/2005	Initial Release	-
0.2	8/17/2005	Updated pinout and invert VTTPWRGD/WOL_STOP polarity	1-4
0.3	8/25/2005	Added I2c Tables	8-21
0.4	8/31/2005	Updated pinout (DOC1 removed, PCICLK1 added)	1-3, 19-21
0.5	9/19/2005	1) Updated pinout, pin description (move freerun latch from PCICLK to 25Mhz_0) 2) Updated I2c Bytes 1, 5, 22, 31	1-3, 8-18
0.6	10/6/2005	1) Changed pin 42, 53, 61 and 62 from Standby (Non Collapsible) Power to Standard Power. 2) Removed Power Groups Table.	1,3, 4
0.7	4/7/2006	Updated I2C.	8-18
0.5	7/31/2006	1. Updated Pinout. 2. Updated Pin Description.	1,2
0.6	9/26/2006	1. Updated I2C.	8-13
0.7	11/2/2006	1. Updated Output Features to represent low power. 2. Updated I2C.	Various
0.8	10/4/2007	Updated Functionality and CPU frequency table	1, 5
0.9	9/5/2008	Added Case Temperature @ 115C to Max Rating Table.	14

Silicon Revision History

Rev.	Description
0.1	B0b6 = 1 in revisions [A:B] B0b6 = 0 in revisions [C:J]
0.2	B7 = 01h in revisions [A:B] B7 = 21h in revisions [C:D] B7 = 41h in revision E B7 = 51h in revision H B7 = 61h in revision J
0.3	B21b7 = 0 in revisions [A:B] B21b7 = 1 in revisions [C:H] B21b7 = 0 in revision J

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