ANALOG DEVICES

Radar Receive Path AFE: 4-Channel Mux with LNA, PGA, AAF, and ADC

Data Sheet

FEATURES

4-channel mux to LNA, PGA, AAF
1 direct-to-ADC channel
Programmable gain amplifier (PGA)
Includes low noise preamplifier (LNA)
SPI-programmable gain = 17 dB to 35 dB in 6 dB steps
Antialiasing filter (AAF)
Programmable third-order low-pass elliptic filter (LPF) from
    9 MHz to 15 MHz
Analog-to-digital converter (ADC)
12 bits of accuracy of up to 60 MSPS
SNR = 67 dB
SFDR = 68 dBc
Low power, 345 mW at 12 bits per 60 MSPS
Low noise, 3.5 nV/√Hz maximum of input referred
    voltage noise
Power-down mode
64-lead, 10 mm × 10 mm TQFP package
Specified from −40°C to +105°C
Qualified for automotive applications

APPLICATIONS

Automotive radar
    Adaptive cruise control
    Collision avoidance
    Blind spot detection
    Self parking
    Electronic bumper

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The _____ is an integrated analog front end designed for low cost, compact size, flexibility, and ease of use. It contains a 4-channel differential multiplexer (mux), a 1-channel low noise preamplifier (LNA) with a programmable gain amplifier (PGA) and an antialiasing filter (AAF), as well as one direct-to-ADC channel, all integrated with a single, 12-bit analog-to-digital converter (ADC). The _____ also incorporates a saturation detection circuit for high frequency overvoltage conditions that would otherwise be filtered by the AAF.

The analog channel features a gain range of 17 dB to 35 dB in 6 dB increments, and an ADC with a conversion rate of up to 60 MSPS. The combined input referred voltage noise of the entire channel is 3.5 nV/√Hz at maximum gain. The channel is optimized
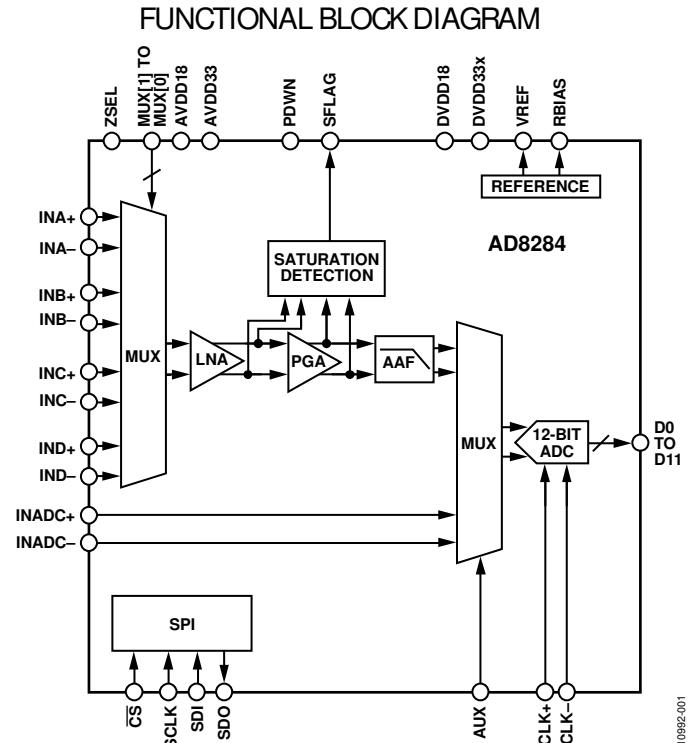
for dynamic performance and low power in applications where a small package size is critical.

Fabricated in an advanced CMOS process, the _____ is available in a 10 mm × 10 mm, RoHS compliant, 64-lead TQFP. It is specified over the automotive temperature range of −40°C to +105°C.

Table 1. Related Devices

Part No.	Description
	4-Channel LNA/PGA/AAF, pseudosimultaneous channel sampling with ADC
	6-Channel LNA/PGA/AAF, pseudosimultaneous channel sampling with ADC
	4-Channel LNA/PGA

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REVISION HISTORY

8/15—Rev. C to Rev. D
Changed AD951x/AD952x to AD9515/AD9520-0.... Throughout
Added Table 1; Renumbered Sequentially 1

6/14—Rev. B to Rev. C
Changed 80 MSPS to 60 MSPS .... Throughout
Changes to Table 1 3
Changed 6.25 to 8.33, Clock Pulse Width High Parameter,
Clock Pulse Width Low Parameter, and Data Setup Time
Parameter, Table 3 6

7/13—Rev. A to Rev. B
Changes to Input Resistance and Power-Down Dissipation
Parameters; Table 1 3
Updated Outline Dimensions 26
Changes to Ordering Guide 26

1/13—Rev. 0 to Rev. A
Changes to Figure 16... 14

10/12—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

AVDD18x = 1.8 V, AVDD33x = 3.3 V, DVDD18x = 1.8 V, DVDD33x = 3.3 V, 1.0 V internal ADC reference, f_{IN} = 2.5 MHz, f_S = 60 MSPS, R_S = 50 Ω, LNA + PGA gain = 35 dB, LPF cutoff = $f_{SAMPLECH}$/4, 12-bit operation, temperature = −40℃ to +105℃, all specifications guaranteed by testing, unless otherwise noted.

Table 2.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG CHANNEL CHARACTERISTICS	LNA, PGA, and AAF channel				
Gain	Programmable		17/23/29/35		dB
Gain Range			18		dB
Gain Error		−1.25		+1.25	dB
Input Voltage Range[2]	Channel gain = 17 dB		0.283		V p-p
	Channel gain = 23 dB		0.142		V p-p
	Channel gain = 29 dB		0.071		V p-p
	Channel gain = 35 dB		0.036		V p-p
Input Resistance	200 Ω input impedance	0.200	0.265	0.300	kΩ
	200 kΩ input impedance	160	200	240	kΩ
Input Capacitance[2]			7		pF
Input Referred Voltage Noise[2]	Maximum gain at 1 MHz			1.85	nV/√Hz
	Minimum gain at 1 MHz			6.03	nV/√Hz
Noise Figure[2]	Maximum gain, R_S = 50 Ω, not terminated		7.1		dB
	Maximum gain, R_S = R_{IN} = 50 Ω		12.7		dB
Output Offset	Gain = 17 dB	−60		+60	LSB
	Gain = 35 dB	−250		+250	LSB
AAF Low-Pass Filter Cutoff	−3 dB, programmable		9.0 to 15.0		MHz
Tolerance	After filter autotune	−10	±5	+10	%
AAF Attenuation in Stop Band[2]	Third-order elliptic filter				
	2× cutoff		30		dB
	3× cutoff		40		dB
Group Delay Variation[2]	Filter set at 9 MHz		400		ns
1 dB Compression[2]	Relative to output		11.9		dBm
Saturation Flag Response Time	Time between saturation event and saturation flag going high (1 dB overdrive)		30	100	ns
	Time between end of saturation event and saturation flag going low	25	40		ns
Saturation Flag Accuracy	Gain = 29 dB				
Off	For PGA voltages below 2 V p-p		2		V p-p
On	For PGA voltages above 2.25 V p-p		2.25		V p-p
Mux[2]					
On Resistance			50		Ω
Switching Time			200		ns
POWER SUPPLY					
AVDD18x[2]		1.7	1.8	1.9	V
AVDD33x[2]		3.1	3.3	3.5	V
DVDD18x[2]		1.7	1.8	1.9	V
DVDD33x[2]		3.1	3.3	3.5	V
I_{AVDD18}	f_S = 60 MSPS			54	mA
I_{AVDD33}	f_S = 60 MSPS			65	mA
I_{DVDD18}	f_S = 60 MSPS			15	mA
I_{DVDD33}	f_S = 60 MSPS			2	mA
Total Power Dissipation	No signal, typical supply voltage × maximum supply current; excludes output current			345	mW

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
Power-Down Dissipation	$T_A = -25°C$ to $+105°C$		2.5	4.0	mW
	$T_A = -40°C$ to $+25°C$		2.5	8.0	mW
Power Supply Rejection Ratio (PSRR)[2]	Relative to input		1.6		mV/V
ADC					
Resolution[2]			12		Bits
Maximum Sample Rate			60		MSPS
Signal-to-Noise Ratio (SNR)	$f_{IN} = 1$ MHz		67		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)[2]			66		dB
SNRFS[2]			68		dB
Differential Nonlinearity (DNL)	Guaranteed no missing codes			1	LSB
Integral Nonlinearity (INL)	$f_S = 60$ MSPS		4	10	LSB
Effective Number of Bits (ENOB)[2]			10.67		LSB
ADC Output Characteristics[2]					
Maximum Capacitor Load	Per bit		20		pF
I_{DVDD33} Peak Current with Capacitor Load[2]	Peak current per bit when driving a 20 pF load; can be programmed via the SPI port, if required			40	mA
ADC REFERENCE					
Output Voltage Error	VREF = 1.000 V			±20	mV
Load Regulation	At 1.0 mA, VREF = 1.000 V		2		mV
Current Output		−1		+1	mA
Input Resistance			6		kΩ
FULL CHANNEL CHARACTERISTICS	LNA, PGA, AAF, and ADC				
SNRFS	$f_{IN} = 1$ MHz, −10 dBFS output				
	Gain = 17 dB, $f_S = 60$ MSPS	60	64		dBFS
	Gain = 23 dB, $f_S = 60$ MSPS	60	64		dBFS
	Gain = 29 dB, $f_S = 60$ MSPS	60	64		dBFS
	Gain = 35 dB, $f_S = 60$ MSPS	60	64		dBFS
SINAD[2]	$f_{IN} = 1$ MHz				
	Gain = 17 dB		62		dB
	Gain = 23 dB		63		dB
	Gain = 29 dB		64		dB
	Gain = 35 dB		63		dB
Spurious-Free Dynamic Range (SFDR)	$f_{IN} = 1$ MHz, −10 dBFS output				
	Gain = 17 dB, $f_S = 60$ MSPS	62	68		dBc
	Gain = 23 dB, $f_S = 60$ MSPS	62	68		dBc
	Gain = 29 dB, $f_S = 60$ MSPS	62	68		dBc
	Gain = 35 dB, $f_S = 60$ MSPS	62	71		dBc
Harmonic Distortion[2]	$f_{IN} = 1$ MHz at −10 dBFS output				
Second Harmonic	Gain = 17 dB		−70		dBc
	Gain = 35 dB		−70		dBc
Third Harmonic	Gain = 17 dB		−66		dBc
	Gain = 35 dB		−75		dBc
IM3 Distortion	$f_{IN1} = 1$ MHz, $f_{IN2} = 1.1$ MHz, −1 dBFS, gain = 35 dB		−69		dBc
Gain Response Time			600		ns
Overdrive Recovery Time			200		ns

[1] See the _____, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and testing methodology.
[2] Guaranteed by design only.

DIGITAL SPECIFICATIONS

$AVDD18x$ = 1.8 V, $AVDD33x$ = 3.3 V, $DVDD18x$ = 1.8 V, $DVDD33x$ = 3.3 V, 1.00 V internal ADC reference, f_{IN} = 2.5 MHz, f_S = 60 MSPS, R_S = 50 Ω, LNA + PGA gain = 35 dB, LPF cutoff = $f_{SAMPLECH}$/4, 12-bit operation, temperature = −40°C to +105°C, all specifications guaranteed by testing, unless otherwise noted.

Table 3.

| Parameter[1]	Temperature	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)[2]					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[3]	Full	250			mV p-p
Input Common-Mode Voltage	Full		1.2		V
Input Resistance (Differential)	25°C		20		kΩ
Input Capacitance	25°C		1.5		pF
LOGIC INPUTS (PDWN, SCLK, AUX, MUX[0], MUX[1], ZSEL)[2]					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT ($\overline{CS}$)[2]					
Logic 1 Voltage	Full	1.2		3.6	V
Logic 0 Voltage	Full			0.3	V
Input Resistance	25°C		70		kΩ
Input Capacitance	25°C		0.5		pF
LOGIC INPUT (SDI)[2]					
Logic 1 Voltage	Full	1.2		DVDD33x + 0.3	V
Logic 0 Voltage	Full	0		0.3	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC OUTPUT (SDO)					
Logic 1 Voltage (I_{OH} = 800 µA)	Full	3.0			V
Logic 0 Voltage (I_{OL} = 50 µA)	Full			0.3	V
LOGIC OUTPUTS (D11 to D0, SFLAG)					
Logic 1 Voltage (I_{OH} = 2 mA)	Full	3.0			V
Logic 0 Voltage (I_{OL} = 2 mA)	Full			0.3	V

[1] See the _____, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and testing methodology.
[2] Guaranteed by design only.
[3] Specified for LVDS and LVPECL only.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 3. Pin Configuration
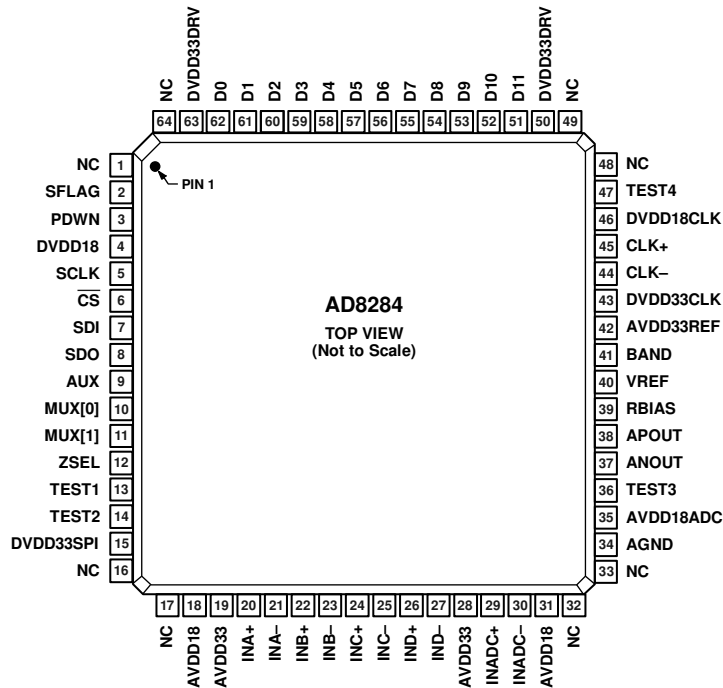
NOTES
1. TIE THE EXPOSED PAD ON THE BOTTOM SIDE TO THE ANALOG GROUND PLANE.
2. NC = NO CONNECTION. TIE NC TO ANY POTENTIAL.

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connection. Tie NC to any potential.
2	SFLAG	Saturation Flag.
3	PDWN	Full Power-Down. A logic high on PDWN overrides the SPI and powers down the part; a logic low allows selection through the SPI.
4	DVDD18	1.8 V Digital Supply.
5	SCLK	Serial Clock.
6	$\overline{CS}$	Chip Select.
7	SDI	Serial Data Input.
8	SDO	Serial Data Output.
9	AUX	Auxiliary Channel. A logic high on AUX switches the AUX channel to ADC (INADC+/INADC−).
10	MUX[0]	Digital Control for Mux Channel Selection.
11	MUX[1]	Digital Control for Mux Channel Selection.
12	ZSEL	Input Impedance Select. A logic high on ZSEL overrides the SPI and sets the input impedance to 200 kΩ; a logic low allows selection through the SPI.
13	TEST1	Test. Do not use the TEST1 pin; tie TEST1 to ground.
14	TEST2	Test. Do not use the TEST2 pin; tie TEST2 to ground.
15	DVDD33SPI	3.3 V Digital Supply, SPI Port.
16	NC	No Connection. Tie NC to any potential.
17	NC	No Connection. Tie NC to any potential.
18	AVDD18	1.8 V Analog Supply.
19	AVDD33	3.3 V Analog Supply.
20	INA+	Positive Mux Analog Input for Channel A.
21	INA−	Negative Mux Analog Input for Channel A.
22	INB+	Positive Mux Analog Input for Channel B.
23	INB−	Negative Mux Analog Input for Channel B.

| Pin No.	Mnemonic	Description
24	INC+	Positive Mux Analog Input for Channel C.
25	INC−	Negative Mux Analog Input for Channel C.
26	IND+	Positive Mux Analog Input for Channel D.
27	IND−	Negative Mux Analog Input for Channel D.
28	AVDD33	3.3 V Analog Supply.
29	INADC+	Positive Analog Input for Alternate Channel (ADC Only).
30	INADC−	Negative Analog Input for Alternate Channel (ADC Only).
31	AVDD18	1.8 V Analog Supply.
32	NC	No Connection. Tie NC to any potential.
33	NC	No Connection. Tie NC to any potential.
34	AGND	Ground.
35	AVDD18ADC	1.8 V Analog Supply.
36	TEST3	Test. Do not use the TEST3 pin; tie TEST3 to ground.
37	ANOUT	Analog Output. ANOUT is for debug purposes only. Leave ANOUT floating.
38	APOUT	Analog Output. APOUT is for debug purposes only. Leave APOUT floating.
39	RBIAS	External Resistor. The RBIAS pin sets the internal ADC core bias current.
40	VREF	Voltage Reference Input/Output.
41	BAND	Band Gap Voltage. BAND is for debug purposes only. Leave BAND floating.
42	AVDD33REF	3.3 V Analog Supply.
43	DVDD33CLK	3.3 V Digital Supply.
44	CLK−	Clock Input Complement.
45	CLK+	Clock Input True.
46	DVDD18CLK	1.8 V Digital Supply.
47	TEST4	Test. Do not use the TEST4 pin; tie TEST4 to ground.
48	NC	No Connection. Tie NC to any potential.
49	NC	No Connection. Tie NC to any potential.
50	DVDD33DRV	3.3 V Digital Supply.
51	D11	ADC Data Output (MSB).
52	D10	ADC Data Output.
53	D9	ADC Data Output.
54	D8	ADC Data Output.
55	D7	ADC Data Output.
56	D6	ADC Data Output.
57	D5	ADC Data Output.
58	D4	ADC Data Output.
59	D3	ADC Data Output.
60	D2	ADC Data Output.
61	D1	ADC Data Output.
62	D0	ADC Data Output (LSB).
63	DVDD33DRV	3.3 V Digital Supply.
64	NC	No Connection. Tie NC to any potential.
	EP	Exposed Pad. Tie the exposed pad on the bottom side to the analog ground plane.
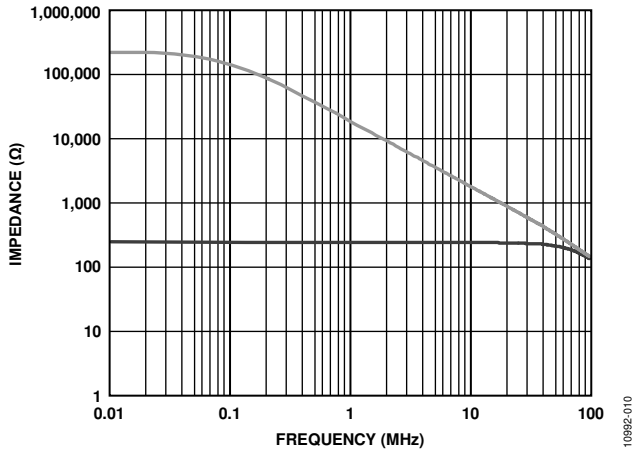
Figure 10. R_{IN} vs. Frequency
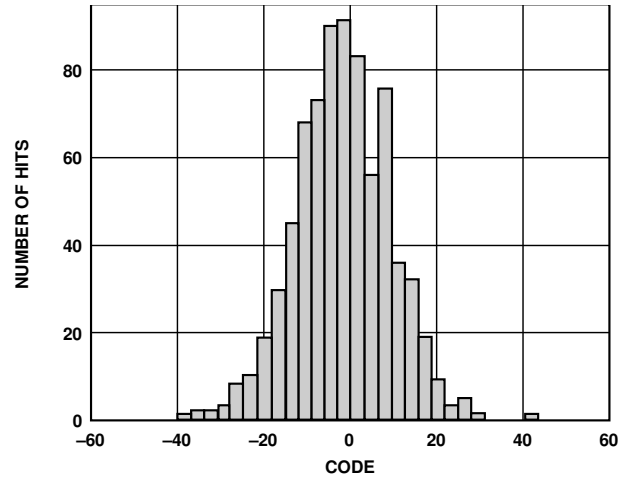

Figure 12. Channel Offset Distribution (Gain = 17 dB)
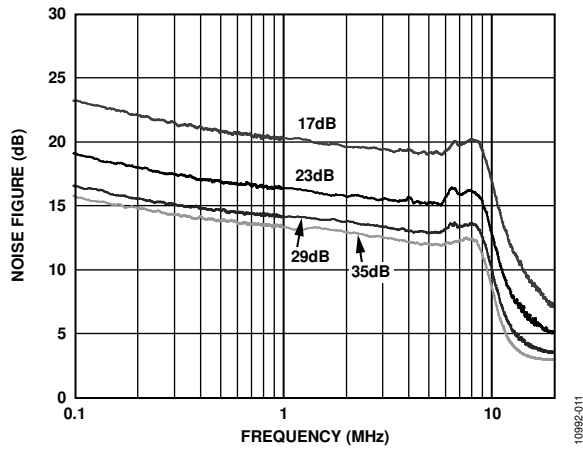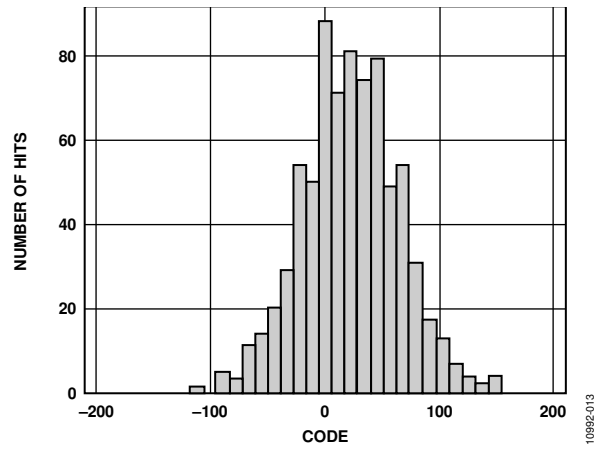

Figure 11. Noise Figure vs. Frequency

Figure 13. Channel Offset Distribution (Gain = 35 dB)

THEORY OF OPERATION

RADAR RECEIVE PATH AFE

The primary application for the   is high speed ramp, frequency modulated, continuous wave (HSR-FMCW) radar requiring baseband signal bandwidths of up to 15 MHz. Figure 14 shows a simplified block diagram of an HSR-FMCW radar system.

The signal chain requires multiple channels, each of which is routed into a low noise amplifier (LNA), a programmable gain amplifier (PGA), an antialiasing filter (AAF), and an analog-to-digital converter (ADC). The   provides all of these key components in a single 10 mm × 10 mm TQFP package.

The performance of each component is designed to meet the demands of an HSR-FMCW radar system. Some examples of these performance metrics include the LNA noise, PGA gain range, AAF cutoff characteristics, and ADC sample rate and resolution.

The   includes a multiplexer (mux) in front of the analog signal chain as a cost-saving alternative to having an AFE for each channel. The mux can be switched between active inputs using the mux pins or through the SPI port.

The   also includes a saturation detection circuit that indicates when the LNA or PGA signals are no longer in the linear region. This feature helps detect fault conditions that might otherwise be filtered out by the AAF.
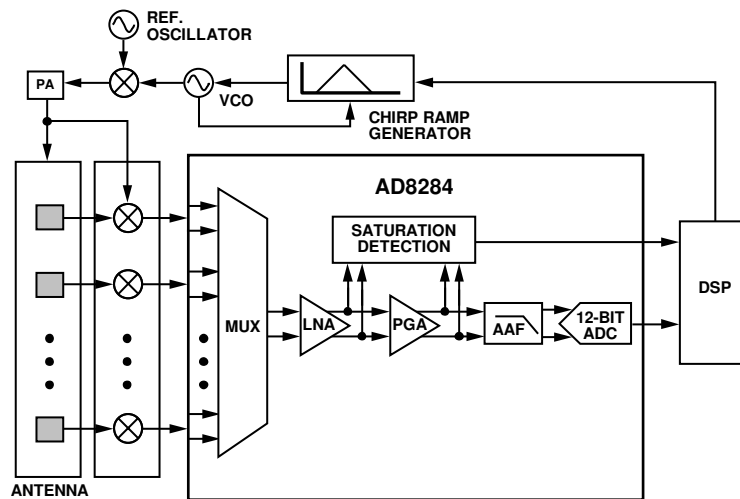

Figure 14. Simplified Block Diagram, HSR-FMCW Radar System

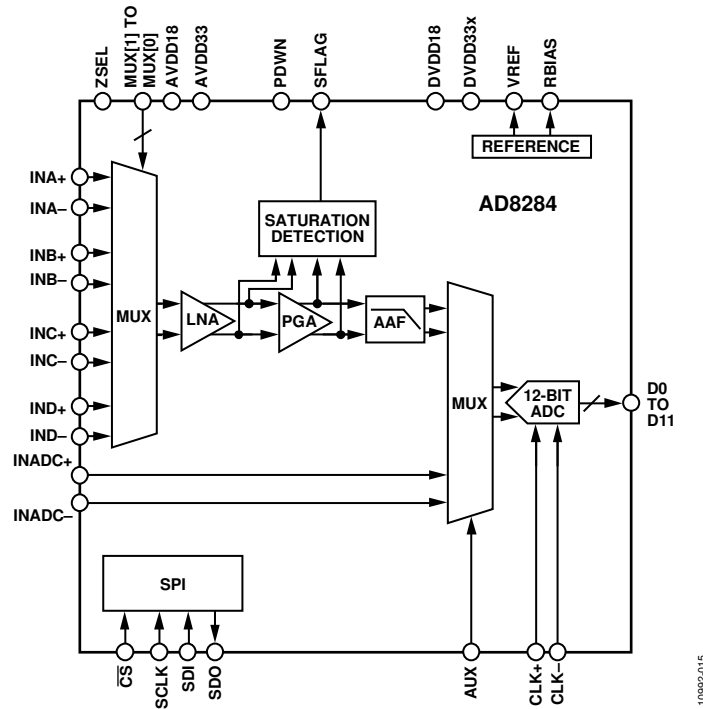Figure 15. Simplified Block Diagram

CHANNEL OVERVIEW

The   contains a four-input mux, an LNA, a PGA, and
an AAF in the signal path, as shown in Figure 15. The signal
chain input impedance can be either 200 Ω or 200 kΩ. The
PGA has selectable gains that result in channel gains ranging
from 17 dB to 35 dB. The AAF has a three-pole elliptical
response with a selectable cutoff frequency from 9 MHz to
15 MHz. The signal path is fully differential throughout to
maximize signal swing and reduce even-order distortion. The
LNA is designed to be driven from either a differential or
single-ended signal source.

Multiplexer

The   has a multiplexer (mux) at the input to switch as
many as four differential channels into the signal chain. The
active mux channel is controlled by the SPI port or by using the
external pins, MUX[0] and MUX[1]. The relationship between
the input code and the selected mux channel is listed in Table 7.

Table 7. Digital Input Values to Select the Active ADC
Channel

AUX	MUX[1]	MUX[0]	Active Channel
1	X	X	AUX
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

The external pins are the default method for selecting the active
mux channel but the SPI Register 0x0C can also control the
mux. Bit 3 of Register 0x0C specifies whether the SPI or the
external pins control the mux.

Low Noise Amplifier

Good noise performance relies on a proprietary ultralow noise
LNA at the beginning of the signal chain; the LNA minimizes the
noise contributions from the PGA and AAF that are next in the
signal chain. The input impedance can be either 200 Ω or
200 kΩ, the value of which is selected through the SPI port or by
the ZSEL pin.

The LNA supports differential output voltages as high as 5.0 V p-p
with positive and negative excursions of ±1.25 V from a common-
mode voltage of 1.5 V. Because the output saturation level is
fixed, the channel gain sets the maximum input signal before
saturation.

Low value feedback resistors and the current driving capability
of the output stage allow the LNA to achieve a low input referred
noise voltage of 3.5 nV/√Hz at a channel gain of 35 dB. The use
of a fully differential topology and negative feedback minimizes
second-order distortion. Differential signaling enables smaller
swings at each output, further reducing third-order distortion.

Recommendation

To achieve the best possible noise performance, it is important
to match the impedances seen by the positive and negative
inputs. Matching the impedances ensures that the signal path
rejects any common-mode noise.

Antialiasing Filter

The AAF uses a combination of poles and zeros to create a third-order elliptic filter. An elliptic filter is used to achieve a sharp roll-off after the cutoff frequency. This architecture achieves a −30 dB per octave roll-off in the first octave after the cutoff frequency.

The filter uses on-chip tuning to trim the internal resistors and capacitors to set the desired cutoff frequency. The tuning method reduces variations in the cutoff frequency due to standard IC process tolerances of resistors and capacitors.

The default tuning settings for a −3 dB low-pass filter cutoff is $1/3 \times 1.125 \times$ the ADC sample clock frequency. This setting can be changed to 1/4 the ADC sample clock frequency. The cutoff can also be scaled from 0.75 to 1.25 (in 0.0625 increments) times these frequencies through the SPI.

Tuning is normally off and is initiated by the user via the SPI port. After the filter is tuned to a specific frequency, it remains at that frequency until another tuning sequence is initiated. The tuning process can take up to 2048 clock cycles.

The filter defaults to its highest frequency setting before it is tuned. To maintain the expected ratio of clock frequency to cutoff frequency, tune the filter after initial power-up, after reprogramming the filter cutoff scaling via the SPI, or after changing the ADC sample rate. Occasional retuning during an idle time is recommended to compensate for temperature drift.

A cutoff frequency range of 9 MHz to 15 MHz is possible, for example

- ADC clock: 40 MHz
- Default tuned cutoff frequency = $(40\text{ MHz} \div 3) \times 1.125 =$ 15 MHz

The autotune cycle takes several clock cycles to complete. During this time, the mux channels, A to D, are not operational; however, the AUX input can be used during the autotuning cycle.

Saturation Flag

The saturation flag function detects overvoltage conditions that may push the LNA or PGA out of their linear regions. The flag is set when the PGA output voltage exceeds 2.0 V p-p or the LNA output voltage exceeds 4.0 V p-p. This function is particularly useful for detecting saturation events that may be filtered out by the AAF and are, therefore, undetectable by monitoring the ADC output.

When the saturation flag trips, it remains on for a minimum of 25 ns after the saturation event has ended.
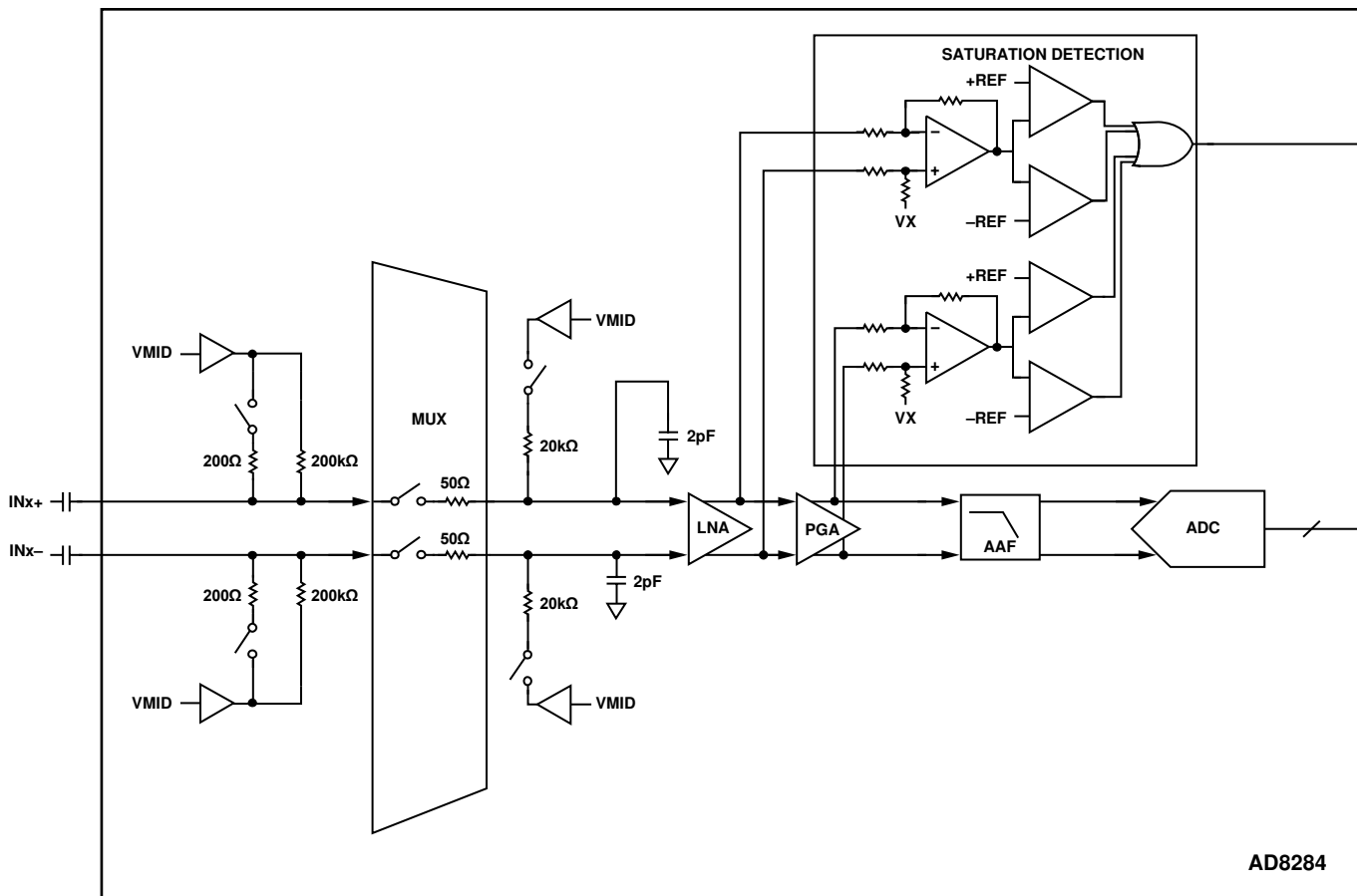

Figure 16. Simplified Block Diagram of the Analog Channel

ADC

The uses a pipelined ADC architecture. The quantized output from each stage is combined into a 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock. The output staging block aligns the data and passes the data to the output buffers.

AUX CHANNEL

The allows direct access to the ADC when the mux settings are used to select the AUX channel. When this channel is selected, the inputs of the ADC can be accessed using the INADC+ and INADC− pins. To ensure enough headroom for full-scale, differential, 2.0 V p-p input signals, bias the INADC± pins with a 0.9 V common-mode voltage.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or by using capacitors; these pins are biased internally and require no additional bias.

Figure 17 shows the preferred method for clocking the . A low jitter clock source, such as the Valpey Fisher oscillator, VFAC3-BHL (50 MHz), is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.
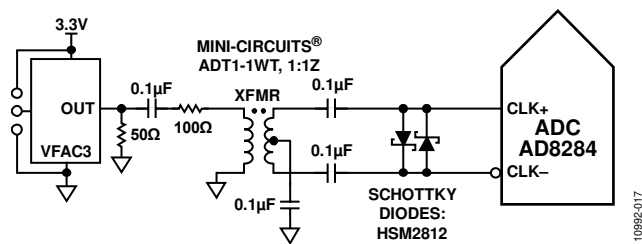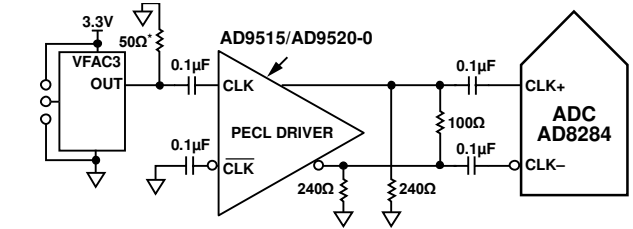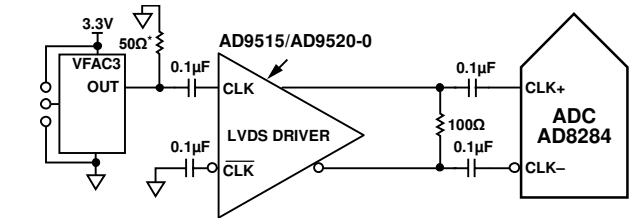
Figure 17. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac-couple a differential PECL or LVDS signal to the sample clock input pins as shown in Figure 18 and Figure 19. The / family of clock drivers offers excellent jitter performance.

*Figure 18. Differential PECL Sample Clock*

Figure 19. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, drive CLK+ directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 μF capacitor in parallel with a 39 kΩ resistor (see Figure 20). Although the CLK+ input circuit supply is via Pin 46, DVDD18CLK, this input is designed to withstand input voltages of up to 3.3 V, making the selection of the logic voltage of the driver very flexible. The / family of parts can be used to provide 3.3 V inputs (see Figure 21). In this case, the 39 kΩ resistor is not needed.
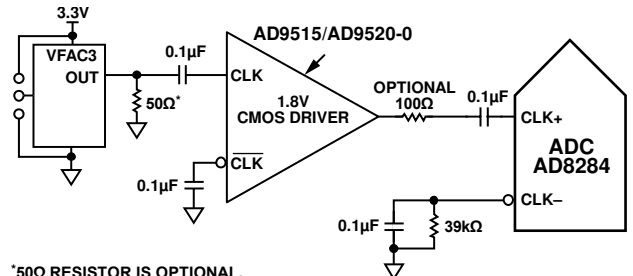
Figure 20. Single-Ended 1.8 V CMOS Sample Clock
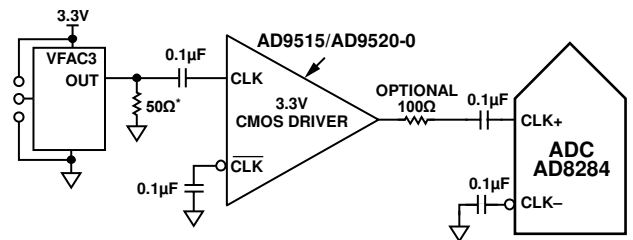
Figure 21. Single-Ended 3.3 V CMOS Sample Clock

AD8284

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the device be connected to a quiet analog ground to achieve the best electrical and thermal performance of the   . Mate an exposed continuous copper plane on the PCB to the exposed pad, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB.

To maximize the coverage and adhesion between the device and the PCB, it is recommended that the continuous copper pad be partitioned by overlaying a silkscreen or solder mask to divide the copper pad into uniform sections. This partitioning helps to ensure several tie points between the PCB and the device during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the   and the PCB. For more information about packaging and for additional PCB layout examples, see the   .

SERIAL PORT INTERFACE (SPI)

The   serial port interface allows the user to configure the signal chain for specific functions or operations through a structured register space provided inside the chip. The SPI offers the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, as documented in the Memory Map section. Detailed operational information can be found in the   , *Interfacing to High Speed ADCs via SPI.*

Four pins define the serial port interface, or SPI: the SCLK, SDI, SDO, and $\overline{CS}$ pins. The serial clock pin (SCLK) synchronizes the read and write data presented to the device. The serial data input and output pins, SDI and SDO, allow data to be sent to and read from the internal memory map registers of the device. The chip select pin ($\overline{CS}$) is an active low control that enables or disables the read and write cycles (see Table 8).

Table 8. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDI	Serial data input.
SDO	Serial data output.
$\overline{CS}$	Chip select (active low). This control gates the read and write cycles.

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing sequence. During an instruction phase, a 16-bit instruction is transmitted, followed by one or more data bytes, which is determined by Bit Field W0 and Bit Field W1. See Figure 22 and Table 9 for an example of the serial timing and its definitions.

In normal operation, $\overline{CS}$ signals to the device that SPI commands are about to be received and processed. When $\overline{CS}$ is brought low, the device processes SCLK and SDI to process instructions. Normally, $\overline{CS}$ remains low until the communication cycle is complete. However, if the AD8284 is connected to a slow device, $\overline{CS}$ can be brought high between bytes, allowing older microcontrollers enough time to transfer data into the shift registers. $\overline{CS}$ can be stalled when transferring one, two, or three bytes of data.

When W0 and W1 are set to 11, the device enters streaming mode and continues to process data, either reading or writing, until $\overline{CS}$ is taken high to end the communication cycle. This allows complete memory transfers without the need to provide additional instructions. Regardless of the mode, if $\overline{CS}$ is taken high in the middle of any byte transfer, the SPI state machine is reset and the device waits for a new instruction.

In addition to the operation modes, the SPI port can be configured to operate in different manners. For applications that do not require a control port, the $\overline{CS}$ line can be tied and held high. This places the remainder of the SPI pins in their secondary mode as defined in the   , *Interfacing to High Speed ADCs via SPI.* $\overline{CS}$ can also be tied low to enable 3-wire mode. When $\overline{CS}$ is tied low, SCLK, SDO, and SDI are the only pins required for communication. Although the device is synchronized during power-up, caution must be exercised when using this mode to ensure that the serial port remains synchronized with the $\overline{CS}$ line. When operating in 3-wire mode, it is recommended that a 1-, 2-, or 3-byte transfer be used exclusively. Without an active $\overline{CS}$ line, streaming mode can be entered but not exited.

Data can be sent in MSB-first or LSB-first mode. MSB-first mode is the default at power-up and can be changed by adjusting the configuration register. For more information about this and other features, see the   , *Interfacing to High Speed ADCs via SPI.*

HARDWARE INTERFACE

The pins described in Table 8 constitute the physical interface between the user's programming device and the serial port of the   . The SCLK, SDI, and $\overline{CS}$ pins function as inputs when using the SPI interface. The SDO pin is an output during readback.

This interface is flexible enough to be controlled by either serial-programmable read-only memory (PROM) or PIC micro-controllers. This provides the user with alternative means, other than a full SPI controller, for programming the device (see the   ).

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: the chip configuration registers map (Address 0x00 and Address 0x01), the device index and transfer registers map (Address 0x04 to Address 0xFF), and the ADC channel functions registers map (Address 0x08 to Address 0x2C).

The leftmost column of the memory map indicates the register address number, and the default value is shown in the second rightmost column.

The Bit 7 (MSB) column is the start of the default hexadecimal value that is given. For example, Address 0x09, the GLOBAL_CLOCK register, has a default value of 0x01, meaning that Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. This setting is the default for the duty cycle stabilizer in the on condition. By writing a 0 to Bit 0 of this address followed by writing 0x01 to the SW transfer bit in Register 0xFF, the duty cycle stabilizer is turned off. It is important to follow each writing sequence with a write to the SW transfer bit to update the SPI registers.

Caution

All registers except for Register 0x00 and Register 0xFF are buffered with a master slave latch and require writing to the transfer bit. For more information about this and other functions, see the   , *Interfacing to High Speed ADCs via SPI.*

LOGIC LEVELS

An explanation of various registers follows: "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly, "bit is cleared" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit.

RESERVED LOCATIONS

Do not write to undefined memory except when writing the default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

DEFAULT VALUES

After a reset, critical registers are automatically loaded with default values. These values are indicated in Table 10, where an X refers to an undefined feature.

Table 10. Memory Map Registers[1]

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Default Notes/ Comments
Chip Configuration Registers											
0x00	CHIP_PORT_CONFIG	0	LSB first 1 = on 0 = off (default)	Soft reset 1 = on 0 = off (default)	1	1	Soft reset 1 = on 0 = off (default)	LSB first 1 = on 0 = off (default)	0	0x18	Mirror the nibbles to correctly set LSB-first or MSB-first mode, regardless of shift mode.
0x01	CHIP_ID				Chip ID Bits[7:0] (= 0xAA, default)					Read only	The default is a unique chip ID, specific to the . This is a read-only register.
Device Index and Transfer Registers											
0xFF	DEVICE_UPDATE	X	X	X	X	X	X	X	SW transfer 1 = on 0 = off (default)	0x00	Synchronously transfers data from the master shift register to the slave.
Channel Functions Registers											
0x08	GLOBAL_MODES	Channel A buffer power 0 = power off 1 = power on (default)	Channel B buffer power 0 = power off 1 = power on (default)	Channel C buffer power 0 = power off 1 = power on (default)	Channel D buffer power 0 = power off 1 = power on (default)	Channel power-down 0 = power on (default) 1 = power off	X	Internal power-down mode 00 = chip run (default) 01 = full power-down 11 = reset		0xF0	Determines the power-down mode (global).
0x09	GLOBAL_CLOCK	X	X	X	X	X	X	X	Duty cycle stabilizer 1 = on (default) 0 = off	0x01	Turns the internal duty cycle stabilizer on and off (global).
0x0C	FLEX_MUX_CONTROL	X	Power down unused channels 0 = PD power-down (default) 1 = power on	X	0 = signal channel (A, B, C, D) on (default) 1 = AUX channel on	0 = use external pins (default) 1 = use internal registers	0 = all channels are off 1 = selected channel is on (default)	00 = Channel A (default) 01 = Channel B 10 = Channel C 11 = Channel D		0x04	Sets which mux input channel is in use and whether to power down unused channels.
0x0D	FLEX_TEST_IO	User test mode 00 = off (default) 01 = on, single alternate 10 = on, single once 11 = on, alternate once		Reset PN long gen 1 = on 0 = off (default)	Reset PN short gen 1 = on 0 = off (default)	Output test mode—see Table 11 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = −FS short 0100 = checkerboard output 0101 = PN sequence long 0110 = PN sequence short 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-bit/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency (format determined by the OUTPUT_MODE register)				0x00	When this register is set, the test data is placed on the output pins in place of normal data. (Local, except for PN sequence.)

Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Default Notes/ Comments
0x0E	TEST_REGISTER	Enable analog outputs (APOUT, ANOUT) 0x01 = analog output enabled									0x00	Routes the differential output of the AAF to APOUT and ANOUT.
0x0F	FLEX_CHANNEL_INPUT	Filter cutoff frequency control 00000 = 1.25 × 1/4 × $f_{SAMPLECH}$ 00001 = 1.1875 × 1/4 × $f_{SAMPLECH}$ 00010 = 1.125 × 1/4 × $f_{SAMPLECH}$ 00011 = 1.0625 × 1/4 × $f_{SAMPLECH}$ 00100 = 1.0 × 1/4 × $f_{SAMPLECH}$ 00101 = 0.9375 × 1/4 × $f_{SAMPLECH}$ 00110 = 0.875 × 1/4 × $f_{SAMPLECH}$ 00111 = 0.8125 × 1/4 × $f_{SAMPLECH}$ 01000 = 0.75 × 1/4 × $f_{SAMPLECH}$ 01001 to 01111 = reserved 10000 = 1.25 × 1/3 × $f_{SAMPLECH}$ 10001 = 1.1875 × 1/3 × $f_{SAMPLECH}$ 10010 = 1.125 × 1/3 × $f_{SAMPLECH}$ (default) 10011 = 1.0625 × 1/3 × $f_{SAMPLECH}$ 10100 = 1.0 × 1/3 × $f_{SAMPLECH}$ 10101 = 0.9375 × 1/3 × $f_{SAMPLECH}$ 10110 = 0.875 × 1/3 × $f_{SAMPLECH}$ 10111 = 0.8125 × 1/3 × $f_{SAMPLECH}$ 11000 = 0.75 × 1/3 × $f_{SAMPLECH}$ 11001 to 11111 = reserved						X	X	X	0x90	Low-pass filter cutoff (global). $f_{SAMPLECH}$ = ADC sample rate. Note that the absolute range is limited to 9 MHz to 15 MHz.
0x10	FLEX_OFFSET	X	X	6-bit LNA offset adjustment 00 0000 for LNA offset low 10 0000 for LNA offset mid (default) 11 1111 for LNA offset high						0x20	LNA force offset correction.
0x11	FLEX_GAIN_1	X	X	X	X	X	000 = 17 dB 001 = 17 dB 010 = 17 dB 011 = 23 dB 100 = 29 dB (default) 101 = 35 dB			0x04	Total LNA + PGA gain adjustment (local).
0x12	FLEX_BIAS_CURRENT	X	X	X	X	X	X	LNA bias 00 = high (default) 01 = mid to high 10 = mid to low 11 = low		0x00	LNA bias current adjustment (global).
0x14	FLEX_OUTPUT_MODE	X	X	X	X	X	1 = output invert (local)	0 = offset binary 1 = twos comple-ment (default)		0x01	Configures the outputs and the format of the data.
0x15	FLEX_OUTPUT_ADJUST	0 = enable Data Bits[11:0] 1 = disable Data Bits[11:0]	X	X	X	Output drive current 0000 = low … 1111 = high (default)				0x0F	Selects output drive strength to limit the noise added to the channels by output switching.
0x18	FLEX_VREF	X	0 = internal reference (default) 1 = external reference	X	X	X	X	Internal reference adjust 00 = 0.625 V 01 = 0.750 V 10 = 0.875 V 11 = 1.000 V (default)		0x03	Select internal reference (recommended default) or external reference (global); adjust internal refer-ence.
0x19	FLEX_USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User defined Pattern 1, LSB.
0x1A	FLEX_USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User defined Pattern 1, MSB.

| Addr. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Default Notes/ Comments
0x1B	FLEX_USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User defined Pattern 2, LSB.
0x1C	FLEX_USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User defined Pattern 2, MSB.
0x2B	FLEX_FILTER	X	Enable automatic low-pass tuning 1 = on (self clearing)	X	X	X	X	X	X	0x00	Enables low-pass filter tuning
0x2C	CH_IN_IMP	Saturation detector limit adjust 000 = 1.90 V p-p at PGA output 011 = 2.00 V p-p at PGA output (default) 111 = 2.15 V p-p at PGA output Other values reserved (001, 010, 100, 101, 110)			Saturation detect hysteresis 0 = low hysteresis (25 mV nominal at PGA output) (default) 1 = high hysteresis (nominally 60 mV at PGA output)	X	X	X	Input impedance 0 = 200 Ω 1 = 200 kΩ (default)	0x61	Saturation detector adjustment and input impedance adjustment (global).

[1] X = undefined feature.

Table 11. Flexible Output Test Modes[1]

| Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	1000 0000 0000	Same	Yes
0010	+Full-scale short	1111 1111 1111	Same	Yes
0011	−Full-scale short	0000 0000 0000	Same	Yes
0100	Checkerboard output	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long	N/A	N/A	Yes
0110	PN sequence short	N/A	N/A	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No
1001	1-bit/0-bit toggle	1010 1010 1010	N/A	No
1010	1× sync	0000 0011 1111	N/A	No
1011	One bit high	1000 0000 0000	N/A	No
1100	Mixed bit frequency	1010 0011 0011	N/A	No

[1] N/A means not applicable.

APPLICATION CIRCUITS
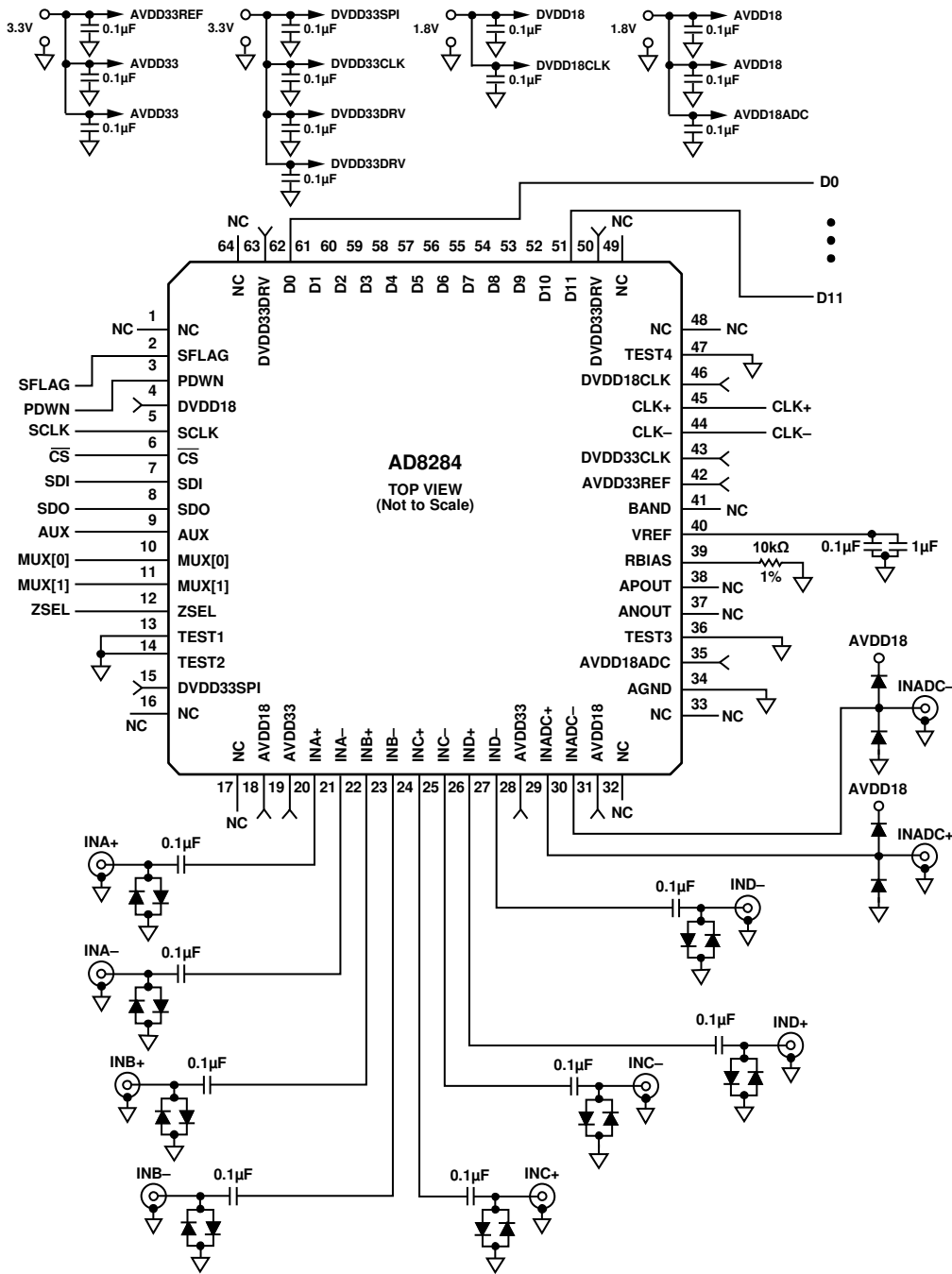
NOTES
1. ALL CAPACITORS FOR SUPPLIES AND REFERENCES SHOULD BE PLACED CLOSE TO THE PART.
2. TIE THE EXPOSED PAD ON THE BOTTOM SIDE TO THE ANALOG GROUND PLANE.

Figure 23. Differential Inputs
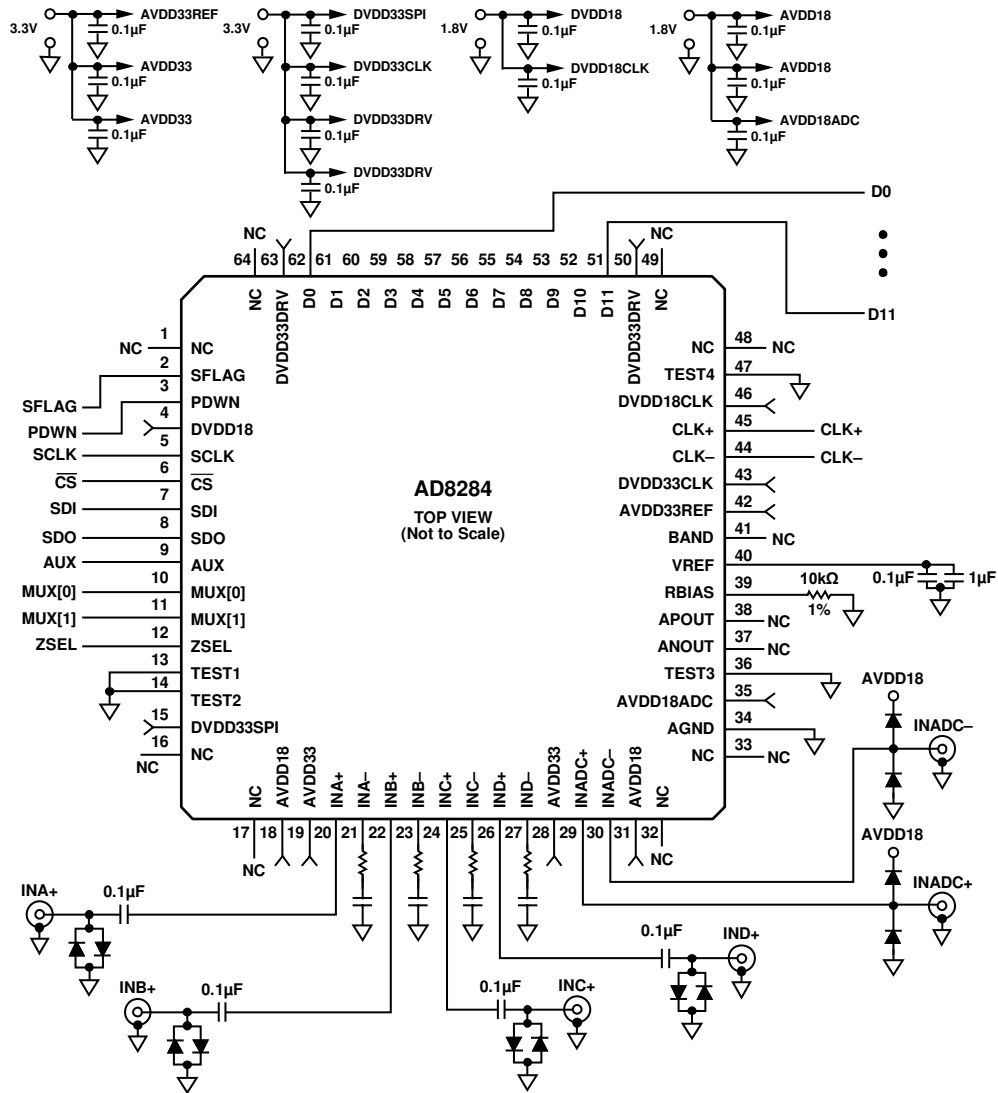
NOTES
1. RESISTOR R (INX– INPUTS) SHOULD MATCH THE OUTPUT IMPEDANCE OF THE INPUT DRIVER.
2. ALL CAPACITORS FOR SUPPLIES AND REFERENCES SHOULD BE PLACED CLOSE TO THE PART.
3. TIE THE EXPOSED PAD ON THE BOTTOM SIDE TO THE ANALOG GROUND PLANE.

Figure 24. Single-Ended Inputs

NOTES

NOTES

ANALOG DEVICES

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