10-Bit, 200-MSPS, 4-Channel and 12-Bit, 80-MSPS, 8-Channel Analog-to-Digital Converter

Check for Samples: ADS5296A

FEATURES

- **Configurable Modes of Operation:**
  - **10-Bit, 200-MSPS, 4-Channel ADC**
  - **12-Bit, 160-MSPS, 4-Channel ADC**
  - **10-Bit, 100-MSPS, 8-Channel ADC**
  - **12-Bit, 80-MSPS, 8-Channel ADC**
- **Designed for Low Power:**
  - **65 mW per Channel at 80 MSPS (12-Bit, 8-Channel)**
  - **150 mW per Channel at 200 MSPS (10-Bit, 4-Channel)**
- **12-Bit, 80 MSPS:**
  - **SNR: 70.3 dBFS**
- **10-Bit, 200 MSPS:**
  - **SNR: 61.3 dBFS**
  - **Interleaving Spur: > 60 dBc at 90 MHz**
- **Serial LVDS One-Wire Interface:**
  - **10x Serialization up to 1000 Mbps Data Rate per Wire**
  - **12x Serialization up to 960 Mbps Data Rate per Wire**
- **Digital Processing Block:**
  - **Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference**
  - **Programmable IIR High-Pass Filter to Minimize DC Offset**
  - **Programmable Digital Gain: 0 dB to 12 dB**
- **Low-Frequency Noise Suppression Mode**
- **Programmable Mapping Between ADC Input Channels and LVDS Output Pins**
- **Channel Averaging Mode**
- **Variety of LVDS Test Patterns to Verify Data Capture by FPGA or Receiver**
- **Package: 9-mm × 9-mm QFN-64**

APPLICATIONS

- **Ultrasound Imaging**
- **Communication Applications**
- **Multichannel Data Acquisition**

DESCRIPTION

The ADS5296A is a low-power, 12-bit, 8-channel, analog-to-digital converter (ADC) with sample rates up to 80 MSPS. However, the device can also be configured to operate as a 4-channel ADC running at 2x the sample rate by interleaving data from two ADC channels. In interleaving mode, the device accepts a double frequency input clock. Each ADC in a pair converts a common analog input signal at alternate rising edges of the 2x input clock. The device can either be configured as a 10-bit, 4-channel ADC with sample rates up to 200 MSPS or as a 12-bit, 4-channel ADC with sample rates up to 160 MSPS.

The data from each ADC within the interleaved pair is output in serial format over one LVDS pair up to a maximum data rate of 1 Gbps (10 bits at 100 MSPS). With interleaving disabled, the ADS5296A can also be operated as an 8-channel, 10-bit device with sample rates up to 100 MSPS.

Several digital functions commonly used in systems are included in the device. These functions include a low-frequency noise suppression (LFNS) mode, digital filtering options, and programmable mapping of LVDS output pins and analog input channels.

For low input frequency applications, the LFNS mode enables the suppression of noise at low frequencies and improves SNR in the 1-MHz band near dc by approximately 3 dB. Digital filtering options include low-pass, high-pass, and band-pass digital filters as well as dc offset removal filters.

Low power consumption and integration of multiple channels in a small package makes the device attractive for high channel count data acquisition systems. The device is available in a compact 9-mm × 9-mm QFN-64 package. The ADS5296A is specified over the –40°C to +85°C operating temperature range.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE
ADS5296A	QFN-64	RGC	–40°C to +85°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		VALUE	UNIT
Supply voltage range	AVDD	–0.3 to 2.2	V
	LVDD	–0.3 to 2.2	V
Voltage between:	AGND and LGND	–0.3 to 0.3	V
	AVDD to LVDD (when AVDD leads LVDD)	0 to 2.2	V
	LVDD to AVDD (when LVDD leads AVDD)	0 to 2.2	V
Voltage applied to:	IN_p, IN_n	–0.3 to min (2.2, AVDD + 0.3)	V
	$\overline{\text{RESET}}$, SCLK, SDATA, $\overline{\text{CS}}$, PD, SYNC	–0.3 to 3.6	V
	CLKP, CLKN(2)	–0.3 to min (2.2, AVDD + 0.3)	V
	Digital outputs	–0.3 to min (2.2, LVDD + 0.3)	V
Temperature range	Operating free-air, T_A	–40 to +85	°C
	Operating junction, T_J	+105	°C
	Storage, T_{stg}	–55 to +150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM)	2000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP and CLKN is less than |0.3 V|. This setting prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS5296 QFN (RGC) 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	22.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	6.9	
θ_{JB}	Junction-to-board thermal resistance	2.4	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
LVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			VCM ± 0.05		V
REFT	External reference mode, top			1.45		V
REFB	External reference mode, bottom			0.45		V
VCM	Common-mode voltage output			0.95		V
CLOCK INPUT						
	Input clock frequency (1 / t_C)	4-channel, 10-bit ADC with interleaving	20		200	MSPS
		4-channel, 12-bit ADC with interleaving	20		160	MSPS
		8-channel, 10-bit ADC without interleaving	10		100	MSPS
		8-channel,12-bit ADC without interleaving	10		80	MSPS
	Input clock amplitude differential (VCLKP – VCLKN)	Sine-wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled	0.2	1.6		V_{PP}
		LVDS, ac-coupled	0.2	0.7		V_{PP}
	Input clock CMOS single-ended (VCLKP)	V_{IL} with < 0.1-mA current sink		< 0.3		V
		V_{IH}		> 1.5		V
	Input clock duty cycle		35	50	65	%
DIGITAL OUTPUTS						
	ADCLKP and ADCLKN outputs (LVDS)			1x (sample rate in MSPS)		MHz
	LCLKP and LCLKN outputs (LVDS)			6x or 5x (sample rate in MSPS)		MHz
	Output data rate	12x serialization			960	Mbps
		10x serialization			1000	Mbps

ELECTRICAL CHARACTERISTICS: General

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.
Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.8 V.

PARAMETER			TEST CONDITIONS	8-CHANNEL, 12-BIT (Non-Interleaving)			4-CHANNEL, 10-BIT (Interleaving)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION										
	Resolution					12			10	Bits
ANALOG INPUTS										
	Differential input voltage range (0-dB gain)				2.0			2.0		V_{PP}
	Differential input resistance		At dc		> 1			> 1		kΩ
	Differential input capacitance		At dc		2.2			2.2		pF
	Analog input bandwidth				> 500			> 500		MHz
	Analog input common-mode current (per input pin)				1			1		µA/MSPS
VCM	Common-mode output voltage				0.95			0.95		V
	VCM output current capability				5			5		mA
DYNAMIC ACCURACY										
E_O	Offset error			–20		20	–20		20	mV
E_{GREF}	Gain error	Resulting from internal reference inaccuracy alone		–1.5		1.5	–1.5		1.5	%FS
E_{GCHAN}		Of channel itself			0.5			0.5		%FS
	E_{GCHAN} temperature coefficient				< 0.01			< 0.01		Δ%FS/°C
POWER SUPPLY										
IAVDD	Analog supply current		80 MSPS, non-interleaving		176					mA
			200 MSPS, interleaving					207	227	mA
ILVDD	Output buffer supply current		80 MSPS with 100-Ω external termination		111					mA
			200 MSPS with 100-Ω external termination					125	148	mA
AVDD	Analog power		80 MSPS, non-interleaving		317					mW
			200 MSPS, interleaving					372	408.6	mW
LVDD	Digital power		80 MSPS with 100-Ω external termination		199					mW
			200 MSPS with 100-Ω external termination					225	266.4	mW
	Total power		80 MSPS with 100-Ω external termination		516					mW
			200 MSPS with 100-Ω external termination					597	675	mW
	Global power-down					40			40	mW
	Standby power				175			190		mW

ELECTRICAL CHARACTERISTICS: Dynamic Performance

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, maximum rated input clock frequency, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.
Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		8-CHANNEL, 12-BIT (Non-Interleaving)			4-CHANNEL, 10-BIT (Interleaving)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (1)	f_{IN} = 5 MHz		66	70.3		59.9	61.3		dBFS
		f_{IN} = 30 MHz			70.1			61		dBFS
		f_{IN} = 90 MHz			68.7			60.3		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 5 MHz			70.1			61.3		dBFS
		f_{IN} = 30 MHz			69.7			60.8		dBFS
		f_{IN} = 90 MHz			67.9			59.8		dBFS
ENOB	Effective number of bits	f_{IN} = 5 MHz			11.3			9.8		LSBs
SFDR	Spurious-free dynamic range (1)	f_{IN} = 5 MHz		73	83		70.5	83		dBc
		f_{IN} = 30 MHz			80			79		dBc
		f_{IN} = 90 MHz			76			72.5		dBc
THD	Total harmonic distortion	f_{IN} = 5 MHz		71	81		67.5	81		dBc
		f_{IN} = 30 MHz			78			77.5		dBc
		f_{IN} = 90 MHz			74			70		dBc
HD2	Second-harmonic distortion	f_{IN} = 5 MHz		73	90		70.5	86		dBc
		f_{IN} = 30 MHz			88			84		dBc
		f_{IN} = 90 MHz			85			83		dBc
HD3	Third-harmonic distortion	f_{IN} = 5 MHz		73	83		70.5	83		dBc
		f_{IN} = 30 MHz			80			79		dBc
		f_{IN} = 90 MHz			76			72.5		dBc
	Worst spur (other than second and third harmonics) (2)	f_{IN} = 5 MHz		75	93		65	79		dBc
		f_{IN} = 30 MHz			92			74		dBc
		f_{IN} = 90 MHz			90		60	71		dBc
IMD	Two-tone intermodulation distortion	f_1 = 8 MHz, f_2 = 10 MHz, each tone at –7 dBFS			83					dBc
	Crosstalk	With a full-scale, 10-MHz aggressor signal applied and no input on victim channel	Adjacent channel		86			95		dBc
			Far channel		110			110		dBc
	Overload recovery	Recovery to < 1% of full-scale after a 6-dB input overload			1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For a 50-mV_{PP} signal on AVDD supply, up to 10 MHz, no signal applied to analog inputs			> 50			> 50		dB
DNL	Differential nonlinearity	f_{IN} = 5 MHz		–0.8	±0.3	+0.95				LSBs
INL	Integrated nonlinearity	f_{IN} = 5 MHz			±0.2	±1.1				LSBs

(1) In the 4-channel interleaving mode, this parameter does not include interleaving spur. Spur is specified separately as part of the worst spur parameter.
(2) In the 4-channel interleaving mode, worst spur includes interleaving spur. Also see Figure 44, which shows interleaving spur across input frequency.

DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD = 1.8 V and DRVDD = 1.8 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS ($\overline{\text{RESET}}$, SCLK, SDATA, $\overline{\text{CS}}$, SYNC, PDN, INTERLEAVE_MUX)							
V_{IH}	High-level input voltage		All pins support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage		All pins support 1.8-V and 3.3-V CMOS logic levels			0.4	V
I_{IH}	High-level input current	$\overline{\text{CS}}$, SDATA, SCLK(1)	V_{HIGH} = 1.8 V		6		µA
I_{IL}	Low-level input current	$\overline{\text{CS}}$, SDATA, SCLK(1)	V_{LOW} = 0 V		0.1		µA
DIGITAL OUTPUTS (CMOS INTERFACE: SDOUT)							
V_{OH}	High-level output voltage			AVDD – 0.1			V
V_{OL}	Low-level output voltage					0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: OUT1_p, OUT1_n to OUT8_p, OUT8_n, ADCLKp, ADCLKn, LCLKp, LCLKn)							
V_{ODH}	High-level output differential voltage(2)			340		560	mV
V_{ODL}	Low-level output differential voltage(2)			–560		–340	mV
V_{OCM}	Output common-mode voltage			0.93		1.2	mV

(1) $\overline{\text{CS}}$, SDATA, and SCLK have an internal 220-kΩ pull-down resistor.
(2) With an external 100-Ω termination.

TIMING REQUIREMENTS(1)

Typical values are at +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 200 MSPS, sine-wave input clock, C_{LOAD} = 5 pF, and R_{LOAD} = 100 Ω, unless otherwise noted.
Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V, with decimation filters DISABLED.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay			4		ns
	Aperture delay matching	Between any two channels of the same device		±200		ps
	Variation of aperture delay	Between two devices at the same temperature and AVDD supply		±1		ns
t_J	Aperture jitter	Sample uncertainty		300		fs rms
	Wake-up time	Time to valid data after coming out of standby		6		µs
		Time to valid data after coming out of global power-down mode		100		µs
	ADC latency(2)	Interleaving disabled		12		Input clock cycles
		Interleaving enabled		24		Input clock cycles
10x SERIALIZATION						
t_{SU}	Data setup time	Data valid to LCLKP zero-crossing	0.200			ns
t_H	Data hold time	LCLKP zero-crossing to data becoming invalid	0.160			ns
t_{PDI}	Clock propagation delay	Input clock rising edge crossover to output clock rising edge crossover		t_{PDI} = (4 / 5) × t_S + t_{DELAY}		ns
t_{DELAY}	Delay time		7.8		11.8	ns
	Variation of t_{DELAY}	Between two devices at the same temperature and LVDD supply		±0.8		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock (LCLKP – LCLKN)		50		%
ACROSS ALL SERIALIZATION MODES						
t_{FALL}	Data fall time	Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS		0.13		ns
t_{RISE}	Data rise time	Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS		0.13		ns
$t_{CLKRISE}$	Output clock rise time	Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS		0.13		ns
$t_{CLKFALL}$	Output clock fall time	Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS		0.13		ns

(1) Timing parameters are ensured by design and characterization, but are not tested in production.
(2) At higher frequencies, t_{PDI} is greater than one clock period. Overall latency = ADC latency + 1.

Table 1. 12x Serialization with Decimation Filters Disabled(1)(2)

INPUT CLOCK FREQUENCY (MHz)		OUTPUT DATA RATE (Mbps)	SETUP TIME (ns)(3)			HOLD TIME (ns)(3)			$t_{PDI} = (9 / 12) \times t_S + t_{DELAY}$ (Where t_{DELAY} is specified as below, ns)		
NON-INTERLEAVED MODE	INTERLEAVED MODE(4)		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
10	20	120	3.80			3.80			8		13
20	40	240	1.60			1.80			8		13
40	80	480	0.80			0.69			8		13
65	130	780	0.38			0.19			8		13
80	160	960	0.22			0.14			8		13

(1) Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V.
(2) All timing specifications are taken with default output clock and data delay settings (0 ps). Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for additional output clock and data delay options.
(3) When decimation filters are enabled, the minimum setup and minimum hold time further reduce by 100 ps compared to their values with the filters disabled (at the same output data rate).
Example: At an 80-MHz input clock frequency, with decimation by 2 enabled, output data rate = 480 Mbps. At 480 Mbps, as per Table 1, the setup time with the decimation disabled is 0.80 ns. Therefore, the set-up time with filter enabled is 100 ps lower (0.8 – 0.1 = 0.7). Similarly, the hold time with filter enabled is 0.59 ns.
(4) Refer to the *Interleaving Mode* section in the Application Information for details on interleaving mode.

Table 2. 10x Serialization with Decimation Filters Disabled(1)(2)

INPUT CLOCK FREQUENCY (MHz)		OUTPUT DATA RATE (Mbps)	SETUP TIME (ns)(3)			HOLD TIME (ns)(3)			$t_{PDI} = (8 / 10) \times t_S + t_{DELAY}$ (Where t_{DELAY} is specified as below, ns)		
NON-INTERLEAVED MODE	INTERLEAVED MODE(4)		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
40	80	400	0.85			1			7.8		11.8
65	130	650	0.52			0.35			7.8		11.8
80	160	800	0.33			0.19			7.8		11.8
100	200	1000	0.2			0.16			7.8		11.8

(1) Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V.
(2) All timing specifications are taken with default output clock and data delay settings (0 ps). Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for additional output clock and data delay options.
(3) When decimation filters are enabled, the minimum setup and minimum hold time further reduce by 100 ps compared to their values with the filters disabled (at the same output data rate).
Example: At an 80-MHz input clock frequency, with decimation by 2 enabled, output data rate = 400 Mbps. At 400 Mbps, as per Table 2, the setup time with the decimation disabled is 0.85 ns. Therefore, the set-up time with filter enabled is 100 ps lower (0.85 – 0.10 = 0.75). Similarly ,the hold time with filter enabled is 0.90 ns.
(4) Refer to the *Interleaving Mode* section in the Application Information for details on interleaving mode.

Table 3. 14x Serialization with Decimation by two filter enabled (Data Rate = 0.5x)(1)(2)(3)

SAMPLING FREQUENCY (MSPS)	OUTPUT DATA RATE (Mbps)	SETUP TIME (ns)			HOLD TIME (ns)		
		MIN	TYP	MAX	MIN	TYP	MAX
65	455	0.73			0.75		
80	560	0.54			0.50		
100	700	0.32			0.25		

(1) Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V.
(2) All timing specifications are taken with default output clock and data delay settings (0 ps).
(3) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for additional output clock and data delay options.

Table 4. 14x Serialization with Decimation by four filter enabled (Data Rate = 0.25x)(1)(2)(3)

SAMPLING FREQUENCY (MSPS)	OUTPUT DATA RATE (Mbps)	SETUP TIME (ns)			HOLD TIME (ns)		
		MIN	TYP	MAX	MIN	TYP	MAX
65	227.5	1.7			1.9		
80	280	1.3			1.45		
100	350	0.9			1.1		

(1) Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V.
(2) All timing specifications are taken with default output clock and data delay settings (0 ps).
(3) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for additional output clock and data delay options.

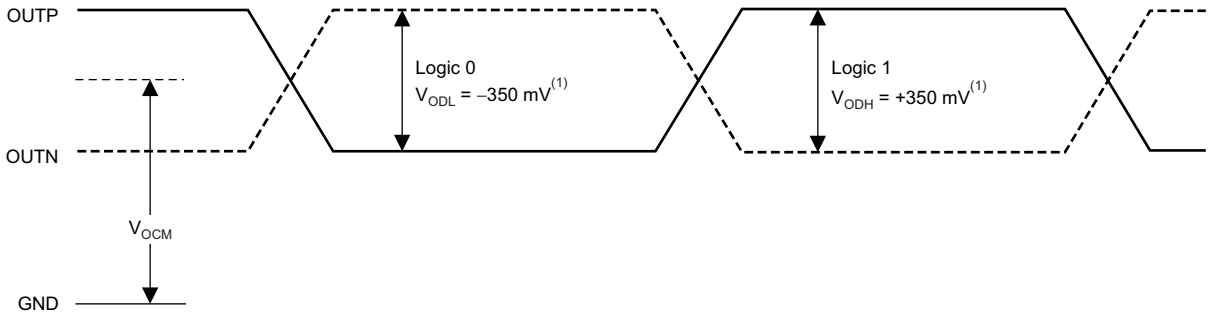
Table 5. 14x Serialization with Decimation by eight filter enabled (Data Rate = 0.125x) (1)(2)(3)

SAMPLING FREQUENCY (MSPS)	OUTPUT DATA RATE (Mbps)	SETUP TIME (ns)			HOLD TIME (ns)		
		MIN	TYP	MAX	MIN	TYP	MAX
65	113.75	3.8			3.8		
80	140	3			3		
100	175	2.2			2.2		

(1) Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V.
(2) All timing specifications are taken with default output clock and data delay settings (0 ps).
(3) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for additional output clock and data delay options.

PARAMETRIC MEASUREMENT INFORMATION

Figure 1 shows a timing diagram of the LVDS output voltage levels.



(1) With an external 100-Ω termination.

Figure 1. LVDS Output Voltage Levels

Figure 2 shows the latency timing diagram.

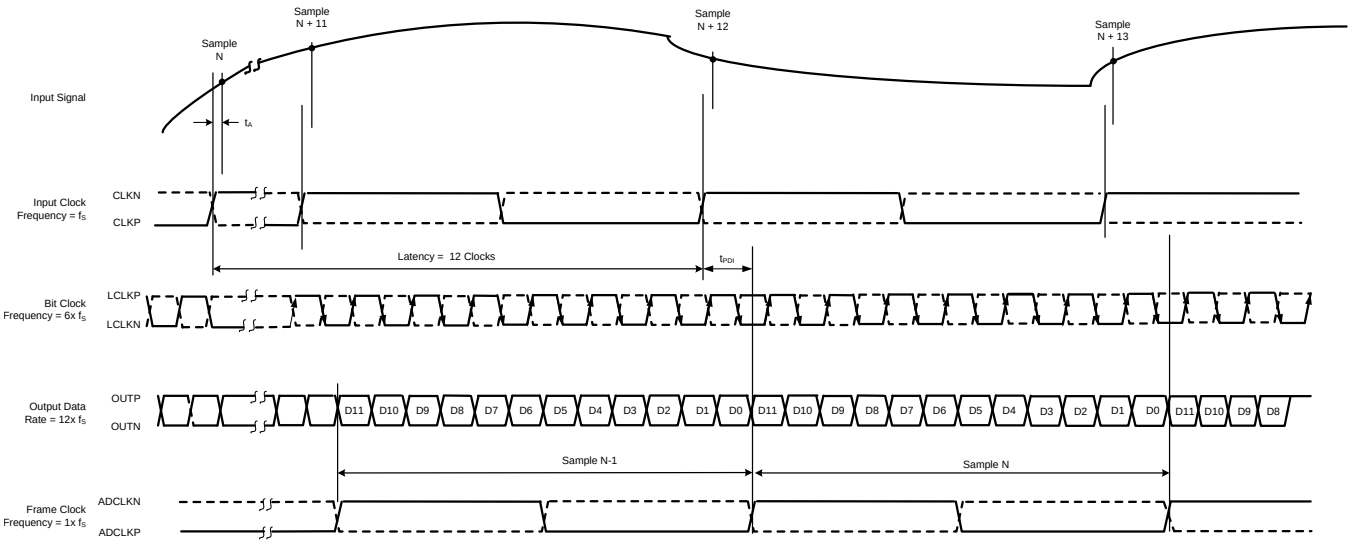
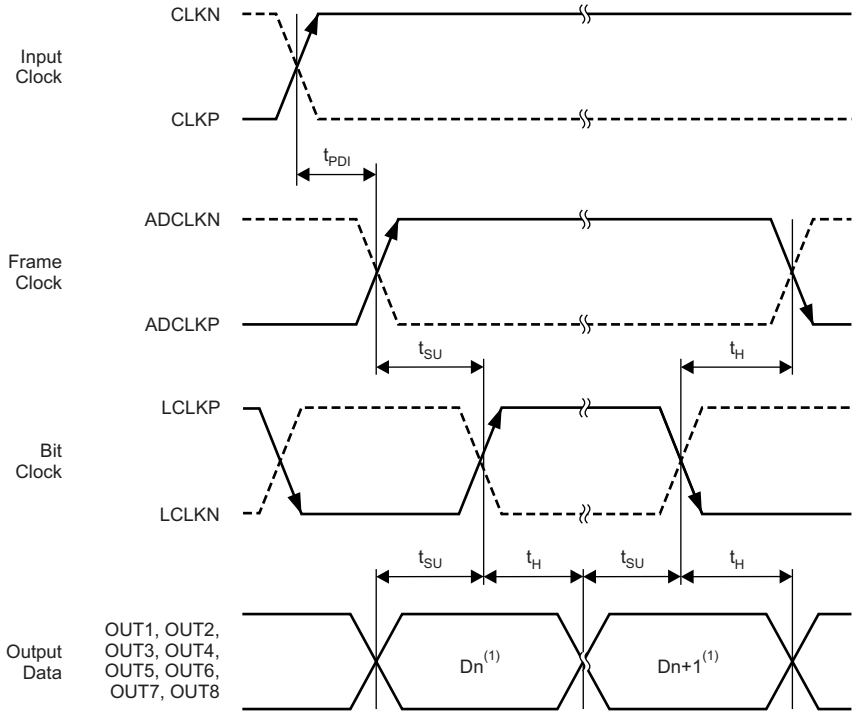


Figure 2. Latency Timing Diagram

PARAMETRIC MEASUREMENT INFORMATION (continued)

LVDS OUTPUT TIMING

Figure 3 shows the output timing described in the Timing Requirements table.

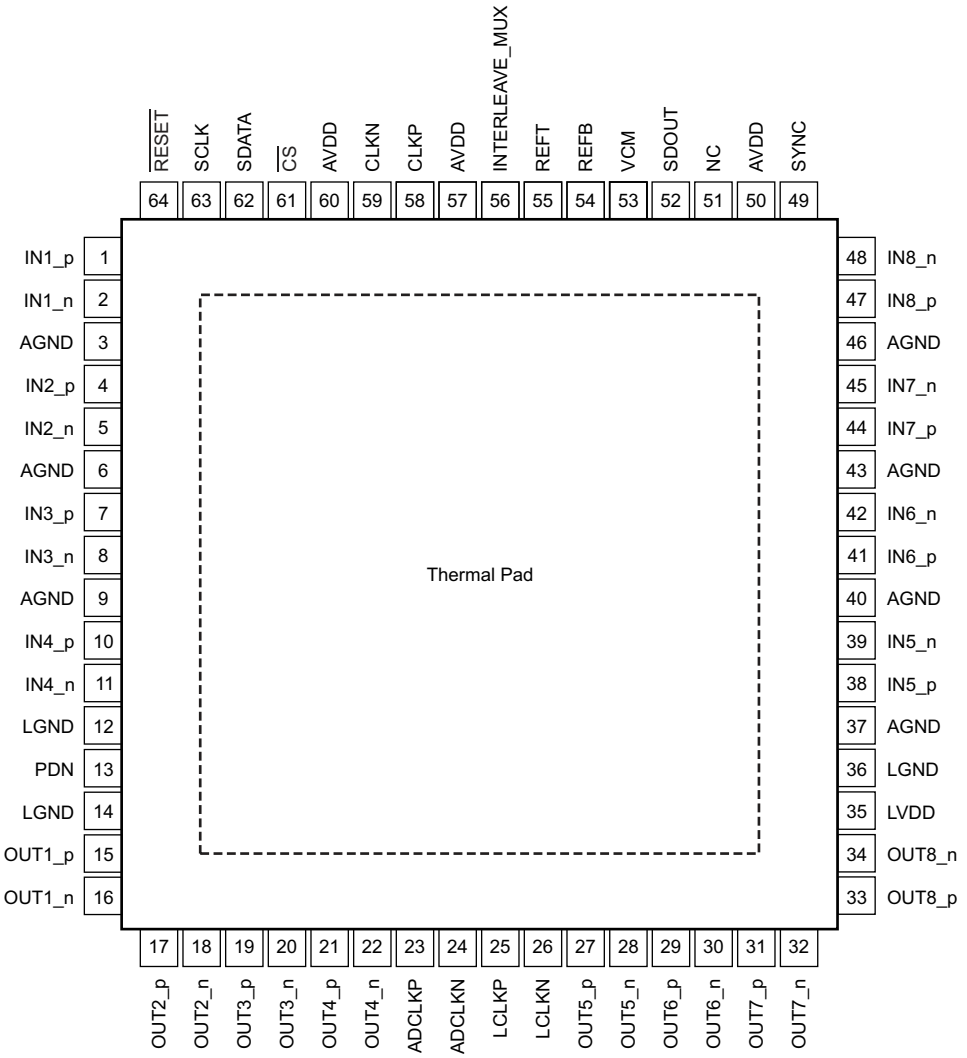


(1) n = 0 to 11.

Figure 3. LVDS Output Timing

PIN DESCRIPTION

RGC PACKAGE
QFN-64
(Top View)



PIN DESCRIPTIONS

NAME	NO.	FUNCTION(1)	DESCRIPTION
ADCLKN	24	DO	Differential LVDS frame clock, negative
ADCLKP	23	DO	Differential LVDS frame clock, positive
AGND	3, 6, 9, 37, 40, 43, 46	G	Analog ground pin
AVDD	50, 57, 60	S	Analog supply pin, 1.8 V
CLKN	59	AI	Differential clock input, negative
CLKP	58	AI	Differential clock input, positive
$\overline{CS}$	61	DI	Serial enable chip select; active low digital input
INTERLEAVE_MUX	56	DI	Control input to select conversion of odd channels (1, 3, 5, and 7) or even channels (2, 4, 6, and 8).
IN1_n	2	AI	Differential analog input for channel 1, negative
IN1_p	1	AI	Differential analog input for channel 1, positive
IN2_n	5	AI	Differential analog input for channel 2, negative
IN2_p	4	AI	Differential analog input for channel 2, positive
IN3_n	8	AI	Differential analog input for channel 3, negative
IN3_p	7	AI	Differential analog input for channel 3, positive
IN4_n	11	AI	Differential analog input for channel 4, negative
IN4_p	10	AI	Differential analog input for channel 4, positive
IN5_n	39	AI	Differential analog input for channel 5, negative
IN5_p	38	AI	Differential analog input for channel 5, positive
IN6_n	42	AI	Differential analog input for channel 6, negative
IN6_p	41	AI	Differential analog input for channel 6, positive
IN7_n	45	AI	Differential analog input for channel 7, negative
IN7_p	44	AI	Differential analog input for channel 7, positive
IN8_n	48	AI	Differential analog input for channel 8, negative
IN8_p	47	AI	Differential analog input for channel 8, positive
LCLKN	26	DO	LVDS differential bit clock output pins (6x), negative
LCLKP	25	DO	LVDS differential bit clock output pins (6x), positive
LGND	12, 14, 36	G	Digital ground pin
LVDD	35	S	Digital and I/O power supply, 1.8 V
NC	51	—	Do not connect
OUT1_n	16	DO	Channel 1 differential LVDS negative data output
OUT1_p	15	DO	Channel 1 differential LVDS positive data output
OUT2_n	18	DO	Channel 2 differential LVDS negative data output
OUT2_p	17	DO	Channel 2 differential LVDS positive data output
OUT3_n	20	DO	Channel 3 differential LVDS negative data output
OUT3_p	19	DO	Channel 3 differential LVDS positive data output
OUT4_n	22	DO	Channel 4 differential LVDS negative data output
OUT4_p	21	DO	Channel 4 differential LVDS positive data output
OUT5_n	28	DO	Channel 5 differential LVDS negative data output
OUT5_p	27	DO	Channel 5 differential LVDS positive data output
OUT6_n	30	DO	Channel 6 differential LVDS negative data output
OUT6_p	29	DO	Channel 6 differential LVDS positive data output
OUT7_n	32	DO	Channel 7 differential LVDS negative data output
OUT7_p	31	DO	Channel 7 differential LVDS positive data output
OUT8_n	34	DO	Channel 8 differential LVDS negative data output
OUT8_p	33	DO	Channel 8 differential LVDS positive data output
PDN	13	DI	Power-down control input pin

(1) Pin functionality: AI = analog input; DI = digital input; DO = digital output; G = ground; and S = supply.

PIN DESCRIPTIONS (continued)

NAME	NO.	FUNCTION(1)	DESCRIPTION
REFB	54	AI	Negative reference input and output. Internal reference mode: Reference bottom voltage (0.45 V) is output on this pin. A decoupling capacitor is not required on this pin. External reference mode: Reference bottom voltage (0.45 V) must be externally applied to this pin.
REFT	55	AI	Positive reference input and output. Internal reference mode: Reference top voltage (1.45 V) is output on this pin. A decoupling capacitor is not required on this pin. External reference mode: Reference top voltage (1.45 V) must be externally applied to this pin.
$\overline{\text{RESET}}$	64	DI	Active high RESET input
SCLK	63	DI	Serial clock input
SDATA	62	DI	Serial data input
SDOUT	52	DO	Serial data output
SYNC	49	DI	Control input pin to synchronize test patterns and decimation filters across devices
VCM	53	AI	Common-mode voltage output pin, 0.95 V.

FUNCTIONAL BLOCK DIAGRAMS

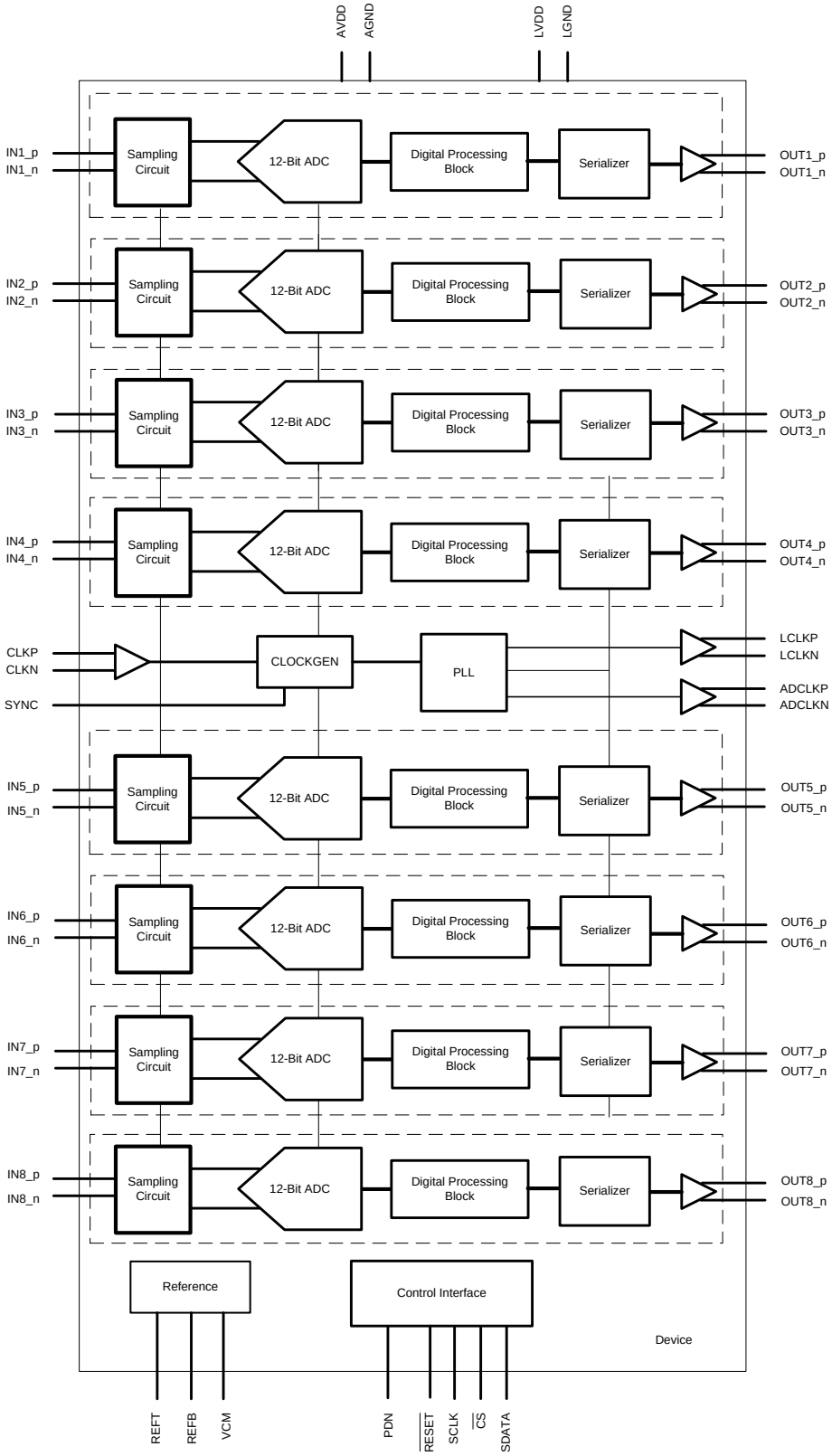


Figure 4. 10- and 12-Bit, 8-Channel ADC, Non-Interleaving Mode

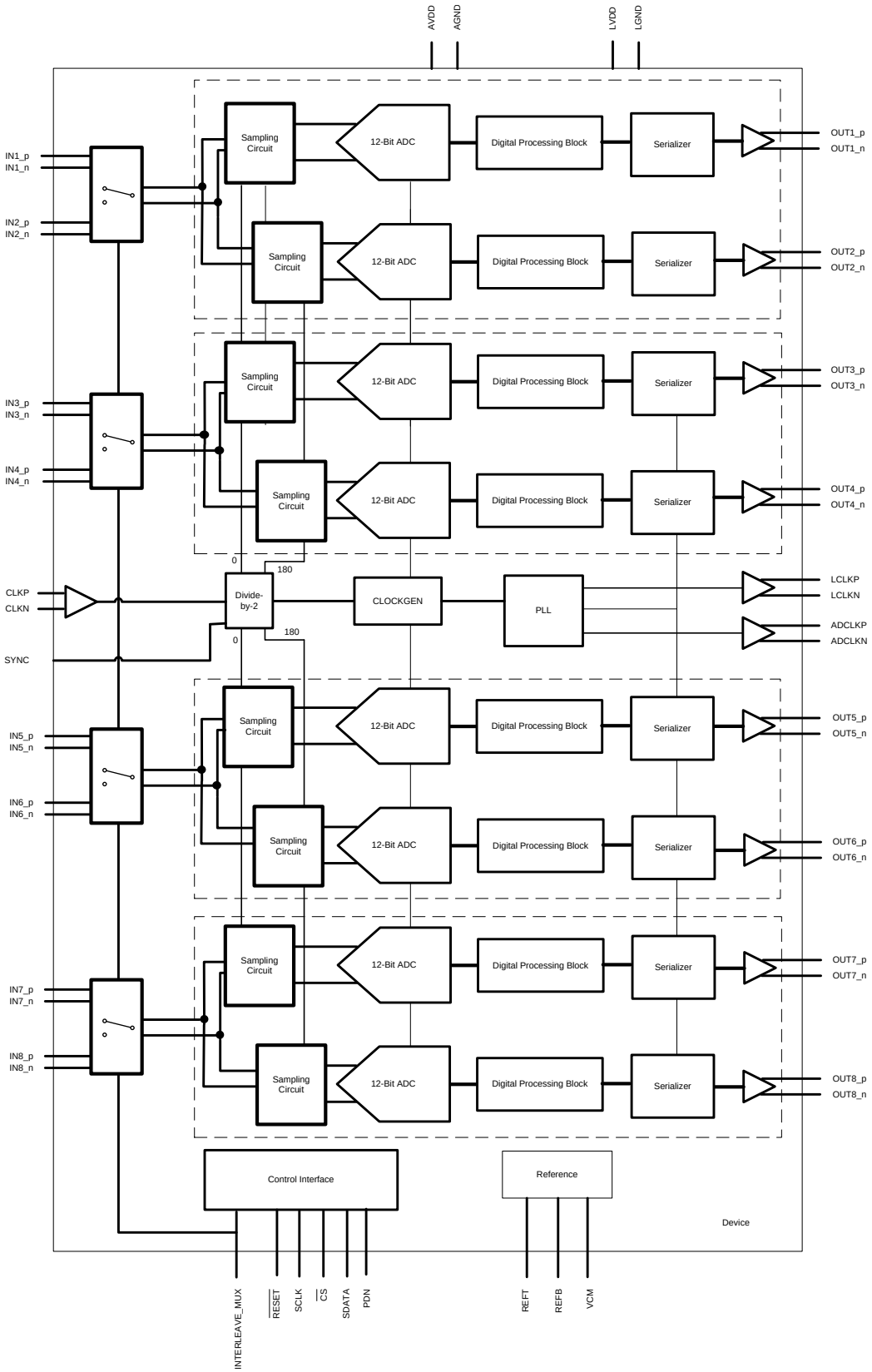


Figure 5. 10- and 12-Bit, 4-Channel ADC, Interleaving Mode

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Non-Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

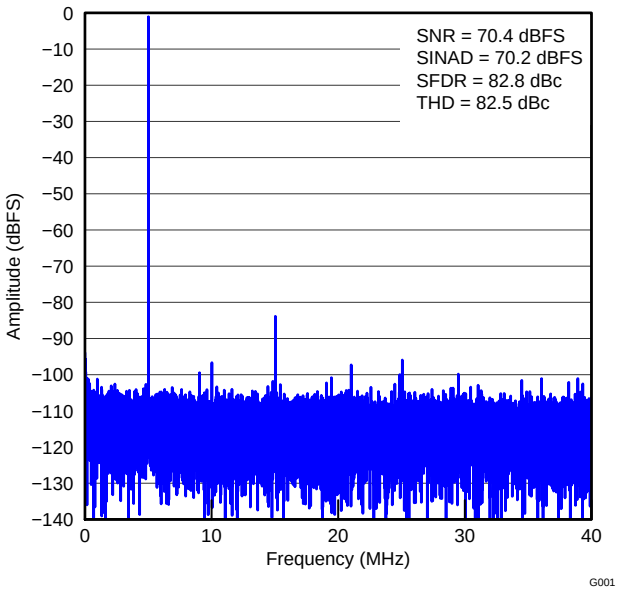


Figure 6. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 80 MSPS)

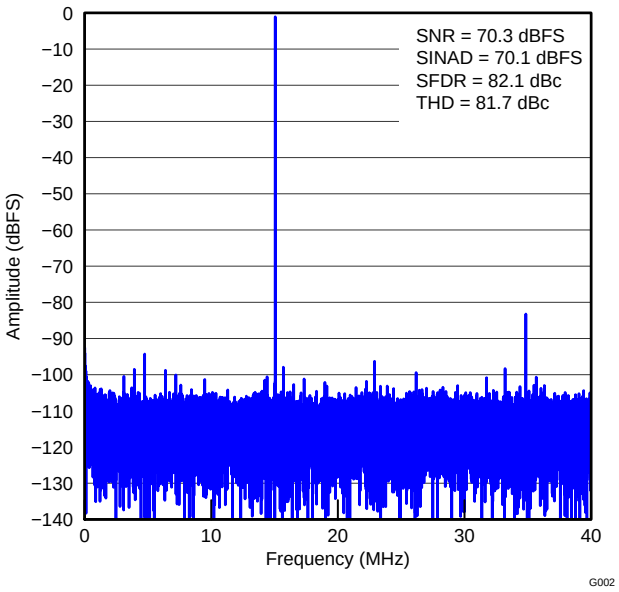


Figure 7. FFT FOR 15-MHz INPUT SIGNAL (Sample Rate = 80 MSPS)

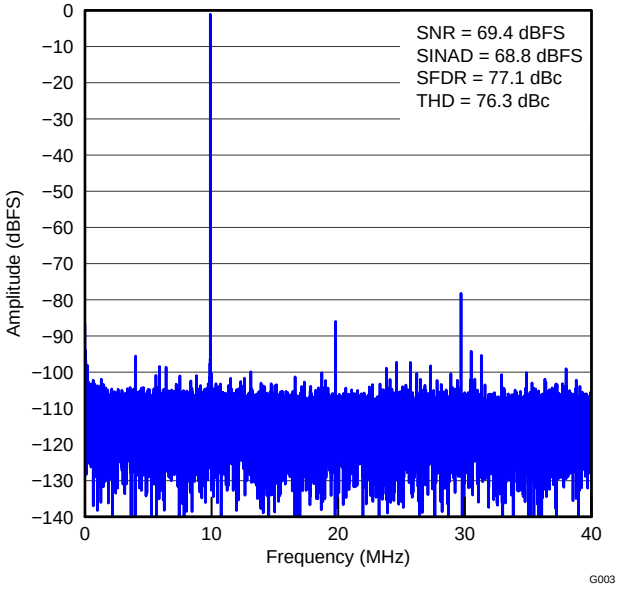


Figure 8. FFT FOR 70-MHz INPUT SIGNAL (Sample Rate = 80 MSPS)

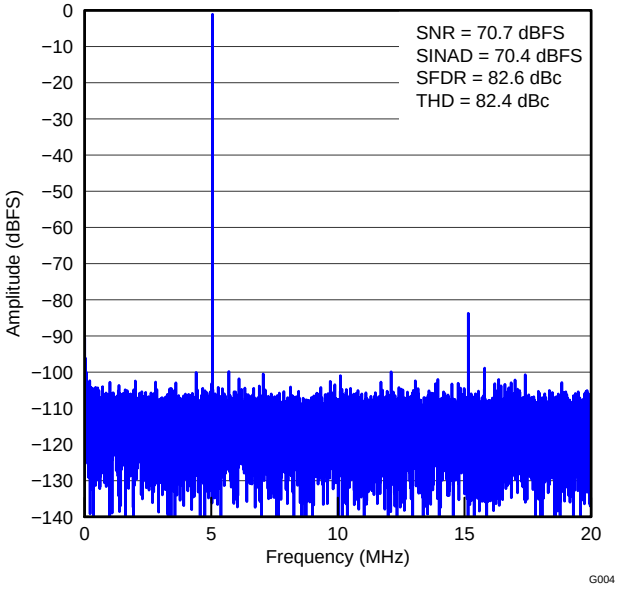


Figure 9. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 40 MSPS)

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

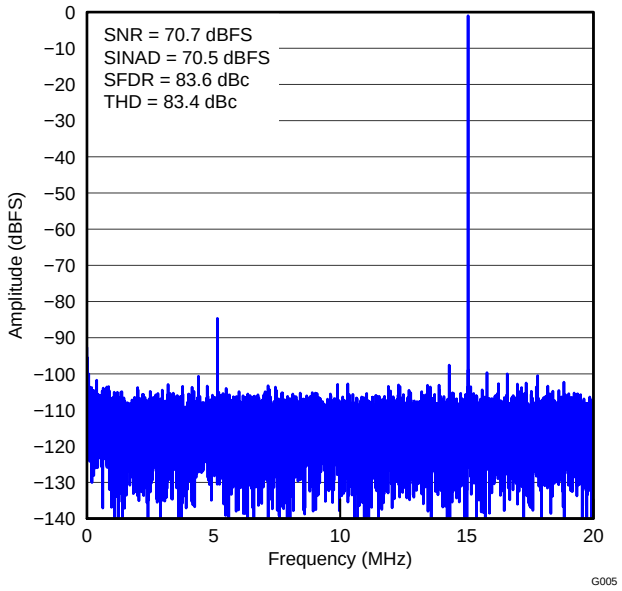


Figure 10. FFT FOR 15-MHz INPUT SIGNAL (Sample Rate = 40 MSPS)

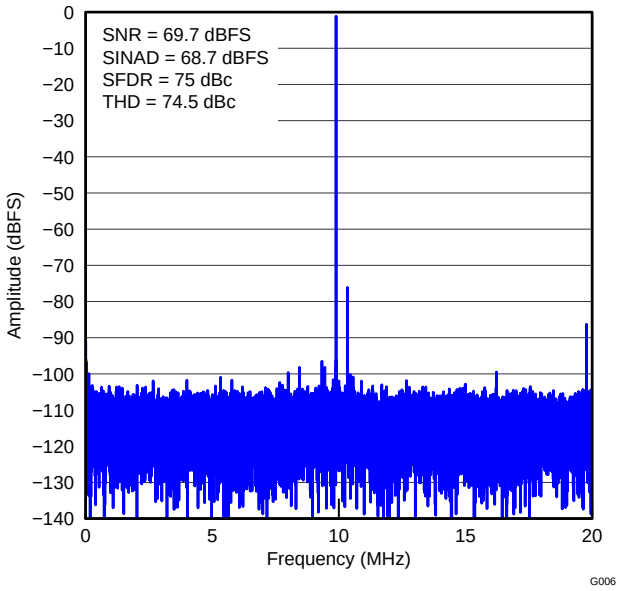


Figure 11. FFT FOR 70-MHz INPUT SIGNAL (Sample Rate = 40 MSPS)

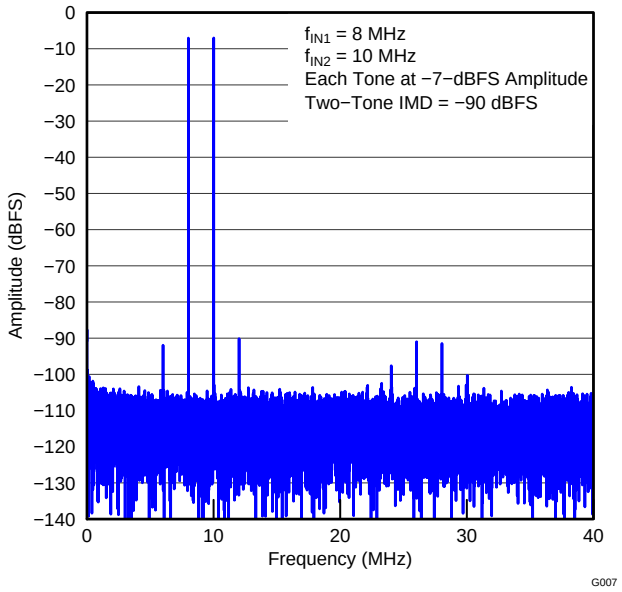


Figure 12. FFT WITH TWO-TONE SIGNAL

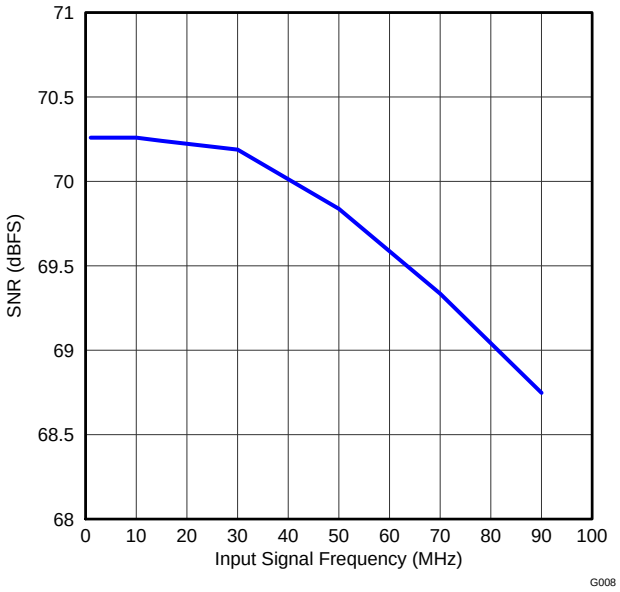


Figure 13. SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL FREQUENCY

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

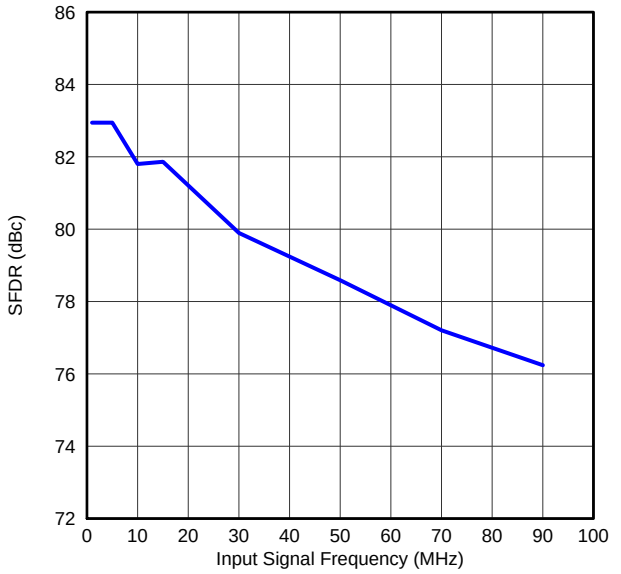


Figure 14. SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY

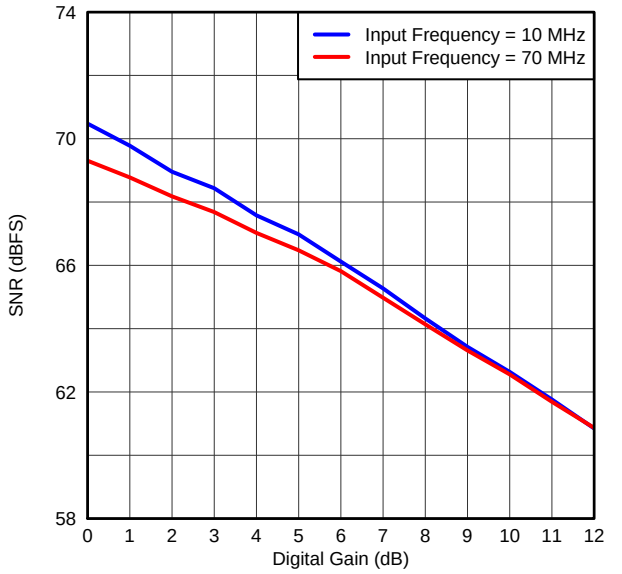


Figure 15. SIGNAL-TO-NOISE RATIO vs DIGITAL GAIN

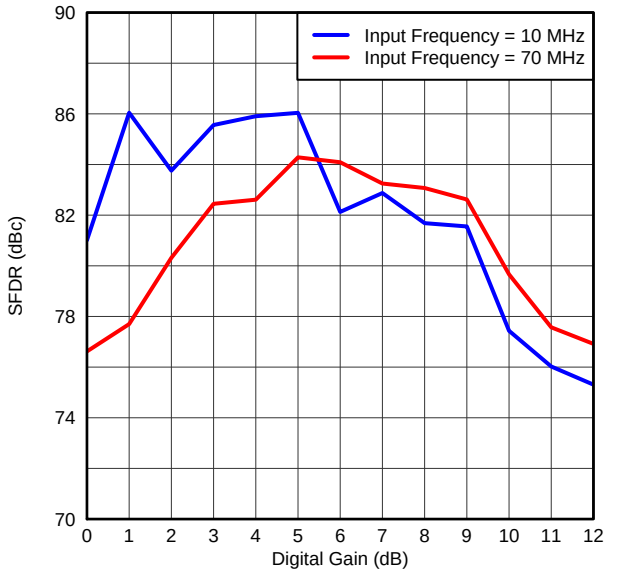


Figure 16. SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL GAIN

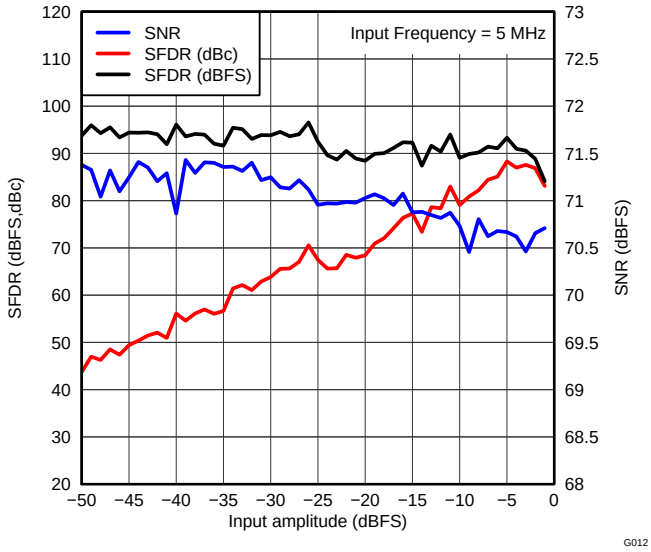


Figure 17. PERFORMANCE vs INPUT AMPLITUDE

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

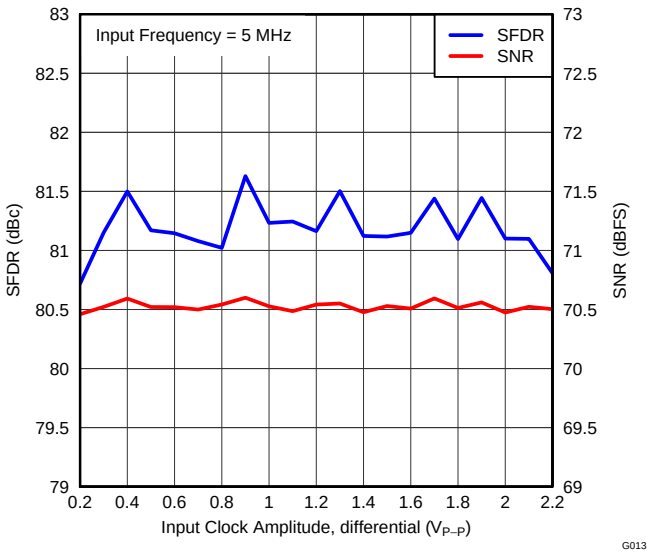


Figure 18. PERFORMANCE vs INPUT CLOCK AMPLITUDE

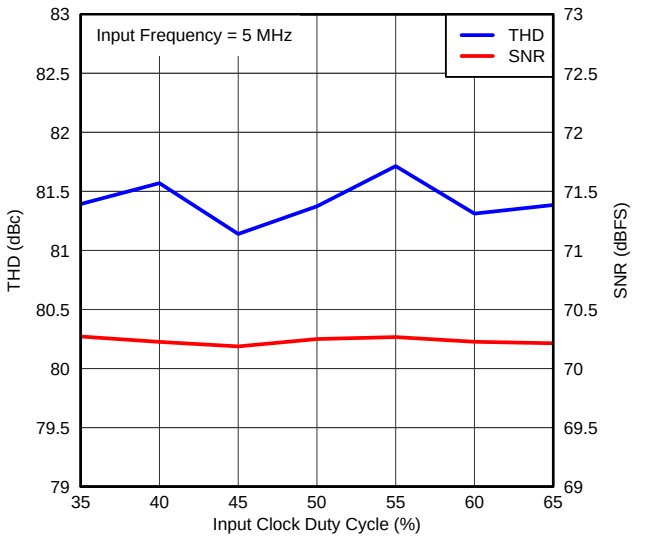


Figure 19. PERFORMANCE vs INPUT CLOCK DUTY CYCLE

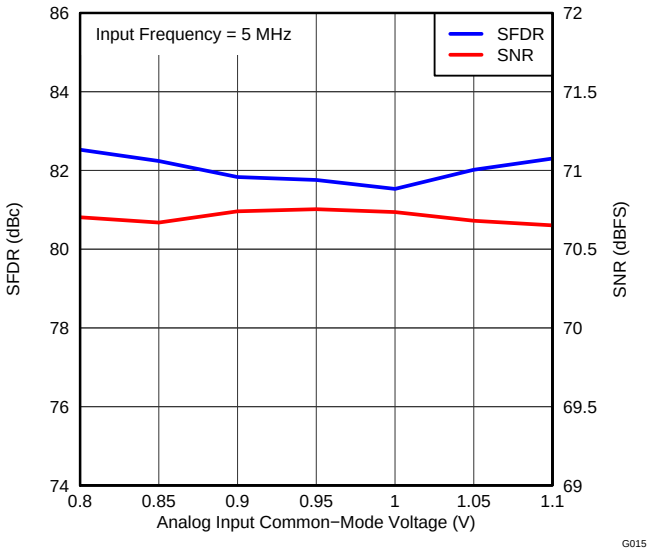


Figure 20. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

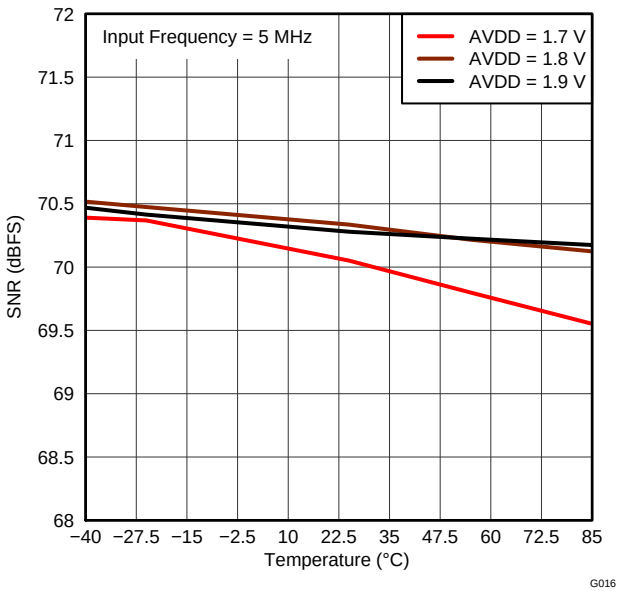


Figure 21. SIGNAL-TO-NOISE RATIO vs AVDD AND TEMPERATURE

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

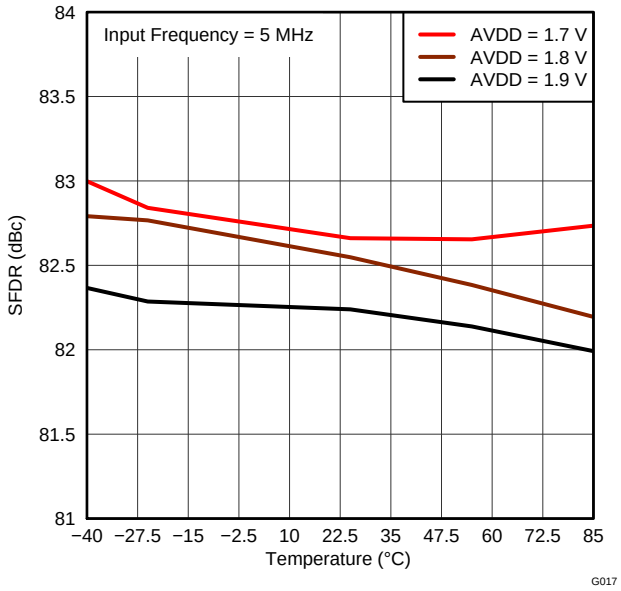


Figure 22. SPURIOUS-FREE DYNAMIC RANGE vs AVDD AND TEMPERATURE

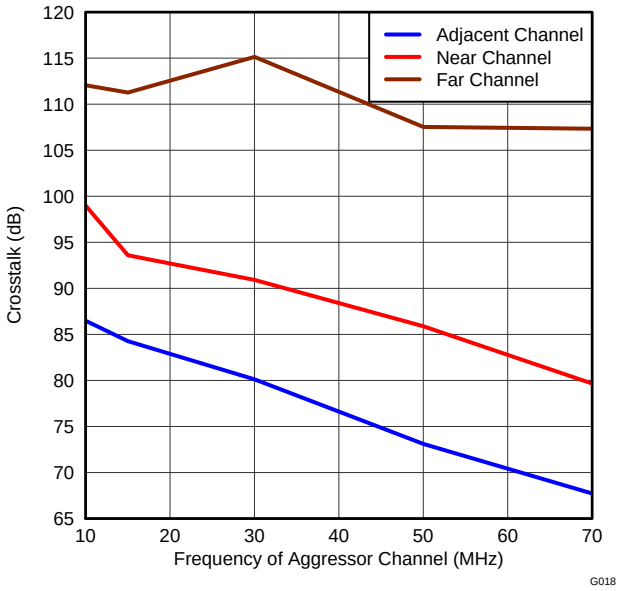


Figure 23. CROSSTALK vs FREQUENCY (1)

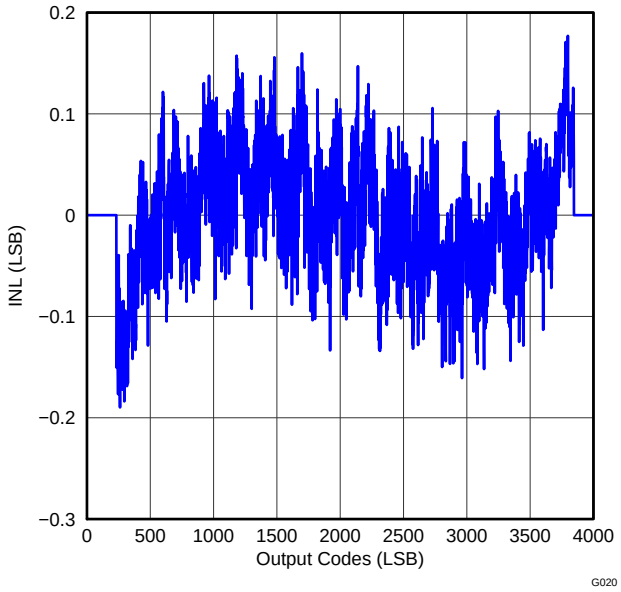


Figure 24. INTEGRAL NONLINEARITY

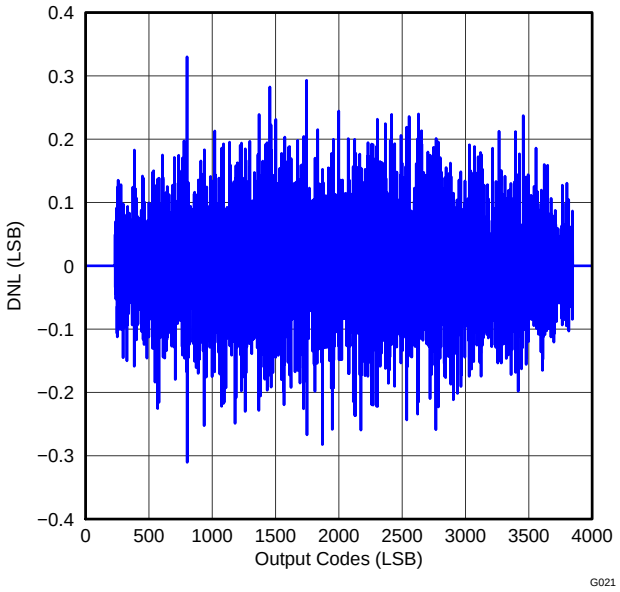


Figure 25. DIFFERENTIAL NONLINEARITY

(1) Adjacent channel: Neighboring channels on the immediate left and right of the channel of interest.
Near channel: Channels on the same side of the package, except the immediate neighbors.
Far channel: Channels on the opposite side of the package.

TYPICAL CHARACTERISTICS: Digital Processing (8-Channel, 12-Bit, Non-Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

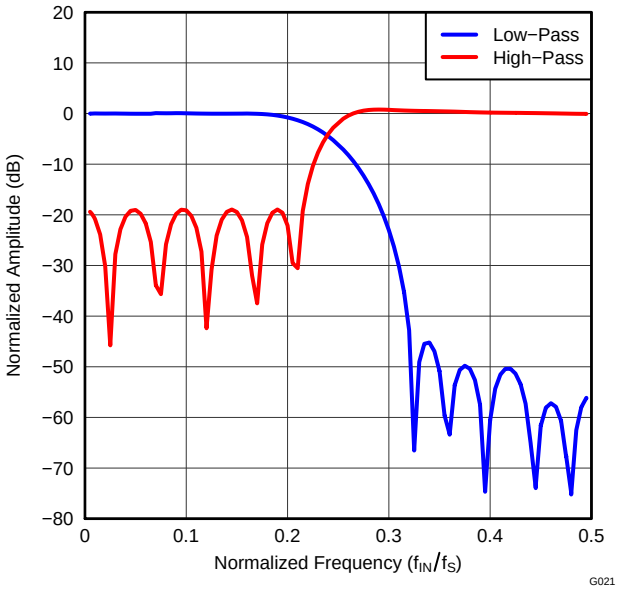


Figure 26. DIGITAL FILTER RESPONSE (Decimate-by-2)

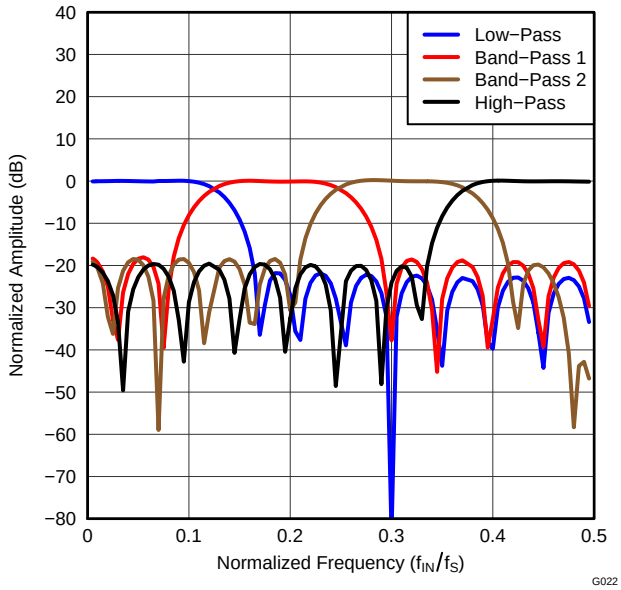


Figure 27. DIGITAL FILTER RESPONSE (Decimate-by-4)

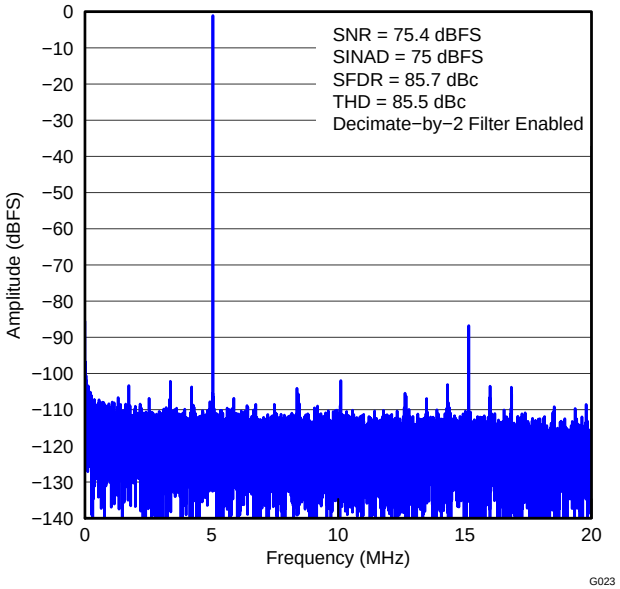


Figure 28. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 80 MSPS, Decimation Filter = 2) (1)

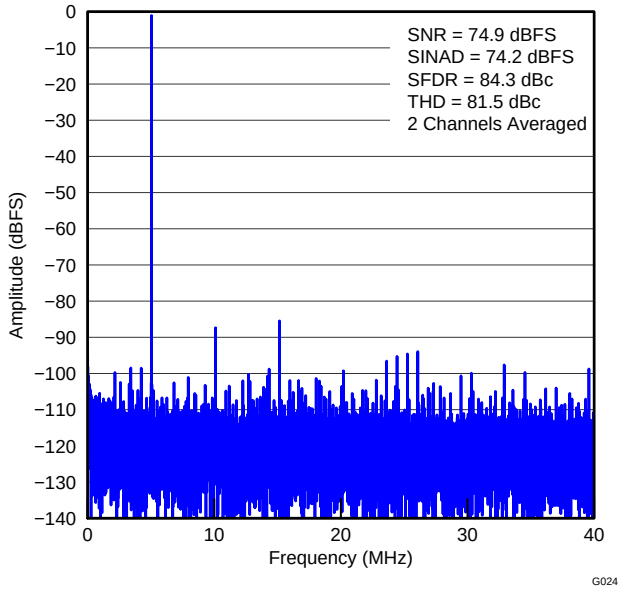


Figure 29. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 80 MSPS by Averaging Two Channels)(1)

(1) 14x serialization is used to capture data.

TYPICAL CHARACTERISTICS:
Digital Processing (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 80 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

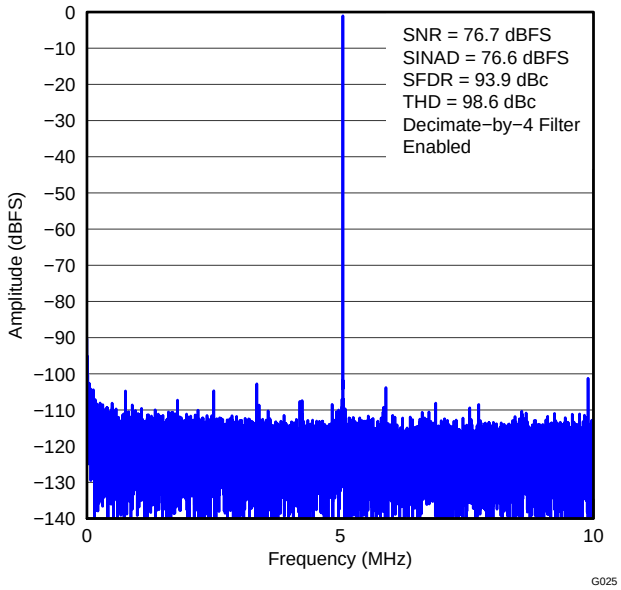


Figure 30. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 80 MSPS, Decimation Filter = 4) (2)

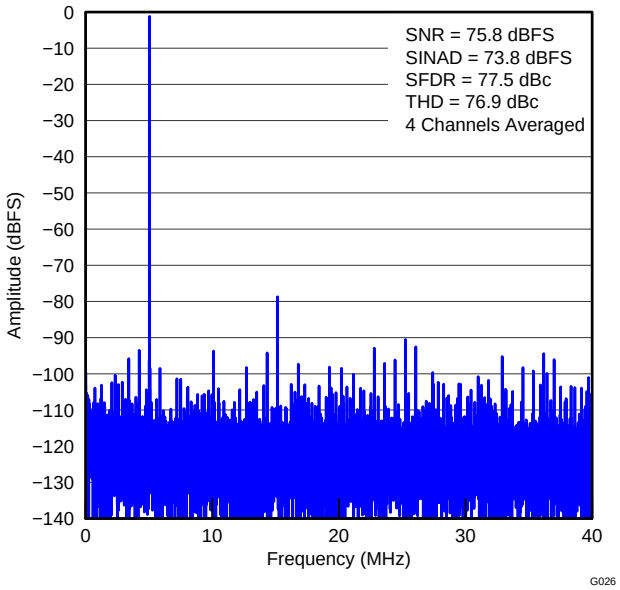


Figure 31. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 80 MSPS by Averaging Four Channels)(2)

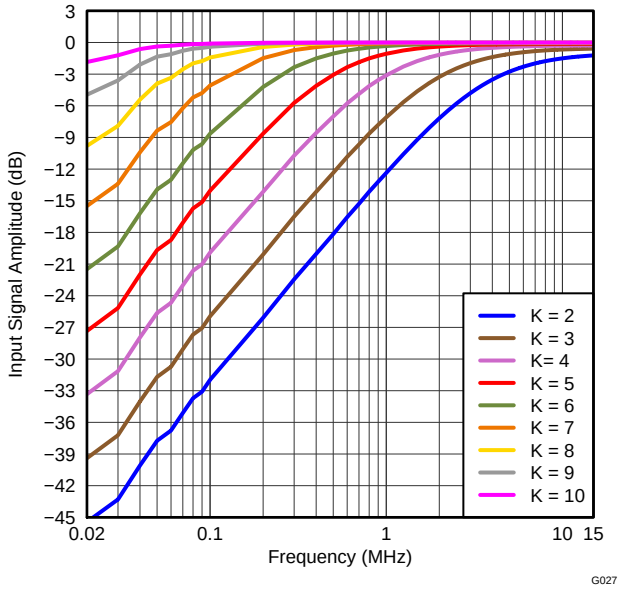


Figure 32. DIGITAL HIGH-PASS FILTER RESPONSE

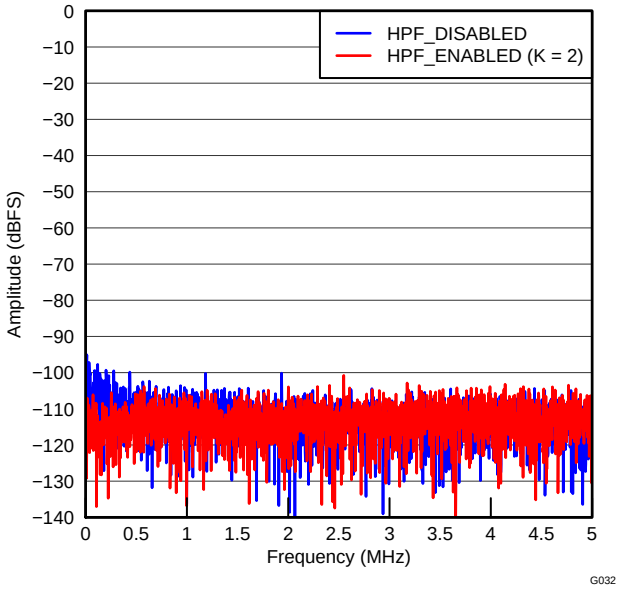


Figure 33. FFT WITH HPF ENABLED AND DISABLED (No Signal)

(2) 14x serialization is used to capture data.

TYPICAL CHARACTERISTICS: Power Consumption (8-Channel, 12-Bit, Non-Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

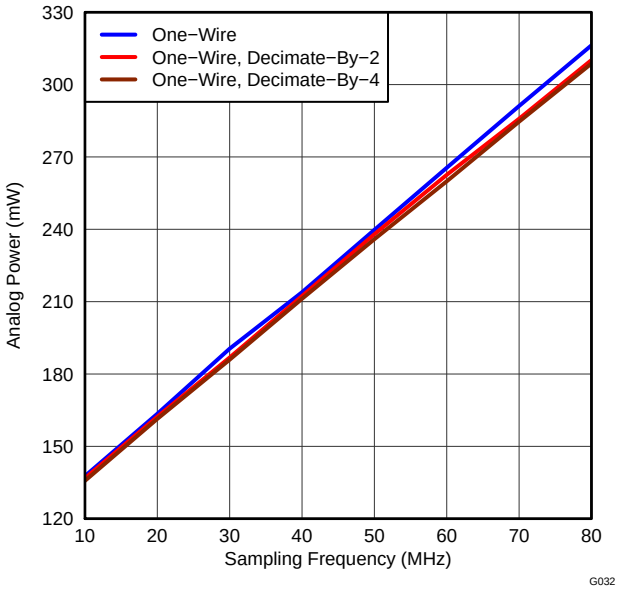


Figure 34. ANALOG SUPPLY POWER

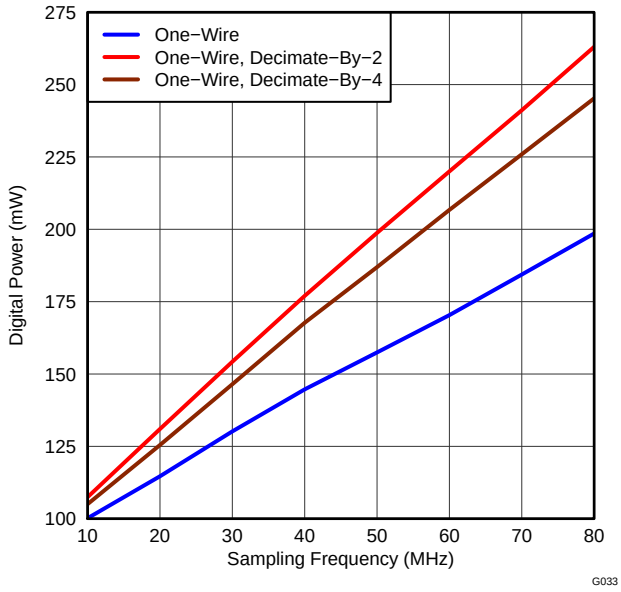


Figure 35. DIGITAL SUPPLY POWER

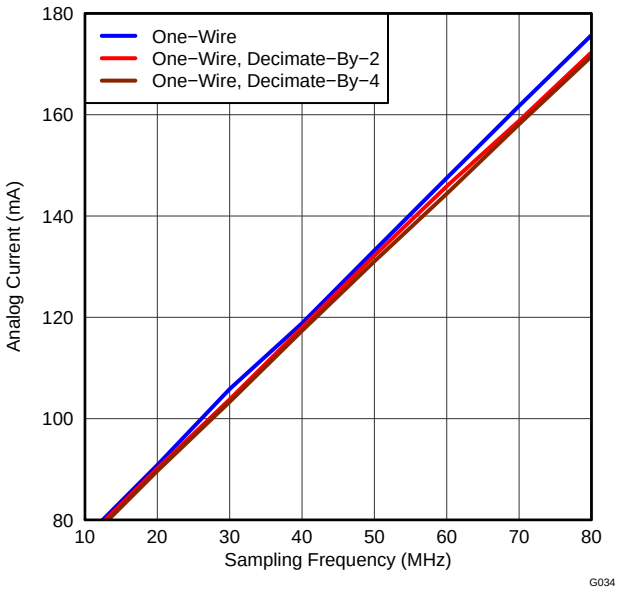


Figure 36. ANALOG SUPPLY CURRENT

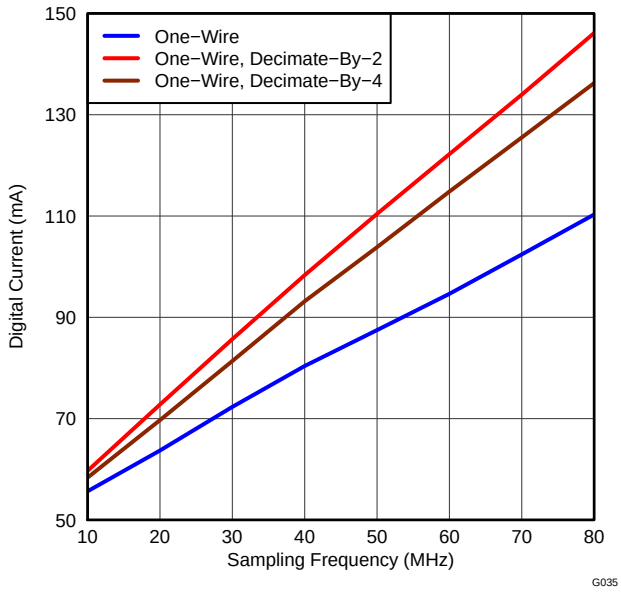


Figure 37. DIGITAL SUPPLY CURRENT

TYPICAL CHARACTERISTICS:
Power Consumption (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

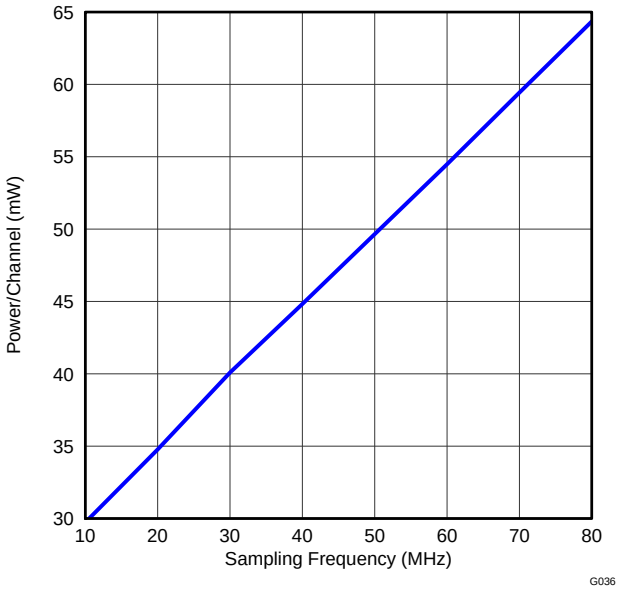


Figure 38. TOTAL POWER PER CHANNEL

TYPICAL CHARACTERISTICS: Contour (8-Channel, 12-Bit, Non-Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

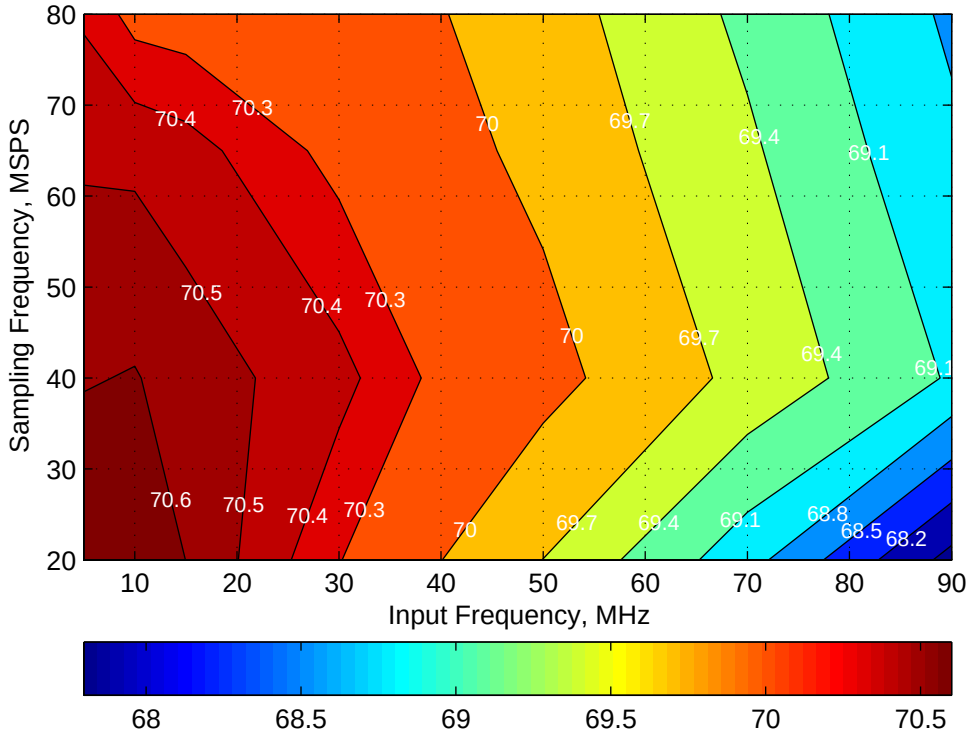


Figure 39. SIGNAL-TO-NOISE RATIO vs INPUT AND SAMPLING FREQUENCIES

TYPICAL CHARACTERISTICS: Contour (8-Channel, 12-Bit, Non-Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

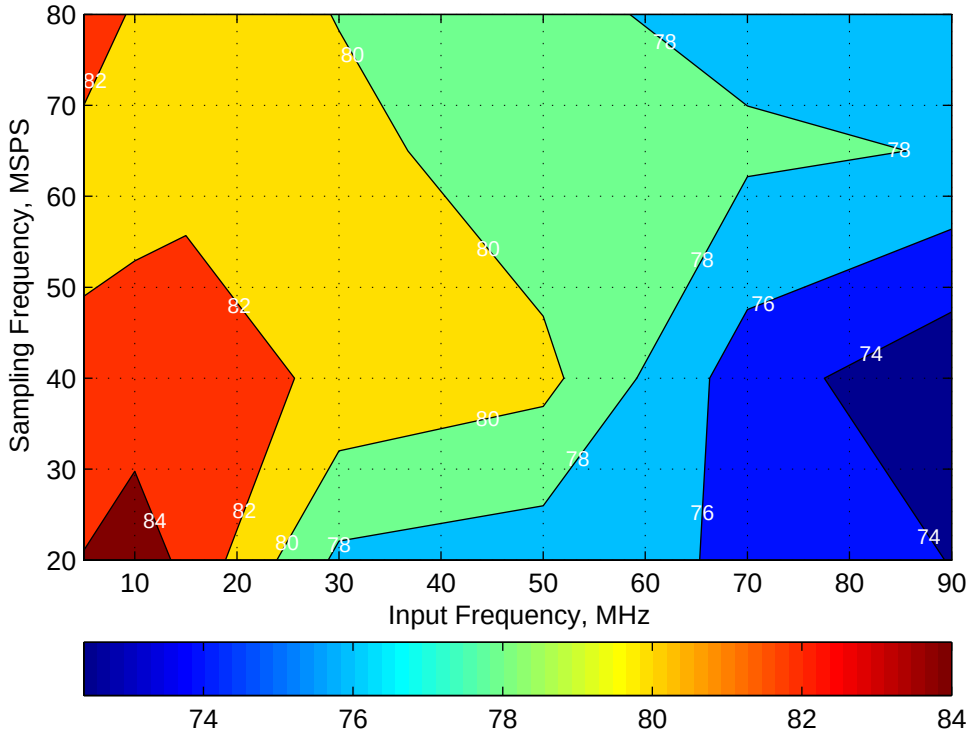


Figure 40. SPURIOUS-FREE DYNAMIC RANGE vs INPUT AND SAMPLING FREQUENCIES

TYPICAL CHARACTERISTICS: General (4-Channel, 10-Bit, Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 200 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

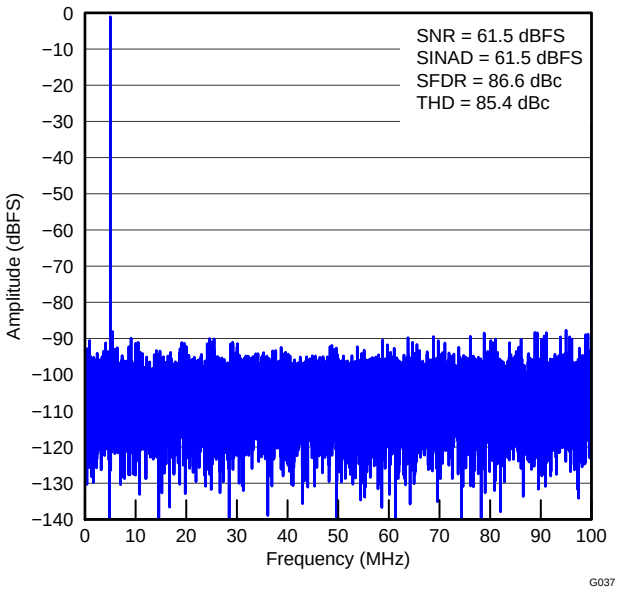


Figure 41. FFT FOR 5-MHz INPUT SIGNAL

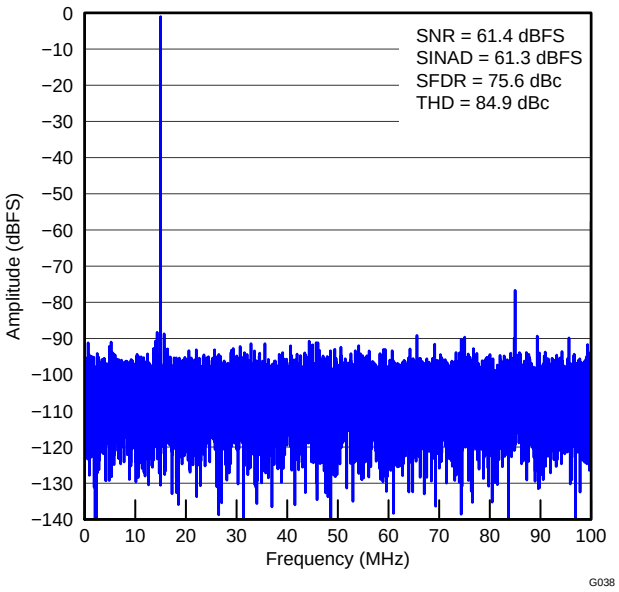


Figure 42. FFT FOR 15-MHz INPUT SIGNAL

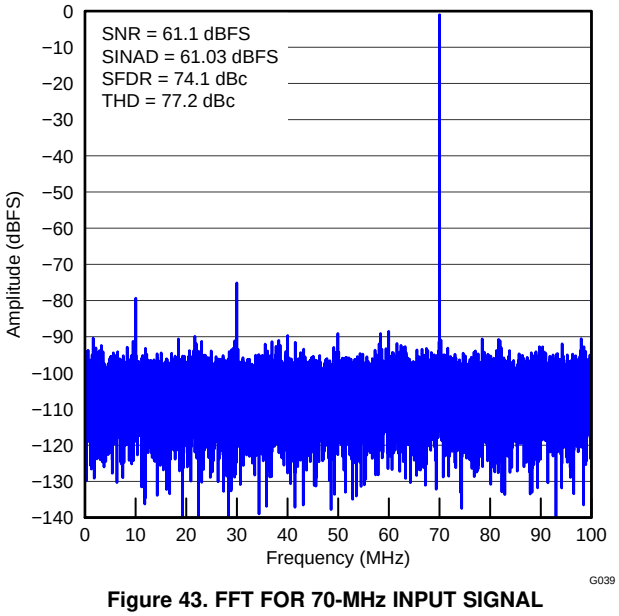


Figure 43. FFT FOR 70-MHz INPUT SIGNAL

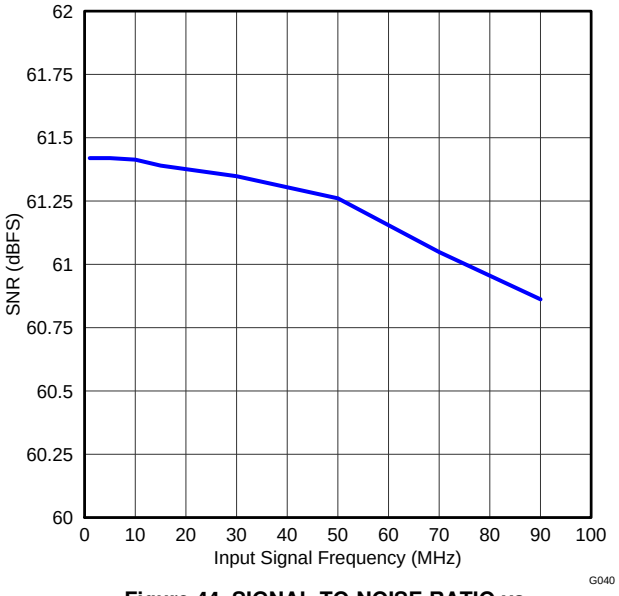


Figure 44. SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL FREQUENCY

TYPICAL CHARACTERISTICS: General (4-Channel, 10-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 200 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

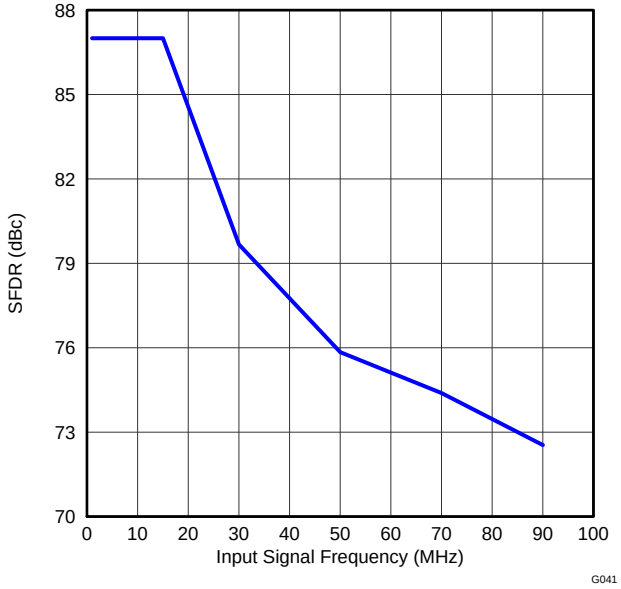


Figure 45. SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY

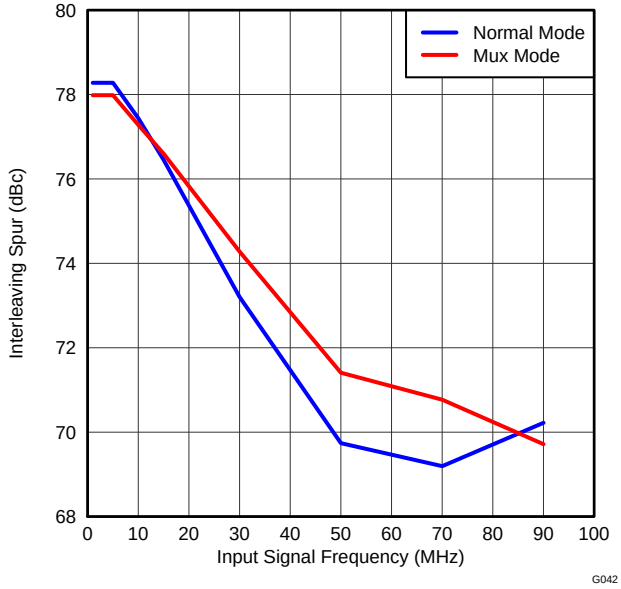


Figure 46. INTERLEAVING SPUR (f_S / 2 – f_{IN}) vs INPUT SIGNAL FREQUENCY

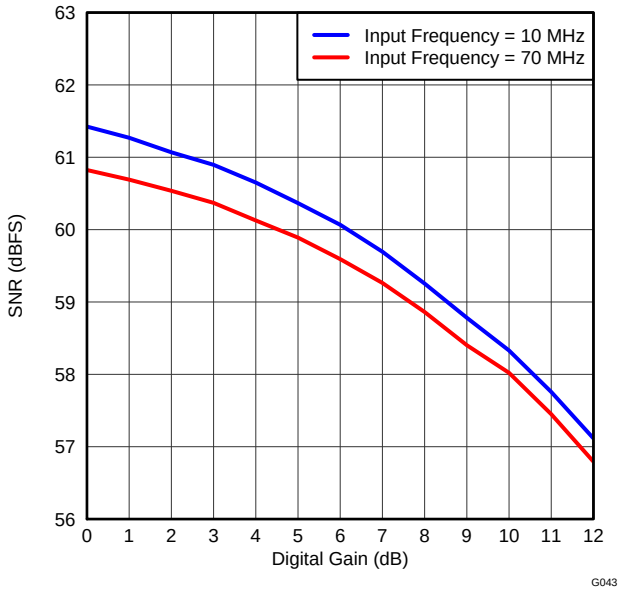


Figure 47. SIGNAL-TO-NOISE RATIO vs DIGITAL GAIN

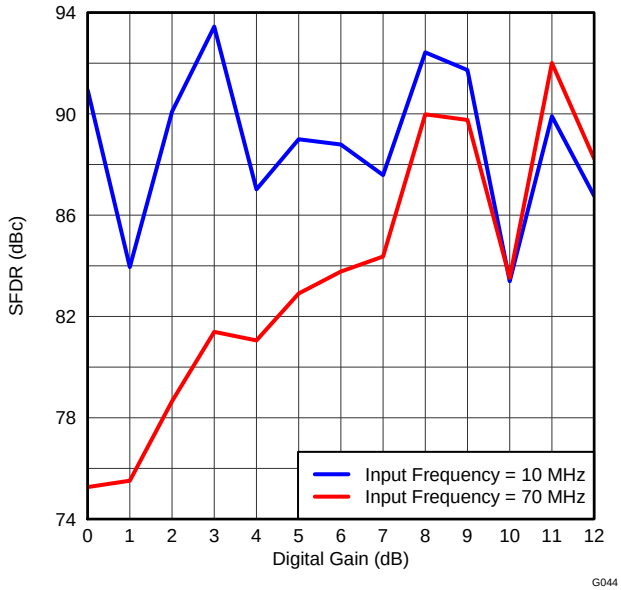


Figure 48. SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL GAIN

TYPICAL CHARACTERISTICS: General (4-Channel, 10-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 200 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

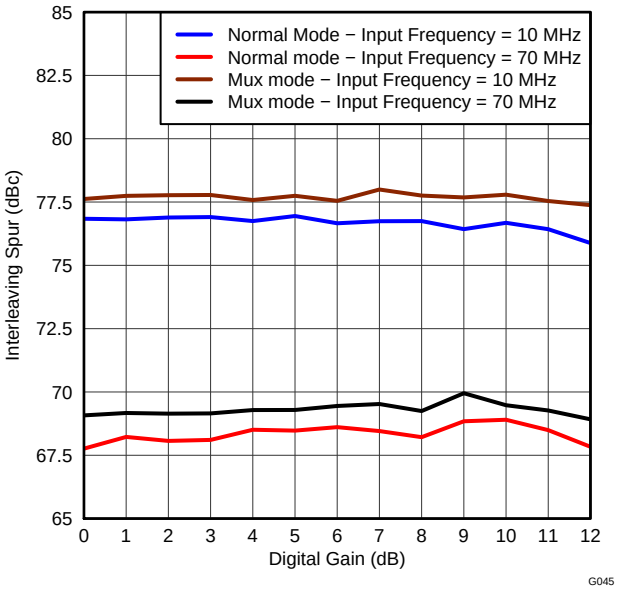


Figure 49. INTERLEAVING SPUR (f_S / 2 – f_{IN}) vs DIGITAL GAIN

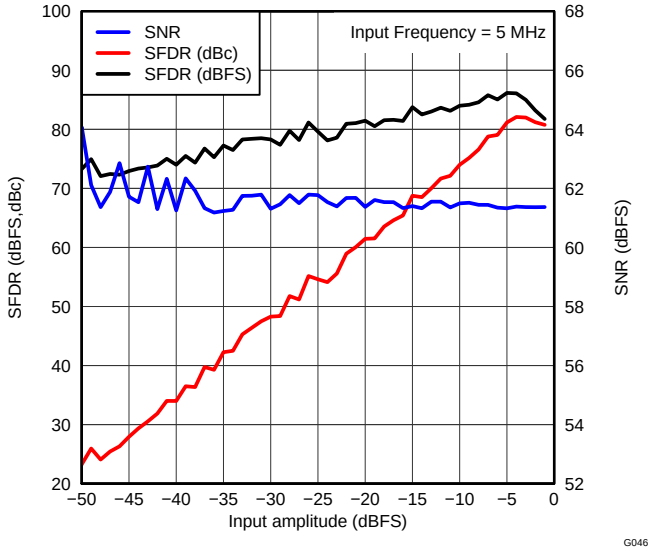


Figure 50. PERFORMANCE vs INPUT AMPLITUDE

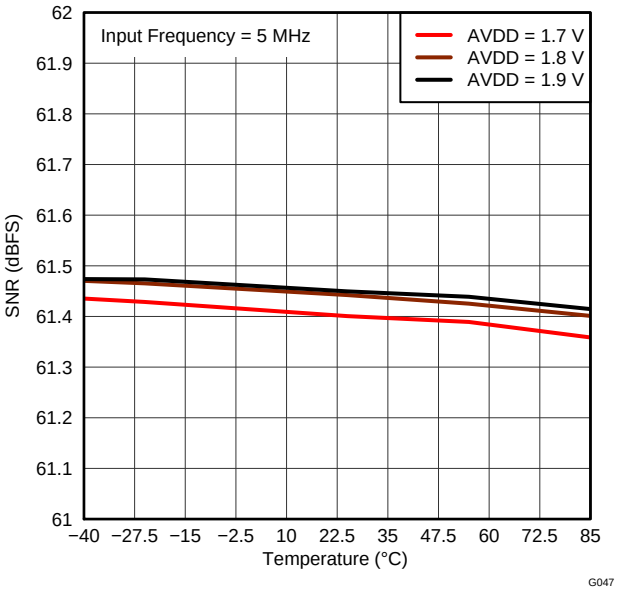


Figure 51. SIGNAL-TO-NOISE RATIO vs AVDD AND TEMPERATURE

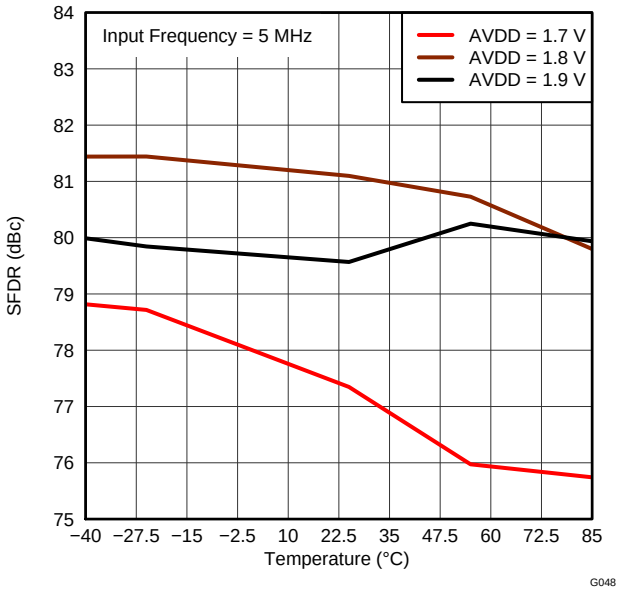


Figure 52. SPURIOUS-FREE DYNAMIC RANGE vs AVDD AND TEMPERATURE

TYPICAL CHARACTERISTICS: General (4-Channel, 10-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 200 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

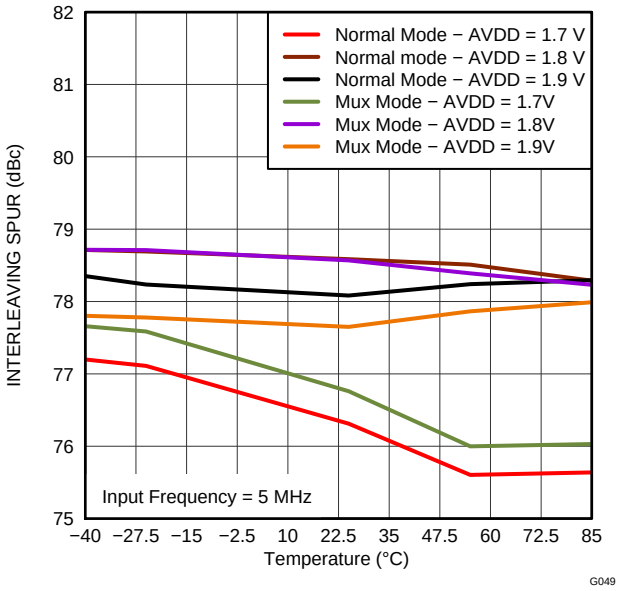


Figure 53. INTERLEAVING SPUR (f_S / 2 – f_{IN}) vs AVDD AND TEMPERATURE

TYPICAL CHARACTERISTICS: Power Consumption (4-Channel, 10-Bit, Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

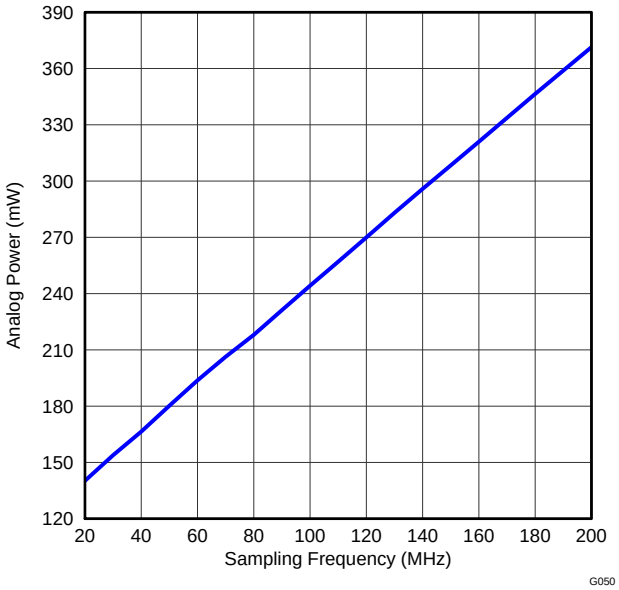


Figure 54. ANALOG SUPPLY POWER

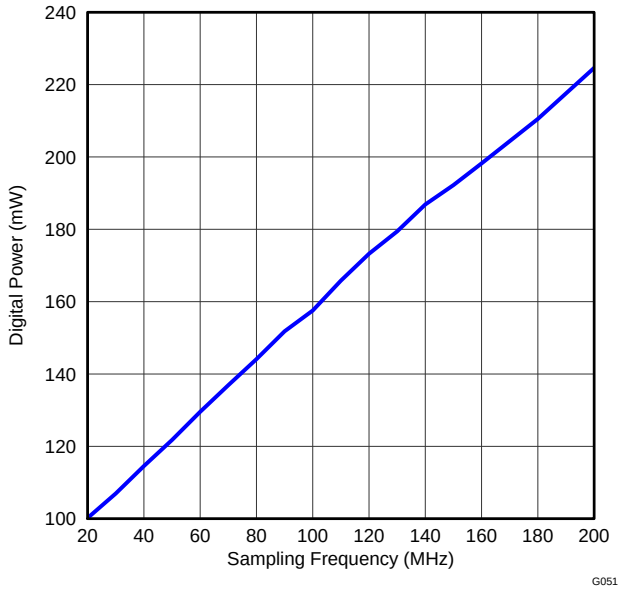


Figure 55. DIGITAL SUPPLY POWER

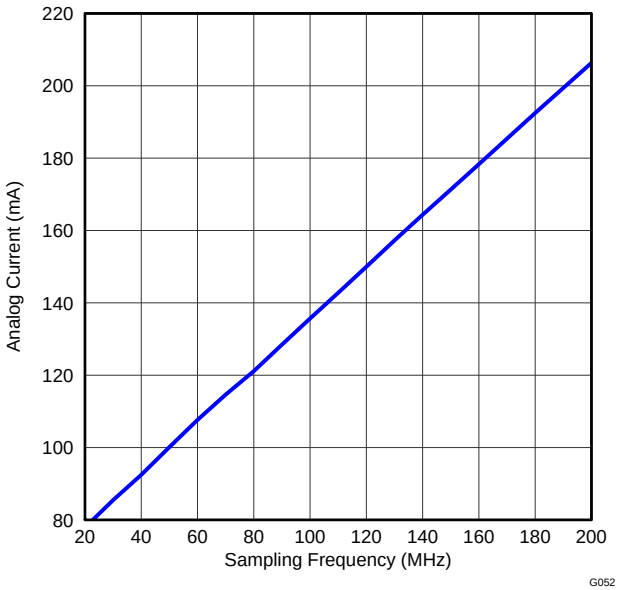


Figure 56. ANALOG SUPPLY CURRENT

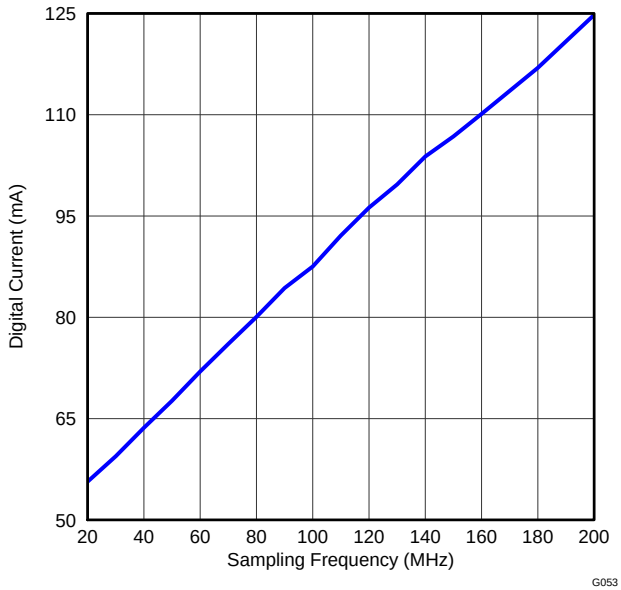


Figure 57. DIGITAL SUPPLY CURRENT

TYPICAL CHARACTERISTICS:
Power Consumption (4-Channel, 10-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

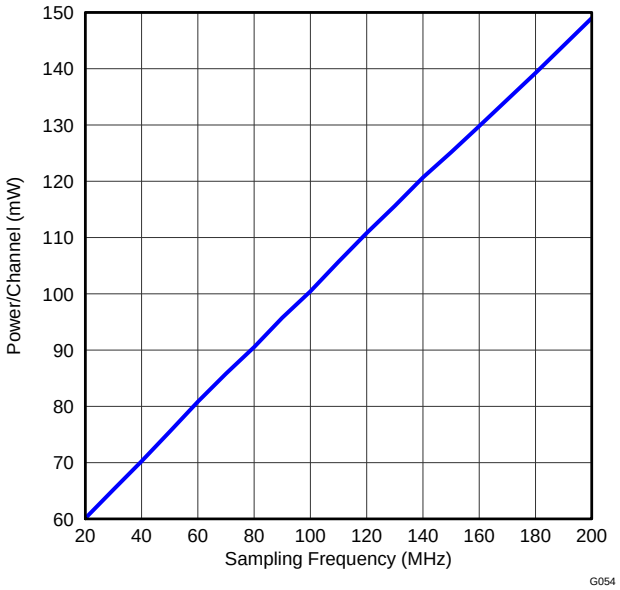


Figure 58. TOTAL POWER PER CHANNEL

TYPICAL CHARACTERISTICS: Contour (4-Channel, 10-Bit, Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

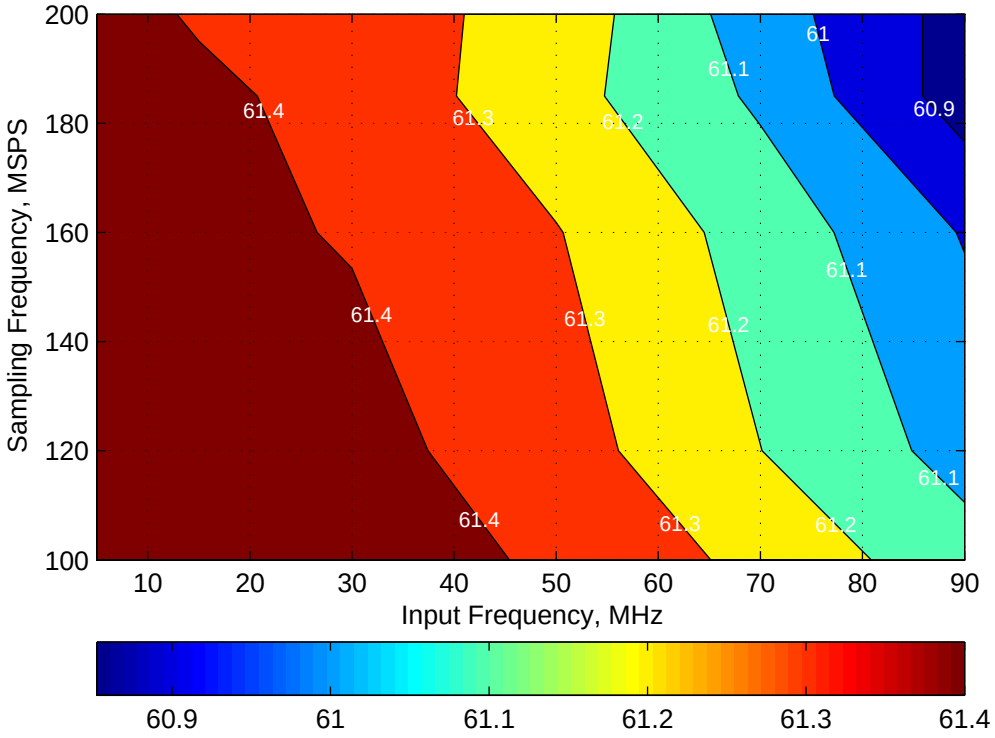


Figure 59. SIGNAL-TO-NOISE RATIO vs INPUT AND SAMPLING FREQUENCIES

TYPICAL CHARACTERISTICS: Contour (4-Channel, 10-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

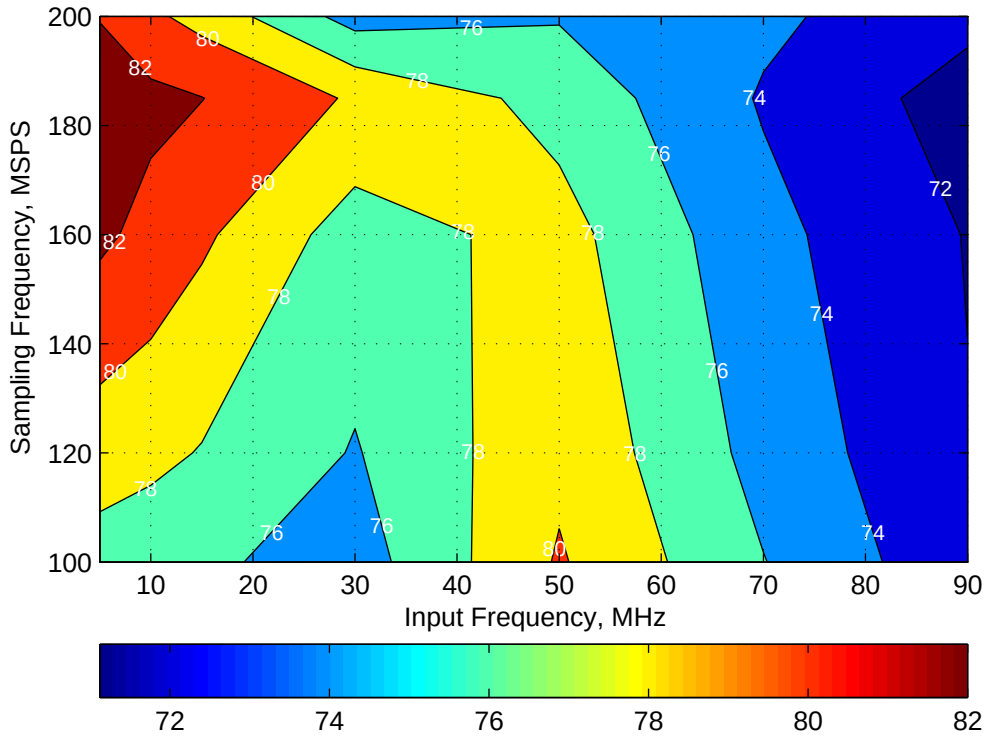


Figure 60. SPURIOUS-FREE DYNAMIC RANGE vs INPUT AND SAMPLING FREQUENCIES

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 160 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

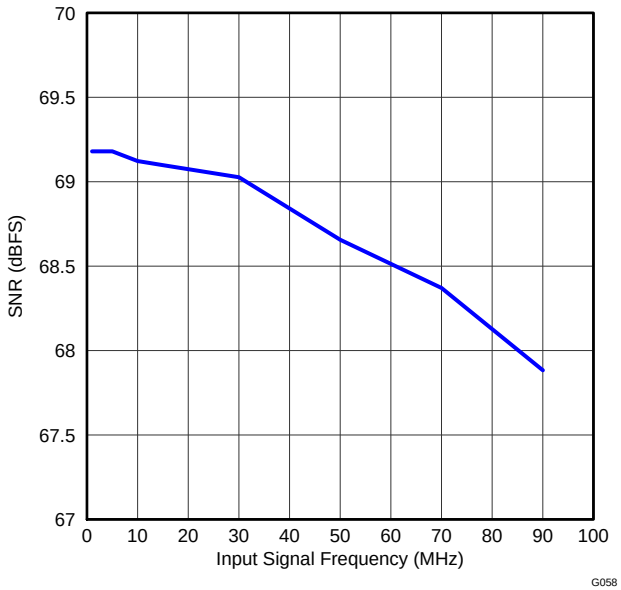


Figure 61. SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL FREQUENCY

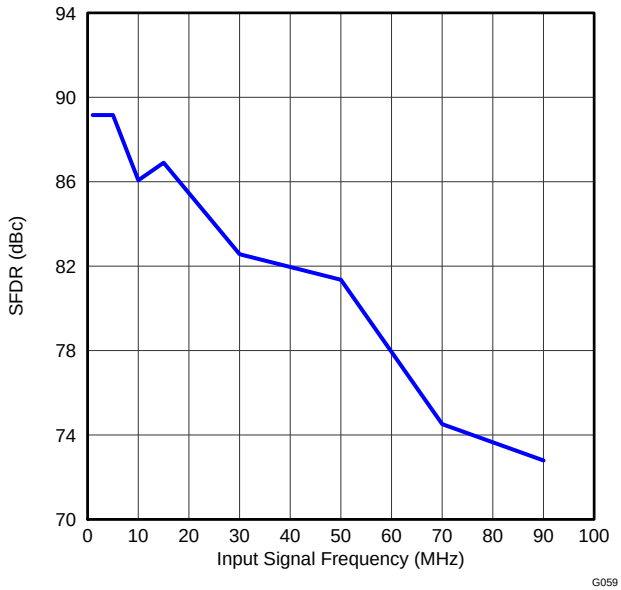


Figure 62. SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY

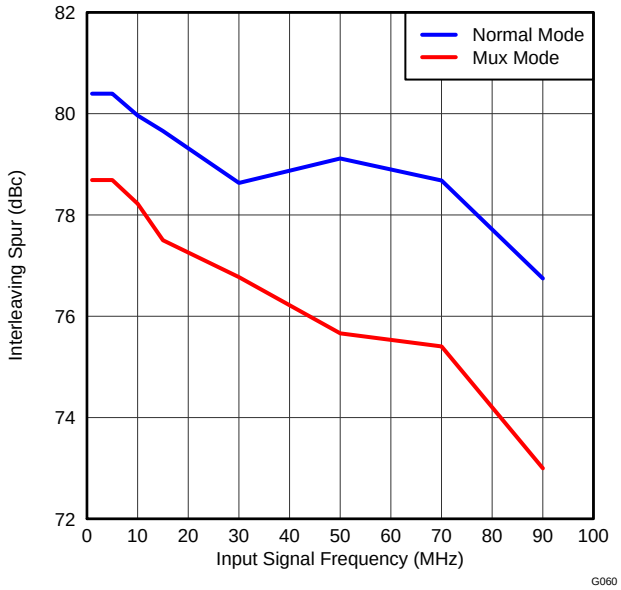


Figure 63. INTERLEAVING SPUR (f_S / 2 – f_{IN}) vs INPUT SIGNAL FREQUENCY

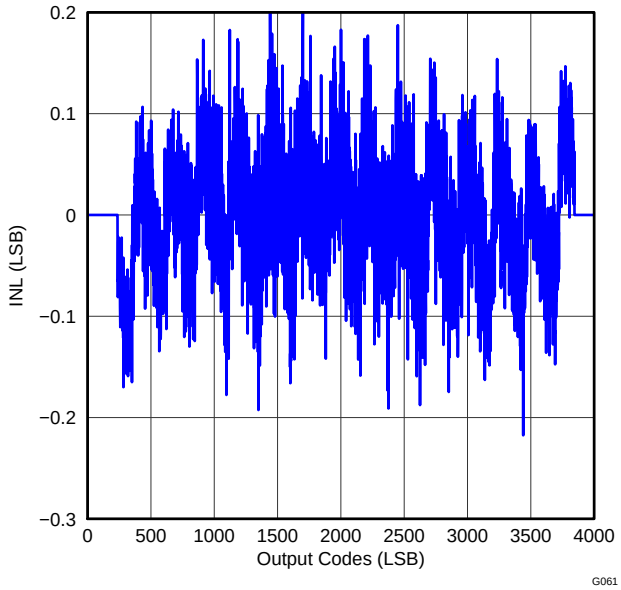


Figure 64. INTEGRAL NONLINEARITY

TYPICAL CHARACTERISTICS: General (8-Channel, 12-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, input clock frequency = 160 MSPS, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

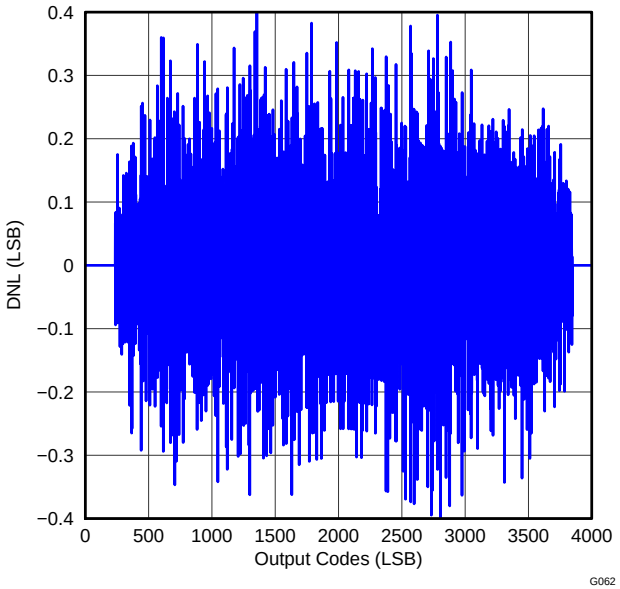


Figure 65. DEFERENTIAL NONLINEARITY

TYPICAL CHARACTERISTICS: Power Consumption (8-Channel, 12-Bit, Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

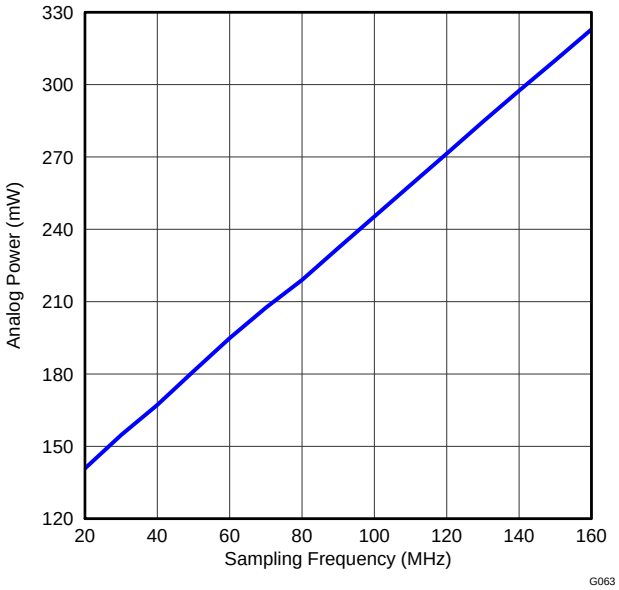


Figure 66. ANALOG SUPPLY POWER

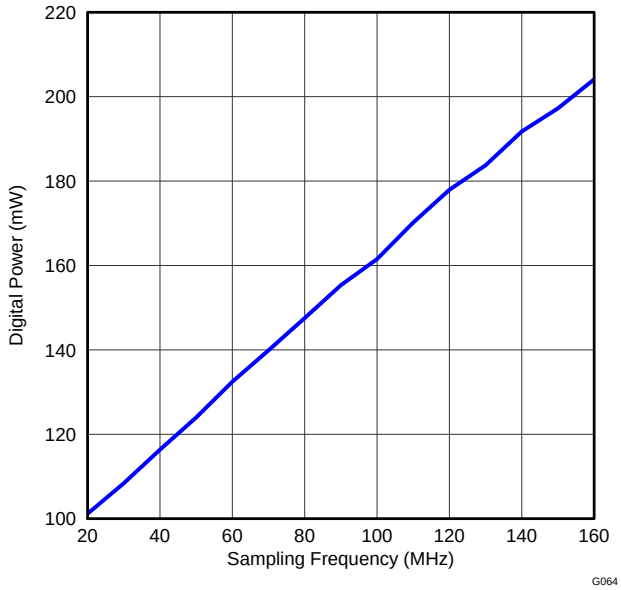


Figure 67. DIGITAL SUPPLY POWER

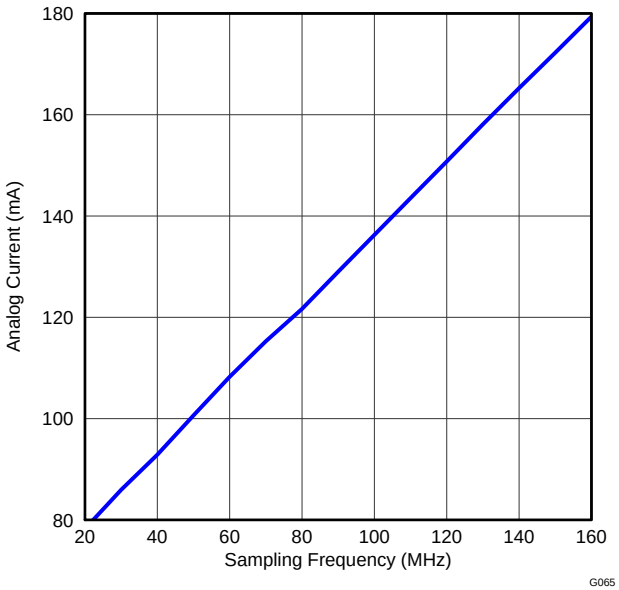


Figure 68. ANALOG SUPPLY CURRENT

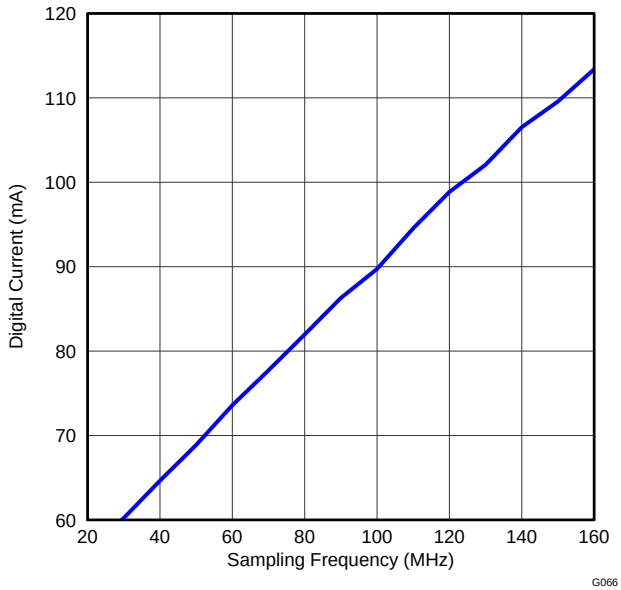


Figure 69. DIGITAL SUPPLY CURRENT

TYPICAL CHARACTERISTICS:
Power Consumption (8-Channel, 12-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

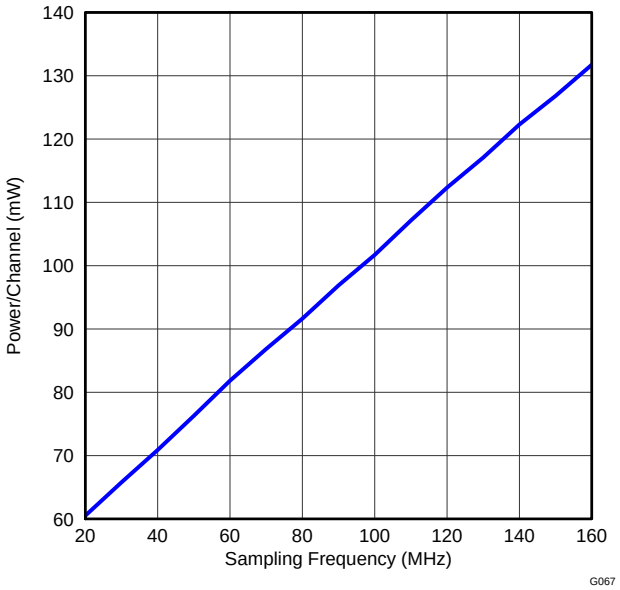


Figure 70. TOTAL POWER PER CHANNEL

TYPICAL CHARACTERISTICS: Contour (8-Channel, 12-Bit, Interleaving Mode)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

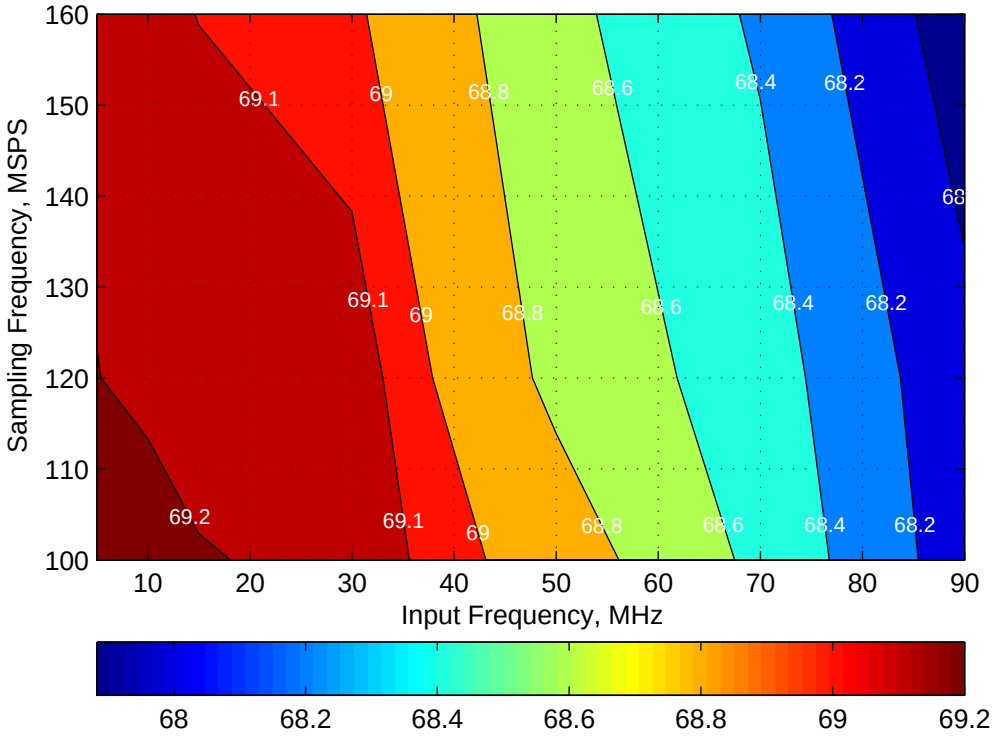


Figure 71. SIGNAL-TO-NOISE RATIO vs INPUT AND SAMPLING FREQUENCIES

TYPICAL CHARACTERISTICS: Contour (8-Channel, 12-Bit, Interleaving Mode) (continued)

Typical values are at T_A = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted.

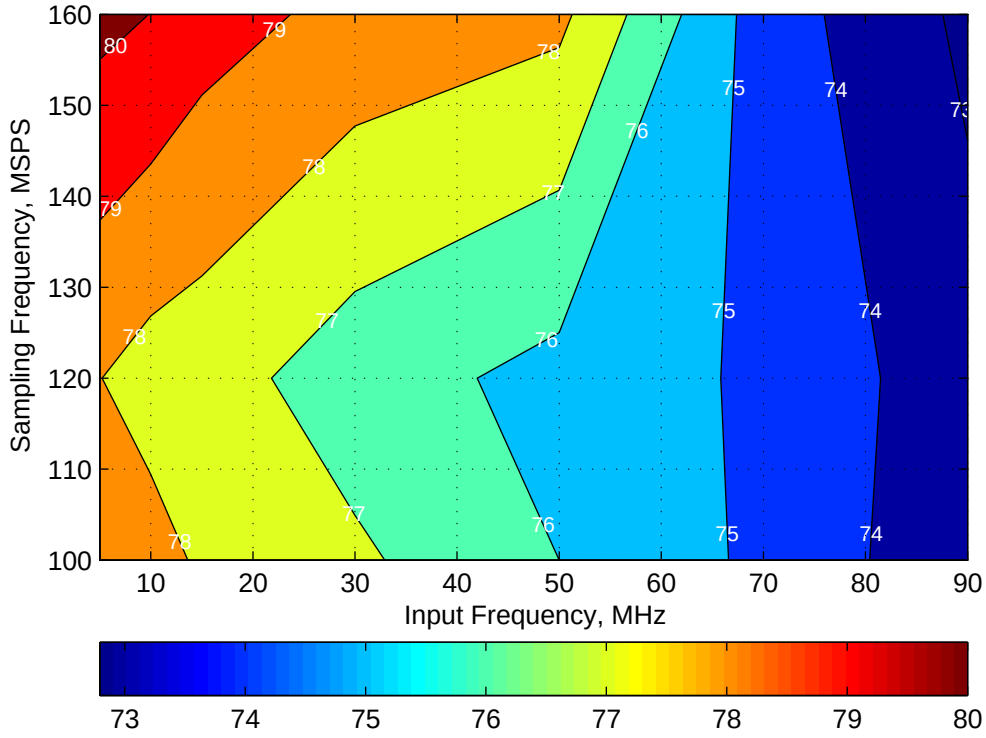


Figure 72. SPURIOUS-FREE DYNAMIC RANGE vs INPUT AND SAMPLING FREQUENCIES

DEVICE CONFIGURATION

SERIAL INTERFACE

The device has a set of internal registers that can be accessed by the serial interface formed by the $\overline{CS}$ (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins.

Register Initialization

After power-up, the internal registers must be initialized to default values. This initialization can be accomplished in one of two ways:

1. Either through a hardware reset by applying a low pulse on the $\overline{RESET}$ pin (of widths greater than 50 ns), see Figure 74; or
2. By applying a software reset. When using the serial interface, set the RST bit (register 00h, bit D0) high. This setting initializes the internal registers to default values and then self-resets the RST bit low. In this case, the $\overline{RESET}$ pin is kept high (inactive).

Reset Timing

Figure 73 shows a timing diagram for the reset function.

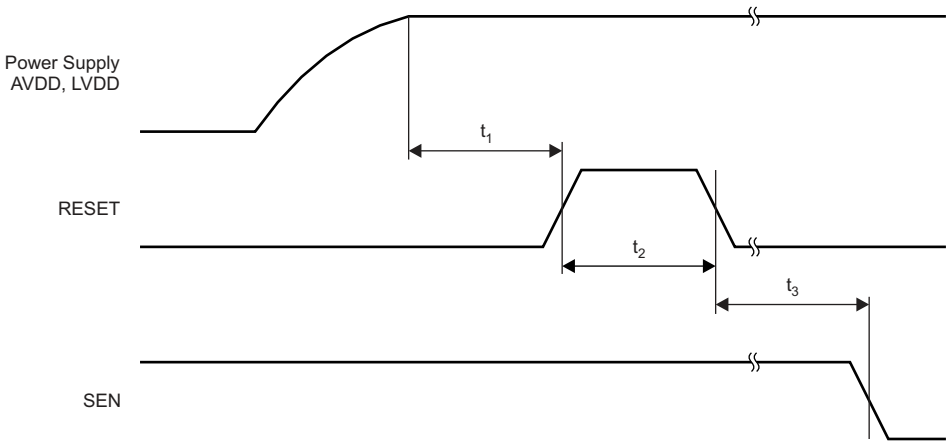


Figure 73. Reset Timing Diagram

Table 6. Timing Characteristics for Figure 73(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and LVDD power-up to active $\overline{RESET}$ pulse		1		ms
t_2	Reset pulse width	Pulse width of active $\overline{RESET}$ signal	50			ns
t_3	Register write delay	Delay from $\overline{RESET}$ disable to $\overline{CS}$ active		100		ns

(1) Typical values are at T_A = +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.
(2) A low pulse on the $\overline{RESET}$ pin is required when initialization is done via a hardware reset.

Serial Interface Write Operation

Serial shifting of bits into the device is enabled when $\overline{CS}$ is low. Serial data (on the SDATA pin) are latched at every SCLK rising edge when $\overline{CS}$ is active (low). Serial data are loaded into the register at every 24th SCLK rising edge when $\overline{CS}$ is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored (the excess bits being the last bits clocked). Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining 16 bits are the register data.

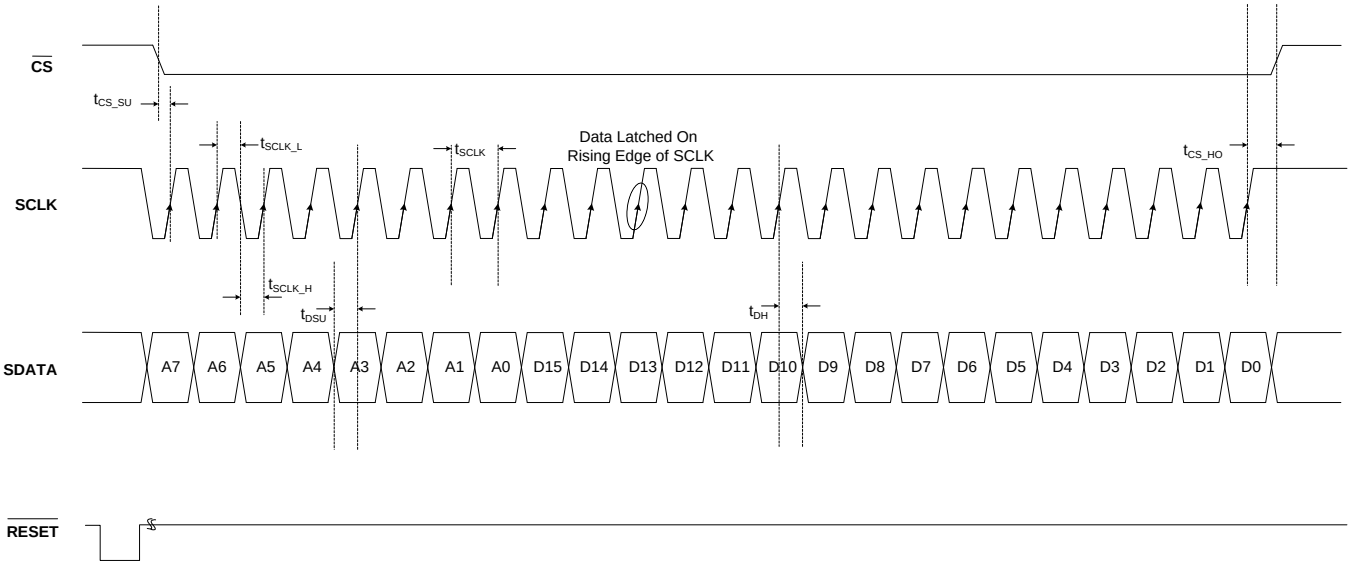


Figure 74. Serial Interface Write Timing Diagram

Table 7. Timing Characteristics for Figure 74 and Figure 76(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SCLK}	SCLK period	50			ns
t_{SCLK_H}	SCLK high time	20			ns
t_{SCLK_L}	SCLK low time	20			ns
t_{DSU}	SDATA setup time	25			ns
t_{DHO}	SDATA hold time	25			ns
t_{CS_SU}	$\overline{CS}$ fall to SCLK rise	25			ns
t_{CS_HO}	Time between last SCLK rising edge to $\overline{CS}$ rising edge	25			ns
t_{OUT_DV}(2)	Delay from SCLK falling edge to SDOUT valid	15	19	23	ns

(1) Typical values are at T_A = +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.
(2) See Figure 76.

Serial Interface Read Operation

The device includes a mode where the contents of the internal registers can be read back on the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

By default, the SDOUT pin is in 3-state after a device power-up or reset. When the readout mode is enabled using the EN_READOUT register bit, SDOUT serially outputs the contents of the selected register. The following steps describe how to achieve this functionality:

1. Set the EN_READOUT register bit to '1'; see Figure 75(a). This setting puts the device in serial readout mode. This mode prevents any further writes to the internal registers, *except* for at register 01h. Note that the EN_READOUT bit is also located in register 01h. The device can exit readout mode by setting the EN_READOUT bit to '0'. Note that only the contents of register 01h are unable to be read in register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read.
3. The device serially outputs the contents (D[15:0]) of the selected register on the SDOUT pin; see Figure 75(b).
4. The external controller can latch the contents at the SCLK rising edge.

To exit serial readout mode, reset the EN_READOUT register bit to '0', which enables writes to all device registers. At this point, the SDOUT pin is in 3-state. A detailed timing diagram for the serial readout mode is shown in Figure 76.

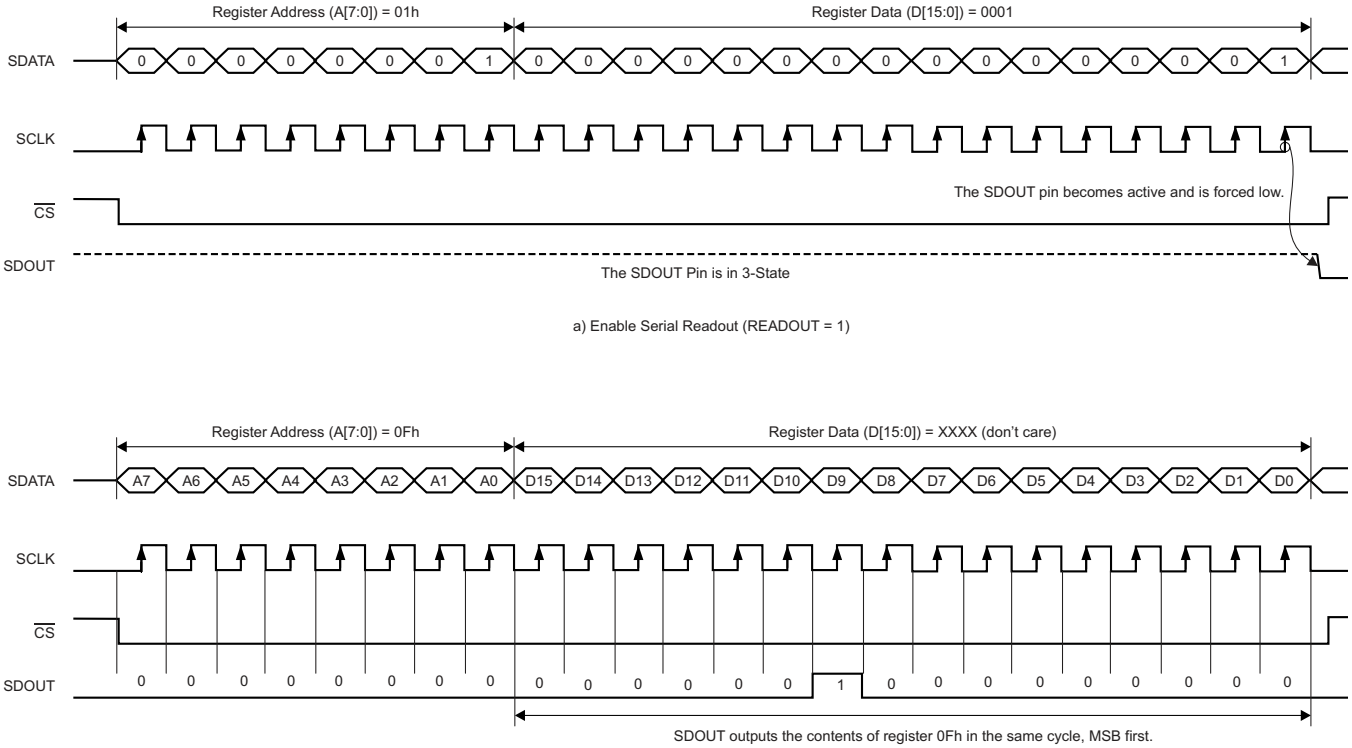


Figure 75. Serial Readout Functional Diagram

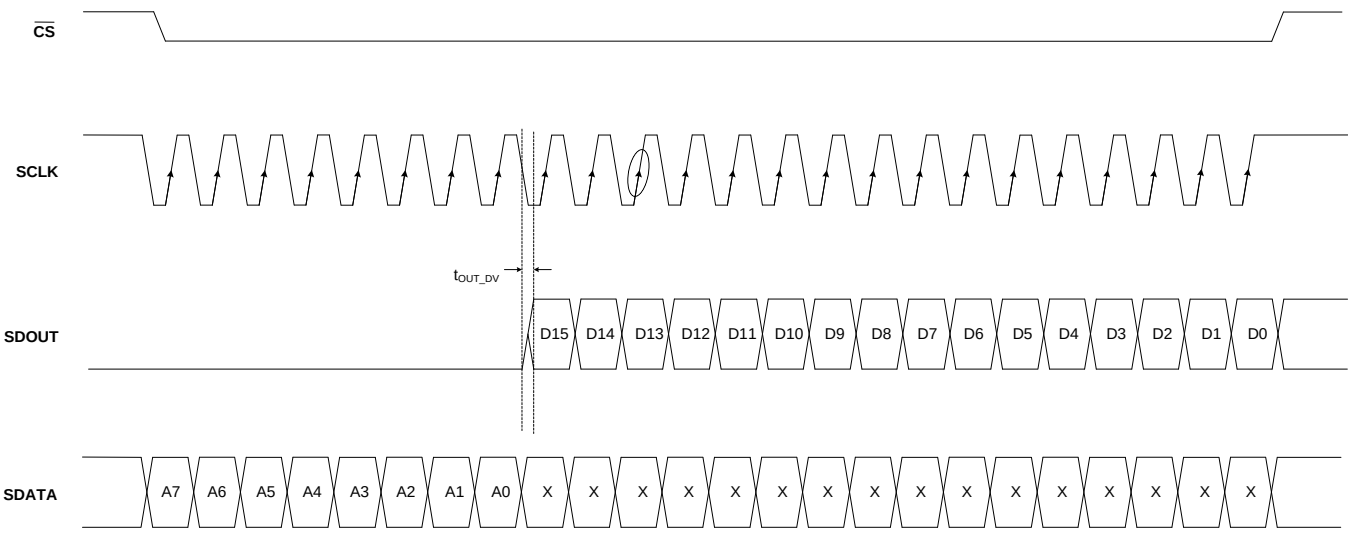


Figure 76. Serial Interface Read Timing Diagram

SERIAL INTERFACE REGISTERS MAP

Table 8 lists the ADS5296A registers.

Table 8. Register Map

REGISTER ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RST(1)
01	0	0	0	0	0	0	0	0	0	0	0	EN_HIGH_ ADDRS	0	0	0	EN_ READOUT
07	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_MUX_R EG	EN_INTER LEAVE
0A	RAMP_PAT_RESET_VAL															
0F	0	0	0	0	0	PDN_PIN_ CFG	PDN_ COMPLETE	PDN_ PARTIAL	PDN_CH[8:1]							
14	0	0	0	0	0	0	0	0	LFNS_CH[8:1]							
1C	0	EN_FRAME _PAT	0	0	ADCLKOUT[11:0]											
23	PRBS_SEED[15:0]															
24	PRBS_SEED[22:16]							0	INVERT_CH[8:1]							
25	TP_HARD_ SYNC	PRBS_ SEED_ FROM_REG	PRBS_ MODE_2	PRBS_ TP_EN	0	0	0	TP_SOFT_ SYNC	0	TEST_PATT[2:0]			BITS_CUSTOM2[11:10]		BITS_CUSTOM1[11:10]	
26	BITS_CUSTOM1[9:0]										0	0	0	0	0	0
27	BITS_CUSTOM2[9:0]										0	0	0	0	0	0
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GLOBAL_E N_ FILTER	EN_ CHANNEL_ AVG
2A	GAIN_CH4[3:0]				GAIN_CH3[3:0]				GAIN_CH2[3:0]				GAIN_CH1[3:0]			
2B	GAIN_CH5[3:0]				GAIN_CH6[3:0]				GAIN_CH7[3:0]				GAIN_CH8[3:0]			
2C	0	0	0	0	0	AVG_OUT4[1:0]		0	AVG_OUT3[1:0]		0	AVG_OUT2[1:0]		0	AVG_OUT1[1:0]	
2D	0	0	0	0	0	AVG_OUT8[1:0]		0	AVG_OUT7[1:0]		0	AVG_OUT6[1:0]		0	AVG_OUT5[1:0]	

(1) Shaded cells indicate used bits.

Table 8. Register Map (continued)

REGISTER ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2E	0	HPF_EN_CH1	HPF_CORNER_CH1[3:0]				FILTER_TYPE_CH1[2:0]			DEC_RATE_CH1			0	SEL_ODD_TAP_CH1	0	USE_FILTER_CH1
2F	0	HPF_EN_CH2	HPF_CORNER_CH2[3:0]				FILTER_TYPE_CH2[2:0]			DEC_RATE_CH2			0	SEL_ODD_TAP_CH2	0	USE_FILTER_CH2
30	0	HPF_EN_CH3	HPF_CORNER_CH3[3:0]				FILTER_TYPE_CH3[2:0]			DEC_RATE_CH3			0	SEL_ODD_TAP_CH3	0	USE_FILTER_CH3
31	0	HPF_EN_CH4	HPF_CORNER_CH4[3:0]				FILTER_TYPE_CH4[2:0]			DEC_RATE_CH4			0	SEL_ODD_TAP_CH4	0	USE_FILTER_CH4
32	0	HPF_EN_CH5	HPF_CORNER_CH5[3:0]				FILTER_TYPE_CH5[2:0]			DEC_RATE_CH5			0	SEL_ODD_TAP_CH5	0	USE_FILTER_CH5
33	0	HPF_EN_CH6	HPF_CORNER_CH6[3:0]				FILTER_TYPE_CH6[2:0]			DEC_RATE_CH6			0	SEL_ODD_TAP_CH6	0	USE_FILTER_CH6
34	0	HPF_EN_CH7	HPF_CORNER_CH7[3:0]				FILTER_TYPE_CH7[2:0]			DEC_RATE_CH7			0	SEL_ODD_TAP_CH7	0	USE_FILTER_CH7
35	0	HPF_EN_CH8	HPF_CORNER_CH8[3:0]				FILTER_TYPE_CH8[2:0]			DEC_RATE_CH8			0	SEL_ODD_TAP_CH8	0	USE_FILTER_CH8
38	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DATA_RATE[1:0]	
40	ENABLE 40								ODD_EVEN_SEL							
42	EN_PHASE DDR	0	0	0	0	0	0	0	0	PHASE_DDR1	PHASE_DDR0	0	0	0	0	0
45	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PAT_DESKEW_SYNC[1:0]	
46	ENABLE 46	0	FALL_SDR	0	EN_BIT_SER				0	0	0	EN_SDR	EN_MSB_FIRST	BTC_MODE	0	0
50	ENABLE 50	0	0	0	MAP_Ch1234_to_OUT2				0	0	0	0	MAP_Ch1234_to_OUT1			
51	ENABLE 51	0	0	0	0	0	0	0	MAP_Ch1234_to_OUT3				0	0	0	0
52	ENABLE 52	0	0	0	0	0	0	0	0	0	0	0	MAP_Ch1234_to_OUT4			
53	ENABLE 53	0	0	0	0	0	0	0	MAP_Ch5678_to_OUT5				0	0	0	0
54	ENABLE 54	0	0	0	MAP_Ch5678_to_OUT7								MAP_Ch5678_to_OUT6			
55	ENABLE 55	0	0	0	0	0	0	0	MAP_Ch5678_to_OUT8				0	0	0	0

Table 8. Register Map (continued)

REGISTER ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
5A to 65	EN_CUSTOM_FILT_CH1	0	0	0	COEFF*n*_SET_CH1[2]											
66 to 71	EN_CUSTOM_FILT_CH2	0	0	0	COEFF*n*_SET_CH2[2]											
72 to 7D	EN_CUSTOM_FILT_CH3	0	0	0	COEFF*n*_SET_CH3[2]											
7E to 89	EN_CUSTOM_FILT_CH4	0	0	0	COEFF*n*_SET_CH4[2]											
8A to 95	EN_CUSTOM_FILT_CH5	0	0	0	COEFF*n*_SET_CH5[2]											
96 to A1	EN_CUSTOM_FILT_CH6	0	0	0	COEFF*n*_SET_CH6[2]											
A2 to AD	EN_CUSTOM_FILT_CH7	0	0	0	COEFF*n*_SET_CH7[2]											
AE to B9	EN_CUSTOM_FILT_CH8	0	0	0	COEFF*n*_SET_CH8[2]											
BE	EN_LVDS_PROG	0	0	0	0	0	DELAY_DATA_R			DELAY_LCLK_R			DELAY_DATA_F		DELAY_LCLK_F	
F0	EN_EXT_REF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(2) n = 0 to 11.

DESCRIPTION OF SERIAL INTERFACE REGISTERS

Table 9. Register 00h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	RST

All bits default to '0' after reset.

Bits D[15:1] **Must write '0'**

Bit D0 **RST**

0 = Normal operation (default)
1 = Self-clearing software RESET; after reset, this bit is set to '0'

Table 10. Register 01h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	EN_HIGH_ ADDRS	0	0	0	EN_READOUT

All bits default to '0' after reset.

Bits D[15:5] **Must write '0'**

Bit D4 **EN_HIGH_ADDRS**

0 = Access to register F0h disabled (default)
1 = Access to register F0h enabled

Bits D[3:1] **Must write '0'**

Bit D0 **EN_READOUT**

0 = Normal operation (default)
1 = READOUT of registers mode using the SDOUT pin enabled

Table 11. Register 07h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	EN_MUX_REG	EN_ INTERLEAVE

All bits default to '0' after reset.

Bits D[15:2] **Must write '0'**

Bit D1 **EN_MUX_REG**

Enables mux mode interleaving using register bit.
0 = Enables mux mode interleaving using the ODD_EVEN_SEL register bits (default)
1 = Enables mux mode interleaving using the INTERLEAVE_MUX pin.
For more details on this bit, see the *Interleaving Mode* section.

Bit D0 **EN_INTERLEAVE**

Enables interleaving of adjacent channel pairs.
0 = Interleaving disabled (default)
1 = Interleaving enabled
For more details on this bit, see the *Interleaving Mode* section.

Table 12. Register 0Ah

D15	D14	D13	D12	D11	D10	D9	D8
RAMP_PAT_RESET_VAL							
D7	D6	D5	D4	D3	D2	D1	D0
RAMP_PAT_RESET_VAL							

All bits default to '0' after reset.

Bits D[15:0] **RAMP_PAT_RESET_VAL**

The starting value of the digital ramp test pattern can be programmed using these register bits. By default, the starting value is 0000h after reset.

Table 13. Register 0Fh

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	PDN_PIN_CFG	PDN_ COMPLETE	PDN_PARTIAL
D7	D6	D5	D4	D3	D2	D1	D0
PDN_CH[8:1]							

All bits default to '0' after reset.

Bits D[15:11] **Must write '0'**

Bit D10 **PDN_PIN_CFG**

0 = PD pin configured for complete power-down mode
1 = PD pin configured for partial power-down mode

Bit D9 **PDN_COMPLETE**

0 = Normal operation
1 = Register mode for complete power-down; slow recovery from power-down

Bit D8 **PDN_PARTIAL**

0 = Normal operation
1 = Partial power-down mode; fast recovery from power-down

Bits D[7:0] **PDN_CH[8:1]**

0 = Normal operation
1 = Individual channel ADC power-down mode

Table 14. Register 14h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
LFNS_CH[8:1]							

All bits default to '0' after reset.

Bits D[15:8] **Must write '0'**

Bits D[7:0] **LFNS_CH[8:1]**

0 = Low-frequency noise suppression (LFNS) mode disabled (default)
1 = LFNS mode enabled for individual channels

Table 15. Register 1Ch

D15	D14	D13	D12	D11	D10	D9	D8
0	EN_FRAME_PAT	0	0	ADCLKOUT[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
ADCLKOUT[11:0]							

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **EN_FRAME_PAT**

0 = Normal operation on frame clock (default)
1 = Enables output frame clock to be programmed through a pattern specified by the ADCCLKOUT register bits

Bits D[13:12] **Must write '0'**

Bits D[11:0] **ADCLKOUT[11:0]**

These bits create the 12-bit pattern for the frame clock on the ADCLKP, ADCLKN pins.

Table 16. Register 23h

D15	D14	D13	D12	D11	D10	D9	D8
PRBS_SEED[15:0]							
D7	D6	D5	D4	D3	D2	D1	D0
PRBS_SEED[15:0]							

All bits default to '0' after reset.

Bits D[15:0] **PRBS_SEED[15:0]**

These bits are the lower 16 bits of the PRBS pattern starting seed value.

The starting seed value of the PRBS test pattern can be specified using these register bits.

Table 17. Register 24h

D15	D14	D13	D12	D11	D10	D9	D8
PRBS_SEED[22:16]							0
D7	D6	D5	D4	D3	D2	D1	D0
INVERT_CH[8:1]							

All bits default to '0' after reset.

Bits D[15:9] **PRBS_SEED[22:16]**

These bits are the seven upper bits of the PRBS seed starting value.

Bit D8 **Must write '0'**

Bits D[7:0] **INVERT_CH[8:1]**

0 = Normal configuration
Normally, the IN_p pin represents the positive analog input pin and IN_n represents the complementary negative input.

1 = The polarity of the analog input pins is electrically swapped
Setting the INVERT_CH[8:1] bits causes the inputs to be swapped. IN_n now represents the positive input and IN_p represents the negative input.

Table 18. Register 25h

D15	D14	D13	D12	D11	D10	D9	D8
TP_HARD_SYNC	PRBS_SEED_FROM_REG	PRBS_MODE_2	PRBS_TP_EN	0	0	0	TP_SOFT_SYNC
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	TEST_PATT[2:0]			BITS_CUSTOM2[11:10]		BITS_CUSTOM1[11:10]	

All bits default to '0' after reset.

Bit D15 **TP_HARD_SYNC**

0 = Inactive
1 = The external SYNC feature is enabled for syncing test patterns

Bit D14 **PRBS_SEED_FROM_REG**

0 = Disabled
1 = The PRBS seed can be chosen from registers 23h and 24h

Bit D13 **PRBS_MODE_2**

The PRBS 9-bit LFSR (23-bit LFSR) is the default mode.

Bit D12 **PRBS_TP_EN**

0 = PRBS test pattern disabled
1 = PRBS test pattern enabled

Bits D[11:9] **Must write '0'**

Bit D8 **TP_SOFT_SYNC**

0 = No sync
1 = Software sync bit for the test patterns on all eight channels

Bit D7 **Must write '0'**

Bit D6 **TEST_PATT2**

0 = Normal operation
1 = A repeating full-scale ramp pattern is enabled on the outputs; ensure that bits D4 and D5 are '0'

Bit D5 **TEST_PATT1**

0 = Normal operation
1 = Enables a mode where the output toggles between two defined codes; ensure that bits D4 and D6 are '0'

Bit D4 **TEST_PATT0**

0 = Normal operation
1 = Enables a mode where the output is a constant specified code; ensure that bits D5 and D6 are '0'

Bits D[3:2] **BITS_CUSTOM2[11:10]**

These bits are the two MSBs for the second code of the dual custom patterns.

Bits D[1:0] **BITS_CUSTOM1[11:10]**

These bits are the two MSBs for the single custom pattern (and for the first code of the dual custom patterns).

Table 19. Register 26h

D15	D14	D13	D12	D11	D10	D9	D8
BITS_CUSTOM1[9:0]							
D7	D6	D5	D4	D3	D2	D1	D0
BITS_CUSTOM1[9:0]		0	0	0	0	0	0

All bits default to '0' after reset.

Bits D[15:6] **BITS_CUSTOM1[9:0]**

These bits are the 10 lower bits for the single custom pattern (and for the first code of the dual custom pattern).

Bits D[5:0] **Must write '0'**

Table 20. Register 27h

D15	D14	D13	D12	D11	D10	D9	D8
BITS_CUSTOM2[9:0]							
D7	D6	D5	D4	D3	D2	D1	D0
BITS_CUSTOM2[9:0]		0	0	0	0	0	0

All bits default to '0' after reset.

Bits D[15:6] **BITS_CUSTOM2[9:0]**

These bits are the 10 lower bits for the second code of the dual custom pattern.

Bits D[5:0] **Must write '0'**

Table 21. Register 29h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	GLOBAL_EN FILTER	EN_CHANNEL _AVG

All bits default to '0' after reset.

Bits D[15:2] **Must write '0'**

Bit D1 **GLOBAL_EN_FILTER**

0 = Global control digital filter disabled(default)
1 = Global control digital filter enabled

Bit D0 **EN_CHANNEL_AVG**

0 = Channel averaging disabled (default)
1 = Channel averaging enabled and specified by the AVG_OUT*n* register bits

Table 22. Register 2Ah

D15	D14	D13	D12	D11	D10	D9	D8
GAIN_CH4[3:0]				GAIN_CH3[3:0]			
D7	D6	D5	D4	D3	D2	D1	D0
GAIN_CH2[3:0]				GAIN_CH1[3:0]			

All bits default to '0' after reset.

Bits D[15:12] **GAIN_CH4[3:0]**

These bits set the programmable gain for channel 4.

Bits D[11:8] **GAIN_CH3[3:0]**

These bits set the programmable gain for channel 3.

Bits D[7:4] **GAIN_CH2[3:0]**

These bits set the programmable gain for channel 2.

Bits D[3:0] **GAIN_CH1[3:0]**

These bits set the programmable gain for channel 1.

Table 23. Register 2Bh

D15	D14	D13	D12	D11	D10	D9	D8
GAIN_CH5[3:0]				GAIN_CH6[3:0]			
D7	D6	D5	D4	D3	D2	D1	D0
GAIN_CH7[3:0]				GAIN_CH8[3:0]			

All bits default to '0' after reset.

Bits D[15:12] **GAIN_CH5[3:0]**

These bits set the programmable gain for channel 4.

Bits D[11:8] **GAIN_CH6[3:0]**

These bits set the programmable gain for channel 5.

Bits D[7:4] **GAIN_CH7[3:0]**

These bits set the programmable gain for channel 6.

Bits D[3:0] **GAIN_CH8[3:0]**

These bits set the programmable gain for channel 7.

Table 24. Register 2Ch

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	AVG_OUT4[1:0]		0
D7	D6	D5	D4	D3	D2	D1	D0
AVG_OUT3[1:0]		0	AVG_OUT2[1:0]		0	AVG_OUT1[1:0]	

All bits default to '0' after reset.

Bits D[15:11] **Must write '0'**

Bits D[10:9] **AVG_OUT4[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT4.

Bit D8 **Must write '0'**

Bits D[7:6] **AVG_OUT3[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT3.

Bit D5 **Must write '0'**

Bits D[4:3] **AVG_OUT2[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT2.

Bit D2 **Must write '0'**

Bits D[1:0] **AVG_OUT1[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT1.

Table 25. Register 2Dh

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	AVG_OUT8[1:0]		0

D7	D6	D5	D4	D3	D2	D1	D0
AVG_OUT7[1:0]		0	AVG_OUT6[1:0]		0	AVG_OUT5[1:0]	

All bits default to '0' after reset.

Bits D[15:11] **Must write '0'**

Bits D[10:9] **AVG_OUT8[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT8.

Bit D8 **Must write '0'**

Bits D[7:6] **AVG_OUT7[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT7.

Bit D5 **Must write '0'**

Bits D[4:3] **AVG_OUT6[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT6.

Bit D2 **Must write '0'**

Bits D[1:0] **AVG_OUT5[1:0]**

These bits set the averaging control for data transmitted on the LVDS output OUT5.

Table 26. Register 2Eh

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH1	HPF_CORNER _CH1[3:0]				FILTER_TYPE_CH1[2:0]	

D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH1[2:0]	DEC_RATE_CH1[2:0]			0	SEL_ODD_ TAP_CH1	0	USE_FILTER_ CH1

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH1**

This bit enables the HPF filter for channel 1.

Bits D[13:10] **HPF_CORNER _CH1[3:0]**

These bits program the HPF corner for channel 1.

Bits D[9:7] **FILTER_TYPE_CH1[2:0]**

These bits select the type of filter on channel 1.

Bits D[6:4] **DEC_RATE_CH1[2:0]**

These bits set the decimation factor for the filter on channel 1.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH1**

This bit enables the odd tap filter for channel 1.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH1**

This bit enables the filter for channel 1.

Table 27. Register 2Fh

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH2	HPF_CORNER _CH2[3:0]				FILTER_TYPE_CH2[2:0]	

D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH2[2:0]	DEC_RATE_CH2[2:0]			0	SEL_ODD_ TAP_CH2	0	USE_FILTER_ CH2

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH2**

This bit enables the HPF filter for channel 2.

Bits D[13:10] **HPF_CORNER _CH2[3:0]**

These bits program the HPF corner for channel 2.

Bits D[9:7] **FILTER_TYPE_CH2[2:0]**

These bits select the type of filter on channel 2.

Bits D[6:4] **DEC_RATE_CH2[2:0]**

These bits set the decimation factor for the filter on channel 2.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH2**

This bit enables the odd tap filter for channel 2.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH2**

This bit enables the filter for channel 2.

Table 28. Register 30h

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH3	HPF_CORNER _CH3[3:0]				FILTER_TYPE_CH3[2:0]	
D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH3[2:0]	DEC_RATE_CH3[2:0]			0	SEL_ODD_ TAP_CH3	0	USE_FILTER_ CH3

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH3**

This bit enables the HPF filter for channel 3.

Bits D[13:10] **HPF_CORNER _CH3[3:0]**

These bits program the HPF corner for channel 3.

Bits D[9:7] **FILTER_TYPE_CH3[2:0]**

These bits select the type of filter on channel 3.

Bits D[6:4] **DEC_RATE_CH3[2:0]**

These bits set the decimation factor for the filter on channel 3.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH3**

This bit enables the odd tap filter for channel 3.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH3**

This bit enables the filter for channel 3.

Table 29. Register 31h

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH4	HPF_CORNER _CH4[3:0]				FILTER_TYPE_CH4[2:0]	

D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH4[2:0]	DEC_RATE_CH4[2:0]			0	SEL_ODD_ TAP_CH4	0	USE_FILTER_ CH4

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH4**

This bit enables the HPF filter for channel 4.

Bits D[13:10] **HPF_CORNER _CH4[3:0]**

These bits program the HPF corner for channel 4.

Bits D[9:7] **FILTER_TYPE_CH4[2:0]**

These bits select the type of filter on channel 4.

Bits D[6:4] **DEC_RATE_CH4[2:0]**

These bits set the decimation factor for the filter on channel 4.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH4**

This bit enables the odd tap filter for channel 4.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH4**

This bit enables the filter for channel 4.

Table 30. Register 32h

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH5	HPF_CORNER _CH5[3:0]				FILTER_TYPE_CH5[2:0]	
D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH5[2:0]	DEC_RATE_CH5[2:0]			0	SEL_ODD_ TAP_CH5	0	USE_FILTER_ CH5

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH5**

This bit enables the HPF filter for channel 5.

Bits D[13:10] **HPF_CORNER _CH5[3:0]**

These bits program the HPF corner for channel 5.

Bits D[9:7] **FILTER_TYPE_CH5[2:0]**

These bits select the type of filter on channel 5.

Bits D[6:4] **DEC_RATE_CH5[2:0]**

These bits set the decimation factor for the filter on channel 5.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH5**

This bit enables the odd tap filter for channel 5.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH5**

This bit enables the filter for channel 5.

Table 31. Register 33h

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH6	HPF_CORNER _CH6[3:0]				FILTER_TYPE_CH6[2:0]	

D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH6[2:0]	DEC_RATE_CH6[2:0]			0	SEL_ODD_ TAP_CH6	0	USE_FILTER_ CH6

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH6**

This bit enables the HPF filter for channel 6.

Bits D[13:10] **HPF_CORNER _CH6[3:0]**

These bits program the HPF corner for channel 6.

Bits D[9:7] **FILTER_TYPE_CH6[2:0]**

These bits select the type of filter on channel 6.

Bits D[6:4] **DEC_RATE_CH6[2:0]**

These bits set the decimation factor for the filter on channel 6.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH6**

This bit enables the odd tap filter for channel 6.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH6**

This bit enables the filter for channel 6.

Table 32. Register 34h

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH7	HPF_CORNER _CH7[3:0]				FILTER_TYPE_CH7[2:0]	

D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH7[2:0]	DEC_RATE_CH7[2:0]			0	SEL_ODD_ TAP_CH7	0	USE_FILTER_ CH7

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH7**

This bit enables the HPF filter for channel 7.

Bits D[13:10] **HPF_CORNER _CH7[3:0]**

These bits program the HPF corner for channel 7.

Bits D[9:7] **FILTER_TYPE_CH7[2:0]**

These bits select the type of filter on channel 7.

Bits D[6:4] **DEC_RATE_CH7[2:0]**

These bits set the decimation factor for the filter on channel 7.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH7**

This bit enables the odd tap filter for channel 7.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH7**

This bit enables the filter for channel 7.

Table 33. Register 35h

D15	D14	D13	D12	D11	D10	D9	D8
0	HPF_EN_CH8	HPF_CORNER _CH8[3:0]				FILTER_TYPE_CH8[2:0]	

D7	D6	D5	D4	D3	D2	D1	D0
FILTER_TYPE _CH8[2:0]	DEC_RATE_CH8[2:0]			0	SEL_ODD_ TAP_CH8	0	USE_FILTER_ CH8

All bits default to '0' after reset.

Bit D15 **Must write '0'**

Bit D14 **HPF_EN_CH8**

This bit enables the HPF filter for channel 8.

Bits D[13:10] **HPF_CORNER _CH8[3:0]**

These bits program the HPF corner for channel 8.

Bits D[9:7] **FILTER_TYPE_CH8[2:0]**

These bits select the type of filter on channel 8.

Bits D[6:4] **DEC_RATE_CH8[2:0]**

These bits set the decimation factor for the filter on channel 8.

Bit D3 **Must write '0'**

Bit D2 **SEL_ODD_TAP_CH8**

This bit enables the odd tap filter for channel 8.

Bit D1 **Must write '0'**

Bit D0 **USE_FILTER_CH8**

This bit enables the filter for channel 8.

Table 34. Register 38h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	DATA_RATE[1:0]	

All bits default to '0' after reset.

Bits D[15:2] **Must write '0'**

Bits D[1:0] **DATA_RATE[1:0]**

Bits D1 and D0 select the output data rate depending on the type of filter.

Table 35. Register 40h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 40	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
ODD_EVEN_SEL							

All bits default to '0' after reset.

Bits D15 **Enable 40**

0 = Disable bits D[7:0] of register 40h
1 = Enable bits D[7:0] of register 40h

Bits D[14:8] **Must write '0'**

Bits D[:0] **ODD_EVEN_SEL[7:0]**

8000 = Input pins IN1, IN3, IN5, and IN7 are interleaved
80FF = Input pins IN2, IN4, IN6, and IN8 are interleaved
For more details on this bit, see the *Interleaving Mode* section.

Table 36. Register 42h

D15	D14	D13	D12	D11	D10	D9	D8
EN_PHASE_DDR	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	PHASE_DDR1	PHASE_DDR0	0	0	0	0	0

All bits default to '0' after reset.

Bit D15 **EN_PHASE_DDR**

This bit enables LCLK phase programmability.

0 = Disable bits D[6:5] of register 42h
1 = Enable bits D[6:5] of register 42h

Bits D[14:7] **Must write '0'**

Bits D[6:5] **PHASE_DDR[1:0]**

These bits control the LCLK output phase relative to data.
Refer to the *Programmable LCLK Phase* section.

Bits D[4:0] **Must write '0'**

Table 37. Register 45h

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	PAT_DESKEW_SYNC[1:0]	

All bits default to '0' after reset.

Bits D[15:2] **Must write '0'**

Bit D1 **PAT_DESKEW_SYNC1**

0 = Inactive
1 = Sync pattern mode enabled; ensure that D0 is '0'

Bit D0 **PAT_DESKEW_SYNC0**

0 = Inactive
1 = Deskew pattern mode enabled; ensure that D1 is '0'

Table 38. Register 46h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 46	0	FALL_SDR	0	EN_BIT_SER			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	EN_SDR	EN_MSB_FIRST	BTC_MODE	0	0

All bits default to '0' after reset. Note that bit D15 must be set to '1' to enable bits D[13:0].

Bit D15 **ENABLE 46**

0 = Disable bits D13, D[11:8] and D[4:2] of register 46h
1 = Enable bits D13, D[11:8] and D[4:2] of register 46h

Bit D14 **Must write '0'**

Bit D13 **FALL_SDR**

0 = The LCLK rising or falling edge comes at the edge of the data window when operating in SDR output mode
1 = The LCLK rising or falling edge comes in the middle of the data window when operating in SDR output mode

Bit D12 **Must write '0'**

Bits D[11:8] **EN_BIT_SER**

0001 = 10-bit serialization mode enabled
0010 = 12-bit serialization mode enabled
0100 = 14-bit serialization mode enabled
Do not use any other bit combinations.

Bits D[7:5] **Must write '0'**

Bit D4 **EN_SDR**

0 = DDR bit clock
1 = SDR bit clock

Bit D3 **EN_MSB_FIRST**

0 = LSB first
1 = MSB first

Bit D2 **BTC_MODE**

0 = Binary offset (ADC data output format)
1 = Twos complement (ADC data output format)

Bit D[1:0] **Must write '0'**

Programmable LVDS Mapping Mode Registers

Table 39. Register 50h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 50	0	0	0	MAP_Ch1234_to_OUT2			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	MAP_Ch1234_to_OUT1			

All bits default to '0' after reset.

Bit D15 **ENABLE 50**

0 = Disable bits D[11:8] and D[3:0] of register 50h.
1 = Enable bits D[11:8] and D[3:0] of register 50h.

Bits D[14:12], D[7:4] **Must write '0'**

Bits D[11:8] **MAP_Ch1234_to_OUT2**

These bits set the OUT2 pin pair to the channel data mapping selection.

Bits D[3:0] **MAP_Ch1234_to_OUT1**

These bits set the OUT1 pin pair to the channel data mapping selection.

Table 40. Register 51h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 51	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
MAP_Ch1234_to_OUT3				0	0	0	0

All bits default to '0' after reset.

Bit D15 **ENABLE 51**

0 = Disable bits D[7:4] of register 51h
1 = Enable bits D[7:4] of register 51h.

Bits D[14:8], D[3:0] **Must write '0'**

Bits D[7:4] **MAP_Ch1234_to_OUT3**

These bits set the OUT3 pin pair to the channel data mapping selection.

Table 41. Register 52h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 52	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	MAP_Ch1234_to_OUT4			

All bits default to '0' after reset.

Bit D15 **ENABLE 52**

0 = Disable bits D[3:0] of register 52h
1 = Enable bits D[3:0] of register 52h

Bits D[14:4] **Must write '0'**

Bits D[3:0] **MAP_Ch1234_to_OUT4**

These bits set the OUT4 pin pair to the channel data mapping selection.

Table 42. Register 53h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 53	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
MAP_Ch5678_to_OUT5				0	0	0	0

All bits default to '0' after reset.

Bit D15 **ENABLE 53**

0 = Disable bits D[7:4] of register 53h.
1 = Enable bits D[7:4] of register 53h.

Bits D[14:8], D[3:0] **Must write '0'**

Bits D[7:4] **MAP_Ch5678_to_OUT5**

These bits set the OUT5 pin pair to the channel data mapping selection.

Table 43. Register 54h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 54	0	0	0	MAP_Ch5678_to_OUT7			
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	MAP_Ch5678_to_OUT6			

All bits default to '0' after reset.

Bit D15 **ENABLE 54**

0 = Disable bits D[11:8] and D[3:0] of register 54h.
1 = Enable bits D[11:8] and D[3:0] of register 54h.

Bits D[14:12], D[7:4] **Must write '0'**

Bits D[11:8] **MAP_Ch5678_to_OUT7**

These bits set the OUT7 pin pair to the channel data mapping selection.

Bits D[3:0] **MAP_Ch5678_to_OUT6**

These bits set the OUT6 pin pair to the channel data mapping selection.

Table 44. Register 55h

D15	D14	D13	D12	D11	D10	D9	D8
ENABLE 55	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
MAP_Ch5678_to_OUT8				0	0	0	0

All bits default to '0' after reset.

Bit D15 **ENABLE 55**

0 = Disable bits D[7:4] of register 55h.
1 = Enable bits D[7:4] of register 55h.

Bits D[14:8], D[3:0] **Must write '0'**

Bits D[7:4] **MAP_Ch5678_to_OUT8**

These bits set the OUT8 pin pair to the channel data mapping selection.

Custom Coefficient Registers

Table 45. Registers 5Ah to 65h(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH1	0	0	0	COEFF*n*_SET_CH1[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH1[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 1.

Bit D15 **EN_CUSTOM_FILT_CH1**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH1[11:0]**

These bits set the custom coefficient *n* for the channel 1 digital filter.

Table 46. Registers 66h to 71h(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH2	0	0	0	COEFF*n*_SET_CH2[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH2[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 2.

Bit D15 **EN_CUSTOM_FILT_CH2**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH2[11:0]**

These bits set the custom coefficient *n* for the channel 2 digital filter.

Table 47. Registers 72h to 7Dh(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH3	0	0	0	COEFF*n*_SET_CH3[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH3[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 3.

Bit D15 **EN_CUSTOM_FILT_CH3**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH3[11:0]**

These bits set the custom coefficient *n* for the channel 3 digital filter.

Table 48. Registers 7Eh to 89h(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH4	0	0	0	COEFF*n*_SET_CH4[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH4[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 4.

Bit D15 **EN_CUSTOM_FILT_CH4**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH4[11:0]**

These bits set the custom coefficient *n* for the channel 4 digital filter.

Table 49. Registers 8Ah to 95h(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH5	0	0	0	COEFF*n*_SET_CH5[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH5[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 5.

Bit D15 **EN_CUSTOM_FILT_CH5**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH5[11:0]**

These bits set the custom coefficient *n* for the channel 5 digital filter.

Table 50. Registers 96h to A1h(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH6	0	0	0	COEFF*n*_SET_CH6[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH6[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 6.

Bit D15 **EN_CUSTOM_FILT_CH6**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH6[11:0]**

These bits set the custom coefficient *n* for the channel 6 digital filter.

Table 51. Registers A2h to ADh(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH7	0	0	0	COEFF*n*_SET_CH7[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH7[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 7.

Bit D15 **EN_CUSTOM_FILT_CH7**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH7[11:0]**

These bits set the custom coefficient *n* for the channel 7 digital filter.

Table 52. Registers AEh to B9h(1)

D15	D14	D13	D12	D11	D10	D9	D8
EN_CUSTOM_FILT_CH8	0	0	0	COEFF*n*_SET_CH8[11:0]			
D7	D6	D5	D4	D3	D2	D1	D0
COEFF*n*_SET_CH8[11:0]							

(1) n = 0 to 11.

All bits default to '0' after reset.

These registers are the custom coefficient registers for channel 8.

Bit D15 **EN_CUSTOM_FILT_CH8**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

Bits D[14:12] **Must write '0'**

Bits D[11:0] **COEFF*n*_SET_CH8[11:0]**

These bits set the custom coefficient *n* for the channel 8 digital filter.

Table 53. Register BEh

D15	D14	D13	D12	D11	D10	D9	D8
EN_LVDS_PROG	0	0	0	0	0	DELAY_DATA_R[1:0]	
D7	D6	D5	D4	D3	D2	D1	D0
DELAY_LCLK_R[2:0]			DELAY_DATA_F[1:0]		DELAY_LCLK_F[2:0]		

All bits default to '0' after reset.

Bit D15	**This bit enables LVDS edge delay programmability.**
Bits D[14:10]	**Must write '0'**
Bits D[9:8]	Refer to Table 68 for settings.
Bits D[7:5]	Refer to Table 69 for settings.
Bits D[4:3]	Refer to Table 68 for settings.
Bits D[2:0]	Refer to Table 69 for settings.

Table 54. Register F0h

D15	D14	D13	D12	D11	D10	D9	D8
EN_EXT_REF	0	0	0	0	0	0	0
D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

All bits default to '0' after reset.

The EN_HIGH_ADDRS register bit (register 01h, bit D4) must be set to '1' to allow access to this register.

Bit D15	**EN_EXT_REF** 0 = Internal reference mode (default) 1 = External reference mode enabled; apply the reference voltages on the REFT and REFB pins
Bits D[14:0]	**Must write '0'**

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5296A is a low-power, multichannel, analog-to-digital converter (ADC) that can be operated at sample rates up to 200 MSPS from a single 1.8-V supply. At the core, the device consists of eight 12-bit ADCs with sample rates up to 80 MSPS. By interleaving every pair of 12-bit ADCs, the effective sample rate can be doubled to 160 MSPS. A mode exists to operate the device as a 10-bit ADC, in which the effective sample rate can be increased to 200 MSPS with interleaving. In both the interleaving modes (12-bit and 10-bit), the device operates as a 4-channel ADC.

When interleaving is disabled, the device can also be operated as an 8-channel 10-bit ADC up to 100 MSPS for systems where the SNR of the 10-bit ADC is sufficient. To summarize, the device can be configured as:

- An 8-channel, 12-bit ADC without interleaving, with sample rates up to 80 MSPS
- An 8-channel, 10-bit ADC without interleaving, with sample rates up to 100 MSPS
- A 4-channel, 12-bit ADC with interleaving, with sample rates up to 160 MSPS
- A 4-channel, 10-bit ADC with interleaving, with sample rates up to 200 MSPS

ANALOG INPUT

The analog input consists of a switched-capacitor-based, differential sample-and-hold architecture, as shown in Figure 77. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input pin (IN_p, IN_n) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 500 MHz (measured from the input pins to the sampled voltage).

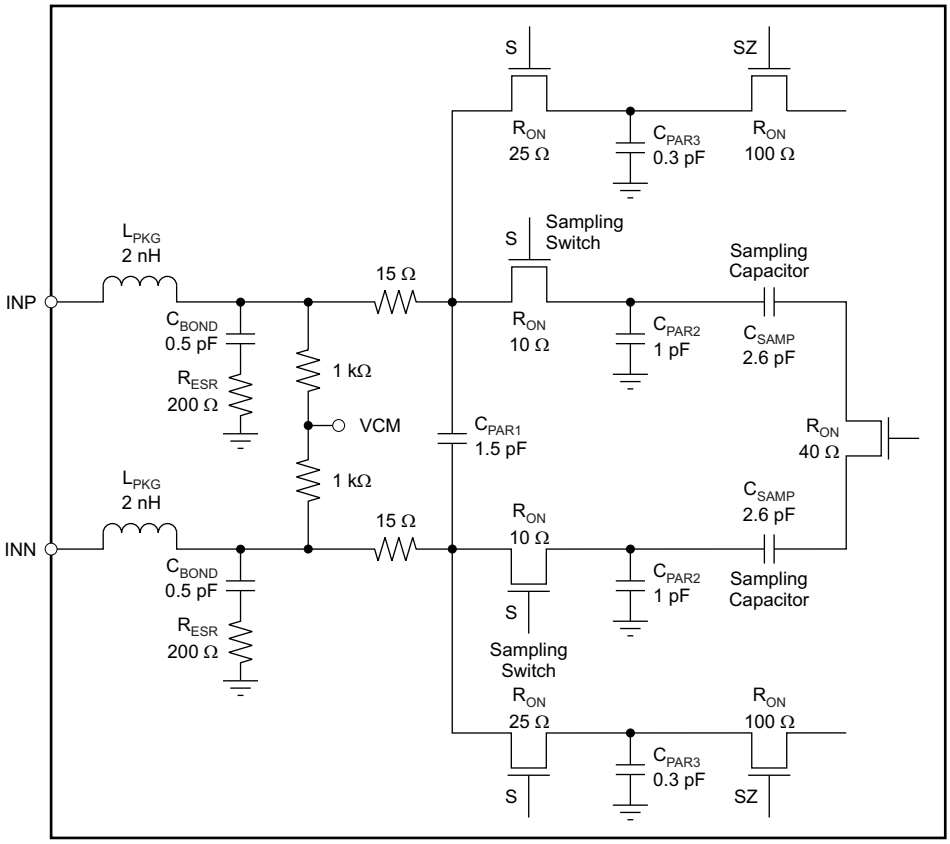


Figure 77. Analog Input Equivalent Circuit

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (10 Ω to 20 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics. The drive circuits in Figure 78 and Figure 79 show an R-C filter across the analog input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. Figure 78 is recommended for driving the analog inputs in interleaving mode and Figure 79 can be used for non-interleaving mode .

The analog input pins of the ADC have an internal 1k-Ω termination resistance connected to VCM voltage (see Figure 77) which allows external signals to be ac-coupled to the ADC input pins. During the sampling process, a common-mode current is drawn from VCM through the 1-kΩ termination. This current scales with sampling frequency (approximately 1 µA per MSPS) and results in a drop in the common-mode voltage of the input pins. The recommended range of input common-mode voltage is VCM ± 50 mV. Therefore, at higher sample rates, TI recommends connecting an external 25-Ω to 100-Ω termination resistor to VCM. Figure 80 and Figure 81 show the differential input resistance and capacitance across frequency.

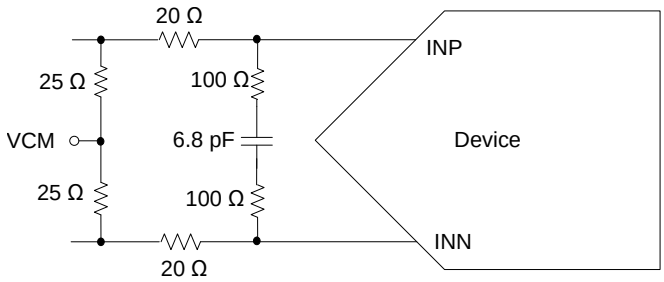


Figure 78. DC-Coupled Drive Circuit with RCR

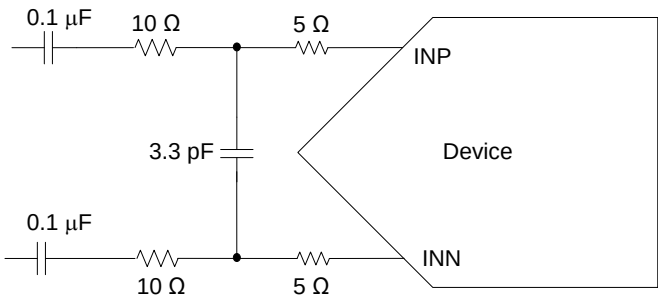


Figure 79. AC-Coupled Drive Circuit

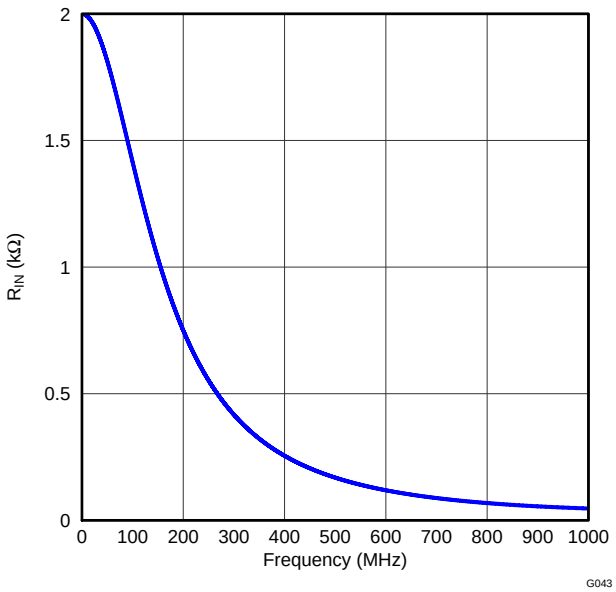


Figure 80. ADC Differential Input Resistance (R_{IN}) vs Frequency

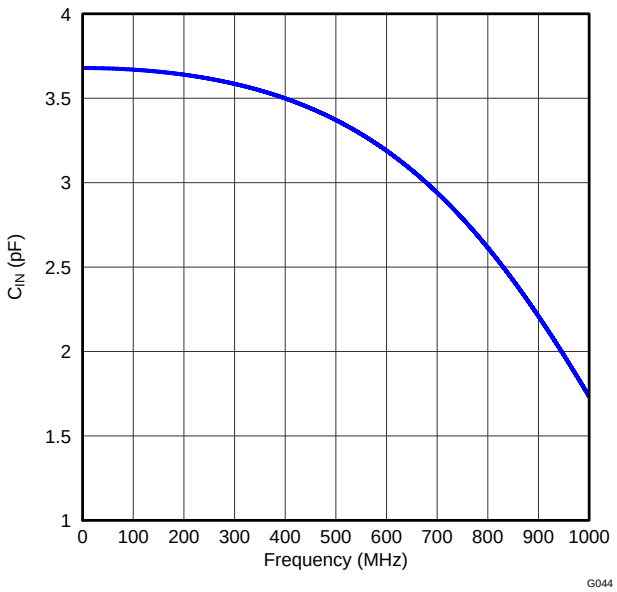


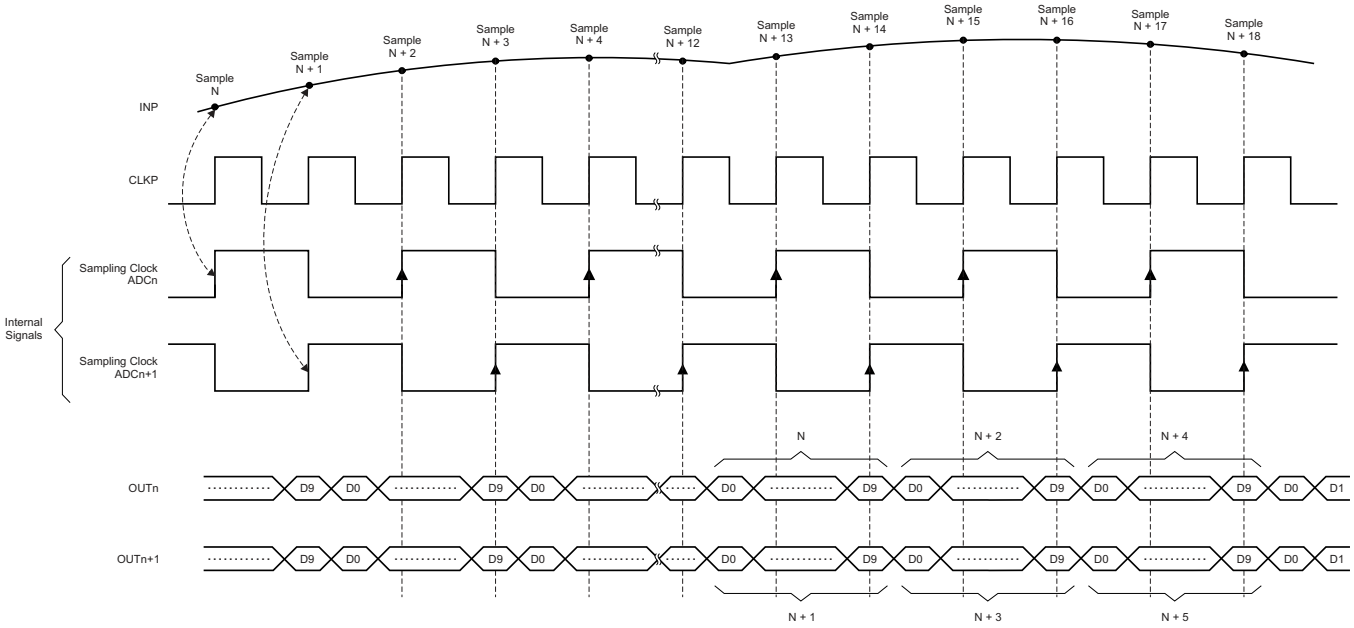
Figure 81. ADC Differential Input Capacitance (C_{IN}) vs Frequency

Large- and Small-Signal Input Bandwidth

The small-signal bandwidth of the analog input circuit is high, approximately 500 MHz. When using an amplifier to drive the ADS5296A, the total amplifier noise up to the small-signal bandwidth must be considered. The large-signal bandwidth of the device depends on the amplitude of the input signal. The ADS5296A supports a 2-V_{PP} amplitude for input signal frequencies up to 90 MHz. For higher frequencies, the amplitude of the input signal must be decreased proportionally. For example, at 180 MHz, the device supports a maximum 1-V_{PP} signal.

INTERLEAVING MODE

The interleaving mode in the device can be used to sample analog inputs at frequencies greater than 100 MSPS. A pair of ADCs are used in interleaving mode, both of which sample the same analog input signal. The sampling instants of the two ADCs are interleaved in such a way that while one ADC samples the input at every odd edge of the device input clock, the second ADC samples the input at every even edge of the input clock, as shown in Figure 82.



NOTE: n = 1, 3, 5, or 7.

Figure 82. Interleaving Mode Latency Timing Diagram

Note that in this mode, device input clock frequency is actually 2x times the sampling rate of each ADC. For example, when a 200-MHz clock input is applied, each ADC in the pair samples at 100 MHz, but the sampling instants of both ADCs are staggered (or offset) by one 200-MHz clock cycle. Each ADC converts the sampled values and outputs the data over separate LVDS pairs. The receiver used to capture the data from the device [either an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA)] must combine the data from the two LVDS pairs and reconstruct the data stream at 200 MSPS (see Figure 83). In this mode, the device operates as a 4-channel ADC because the interleaving operation requires two ADCs per channel. After applying a reset and enabling interleaving mode (EN_INTERLEAVE = 1), the four interleaved ADC channels sample the analog inputs at the odd pins (IN1, IN3, IN5, and IN7). A mode exists where the analog inputs at the even pins can be sampled by using the ODD_EVEN_SEL register bits. Instead of using the register bits, the INTERLEAVE_MUX pin can be used to select between the odd and even input pins (see Table 55).

As Figure 82 shows, in the interleaving mode, the device input clock is divided by two to generate two sampling clocks which are 180° out of phase with each other. The odd ADC (ADC1, ADC3, ADC5, ADC7) in each interleaving pair uses one sampling clock while the even ADC (ADC2, ADC4, ADC6, ADC8) in the pair uses the other sampling clock. When using multiple ADS5296A devices, ensure that the sampling clock for the odd (and even) ADCs in every chip are synchronized. This can be achieved by using the SYNC input signal; see the *Synchronization Using the SYNC Pin* section for a description of the SYNC functionality.

Table 55. Interleaving Mode

MODE	PIN(1)	REGISTER BITS		
	INTERLEAVE_MUX	EN_INTERLEAVE	EN_MUX_REG	ODD_EVEN_SEL
No interleaving • 8-channel ADC mode • IN1 ↔ OUT1, IN2 ↔ OUT2	Don't care	0	0	8000h
• IN3 ↔ OUT3, IN4 ↔ OUT4 • IN5 ↔ OUT5, IN6 ↔ OUT6 • IN7 ↔ OUT7, IN8 ↔ OUT8	Low	0	1	Don't care
No interleaving • 8-channel ADC mode • IN1 ↔ OUT2, IN2 ↔ OUT1	Don't care	0	0	80FFh
• IN3 ↔ OUT4, IN4 ↔ OUT3 • IN5 ↔ OUT6, IN6 ↔ OUT5 • IN7 ↔ OUT8, IN8 ↔ OUT7	High	0	1	Don't care
Interleaving enabled • 4-channel ADC mode • IN1 ↔ OUT1, OUT2	Don't care	1	0	8000h
• IN3 ↔ OUT3, OUT4 • IN5 ↔ OUT5, OUT6 • IN7 ↔ OUT7, OUT8	Low	1	1	Don't care
Interleaving enabled • 4-channel ADC mode • IN2 ↔ OUT1, OUT2	Don't care	1	0	80FFh
• IN4 ↔ OUT3, OUT4 • IN6 ↔ OUT5, OUT6 • IN8 ↔ OUT7, OUT8	High	1	1	Don't care

(1) INTERLEAVE_MUX has an internal pull-up resistor to supply.

The block diagrams for interleaving even input pins and interleaving odd input pins are shown in Figure 83 and Figure 84.

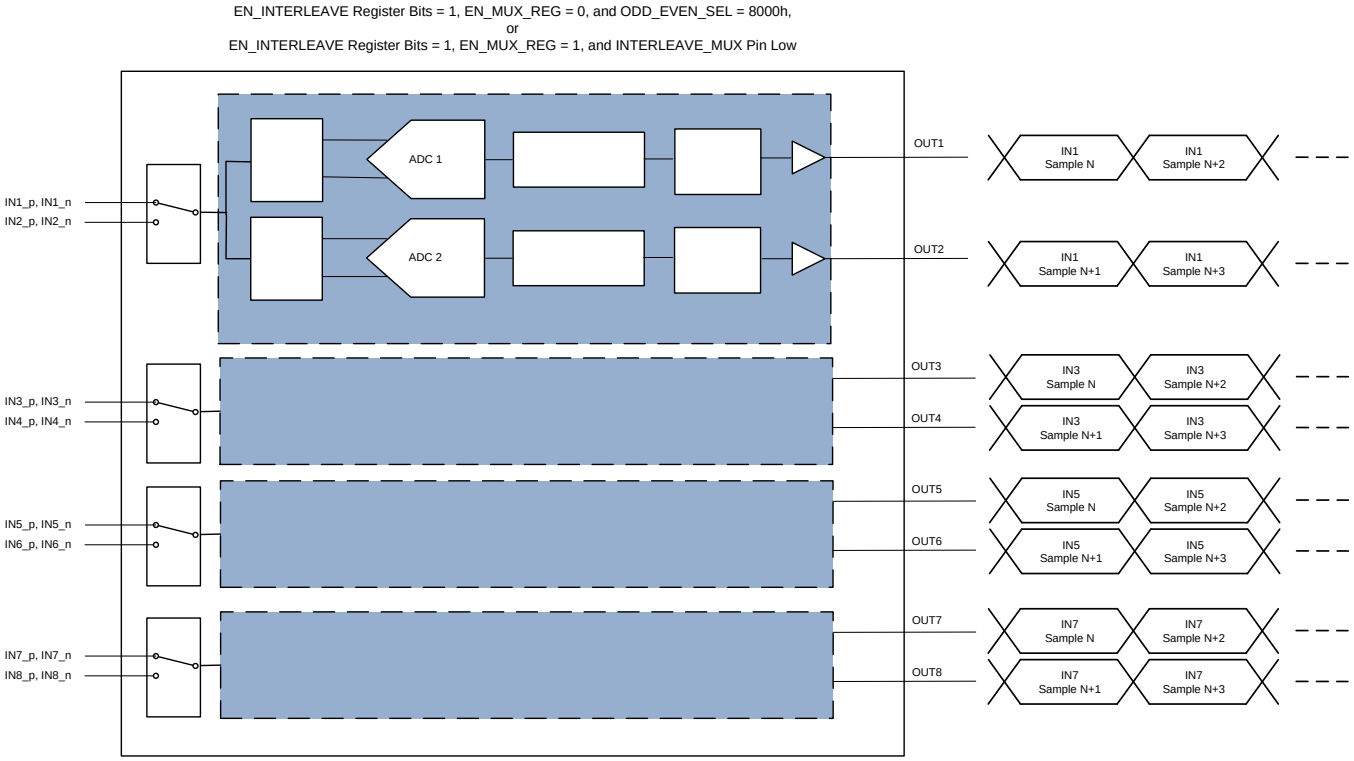


Figure 83. Odd Input Pins, Interleaved

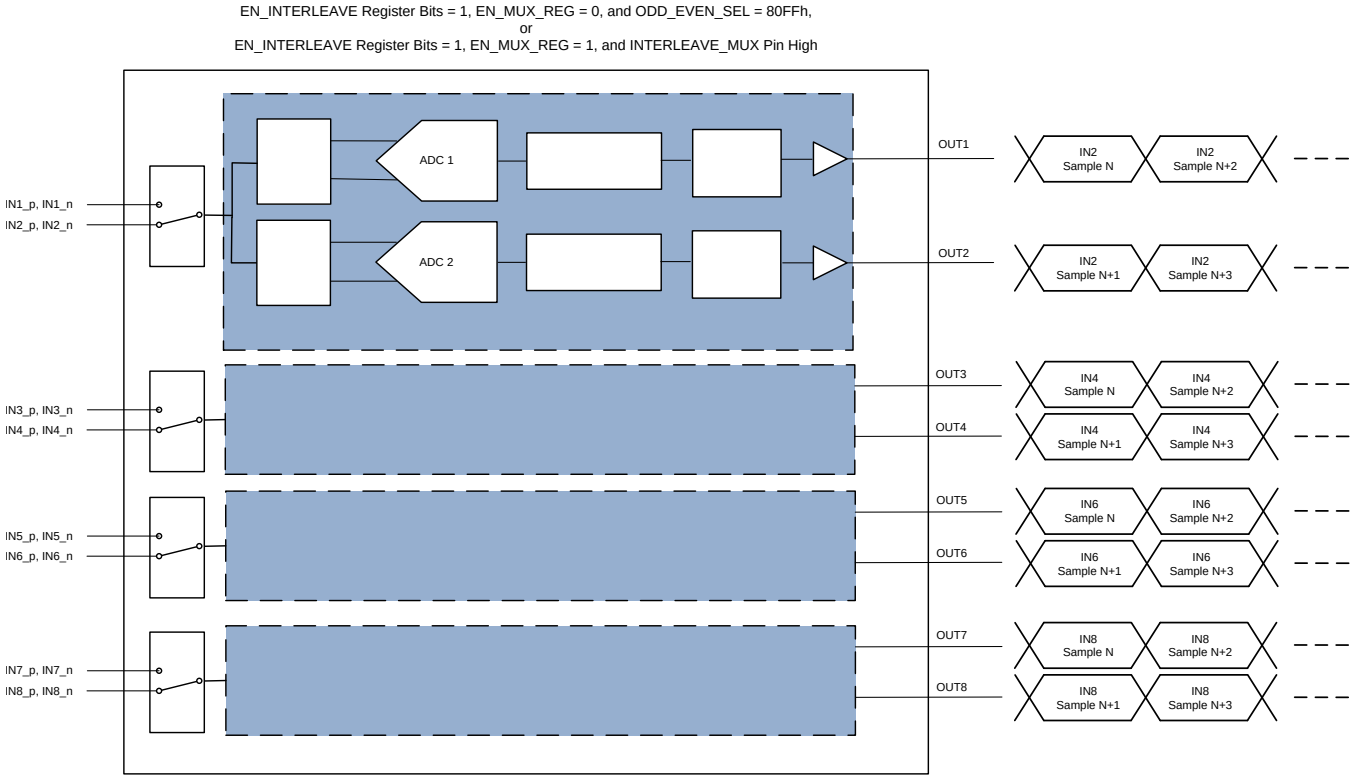


Figure 84. Even Input Pins, Interleaved

CLOCK INPUT

The device can operate with both single-ended (CMOS) and differential input clocks (such as sine wave, LVPECL, and LVDS). Operating with a low-jitter differential clock is recommended for good SNR performance, especially at input frequencies greater than 30 MHz. In differential mode, the clock inputs are internally biased to a 0.95-V common-mode voltage. While driving with an external LVPECL or LVDS driver, TI recommends ac-coupling the clock signals so that the clock pins are correctly biased to the common-mode voltage (0.95 V). To operate using a single-ended clock, connect a CMOS clock source to CLKP and tie CLKN to GND. The device automatically detects the presence of a single-ended clock without requiring any configuration and disables internal biasing. Typical clock termination schemes are shown in Figure 85, Figure 86, Figure 87, and Figure 88. Figure 89 and Figure 90 show the equivalent circuit of the clock pins in both single-ended and differential modes.

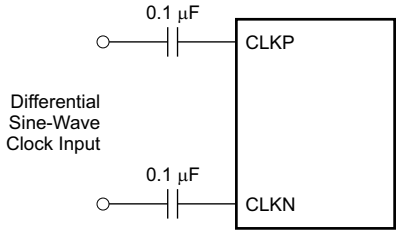


Figure 85. Differential Sine-Wave Clock Driving Circuit

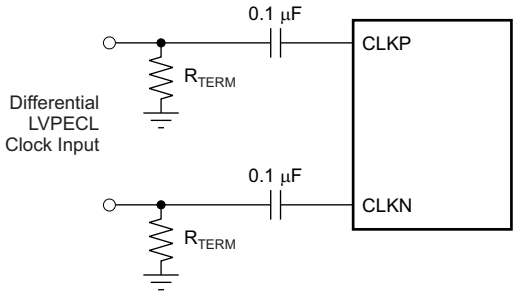


Figure 86. Differential LVPECL Clock Driving Circuit

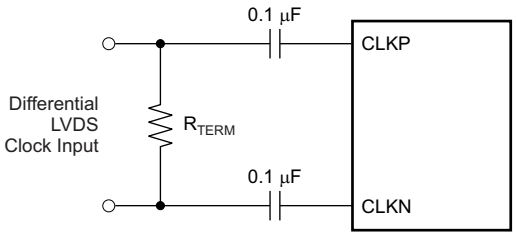


Figure 87. Differential LVDS Clock Driving Circuit

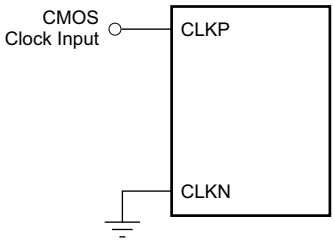


Figure 88. Single-Ended Clock Driving Circuit

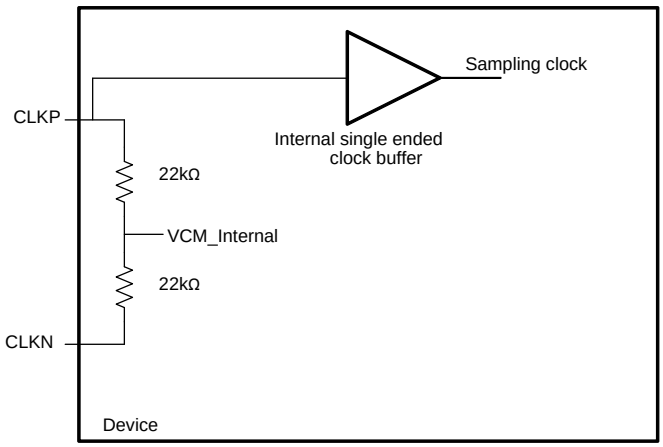


Figure 89. Input Clock Equivalent Circuit: Single-Ended Mode

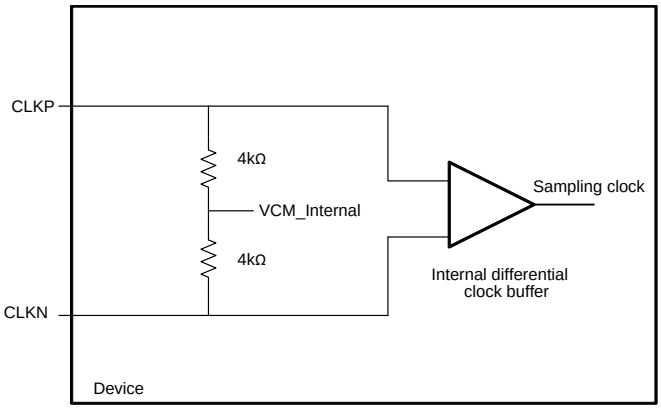


Figure 90. Input Clock Equivalent Circuit: Differential Mode

EXTERNAL REFERENCE MODE OF OPERATION

For normal operation, the device requires two reference voltages (REFT and REFB) that are generated internally by default, as shown in Figure 91. The value of the reference voltage determines the actual ADC full-scale input voltage, as shown in Equation 1:

$$\text{Full-Scale Input Voltage} = 2 \times (V_{REFT} - V_{REFB}) \quad (1)$$

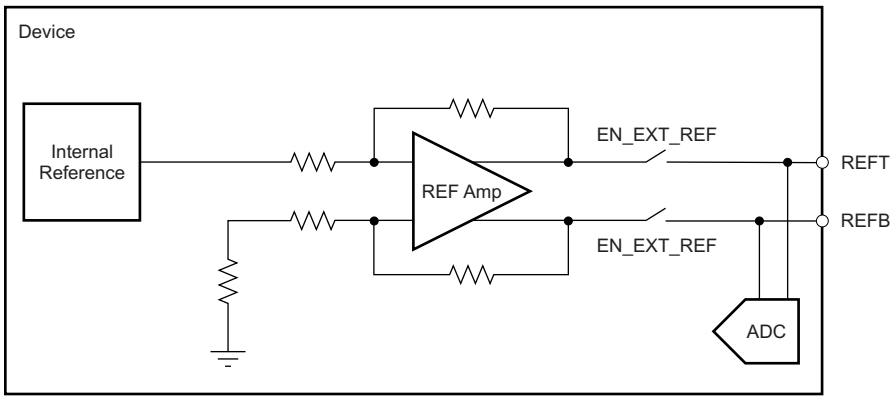


Figure 91. Reference Equivalent Circuit

Any error in the reference results in a deviation of the full-scale input range from its ideal value of 2.0 V_{PP}, as shown in Equation 2:

$$\text{Error in Full-Scale Voltage} = 2x\ [\text{Error in } (V_{REFT} - V_{REFB})] \quad (2)$$

The reference inaccuracy results in a gain error, which is defined as Equation 3:

$$\text{Gain Error (\%)} = \text{Error in Full-Scale Voltage} \times \frac{100}{\text{Ideal Full-Scale Voltage}}$$

$$= 2x\ [\text{Error in } (V_{REFT} - V_{REFB})] \times \frac{100}{2.0} \quad (3)$$

To minimize gain error, the internal reference voltages are trimmed to an accuracy of ±1.5%. To obtain even lower gain error, the device supports an external reference mode of operation. In this mode, the internal reference amplifiers are powered down and an external amplifier must force the reference voltages on the REFT and REFB pins. For example, this mode can be used to ensure that multiple ADS5296A devices in the system have nearly the same full-scale voltage.

To enable external reference mode, set the register bits as shown in Table 56. These settings power-down the internal reference amplifier and the two reference voltages can be forced directly on the REFT and REFB pins as V_{REFT} = 1.45 V and V_{REFB} = 0.45 V, respectively.

Table 56. External Reference Function

FUNCTION	EN_HIGH_ADDRS	EN_EXT_REF
External reference using the REFT, REFB pins	1	1

Because the internal reference amplifiers are powered down, the accuracy of the full-scale voltage is determined by the accuracy of ($V_{REFT} - V_{REFB}$), where V_{REFT} is the voltage forced on REFT and V_{REFB} is the voltage forced on REFB. Note that although the nominal value of ($V_{REFT} - V_{REFB}$) = 1.0 V, ensure that Equation 4 is met:

$$[(V_{REFT} + V_{REFB}) / 2 = 0.950\ V \pm 50\ mV] \quad (4)$$

Figure 92 shows an example of driving the reference pins. The 1-µF bypass capacitor helps provide the switching current drawn by the REFT and REFB pins. The external amplifier must provide an average current of 5 mA or less at the maximum sample rate. Performance in the external reference mode depends on sampling speed. At low sampling speeds (for instance, 20 MSPS), performance is the same as that of an internal reference. At higher speeds, performance degrades because of the effect of parasitic bond-wire inductance of the REF pins. Figure 93 highlights the difference in SNR between the external and internal reference modes.

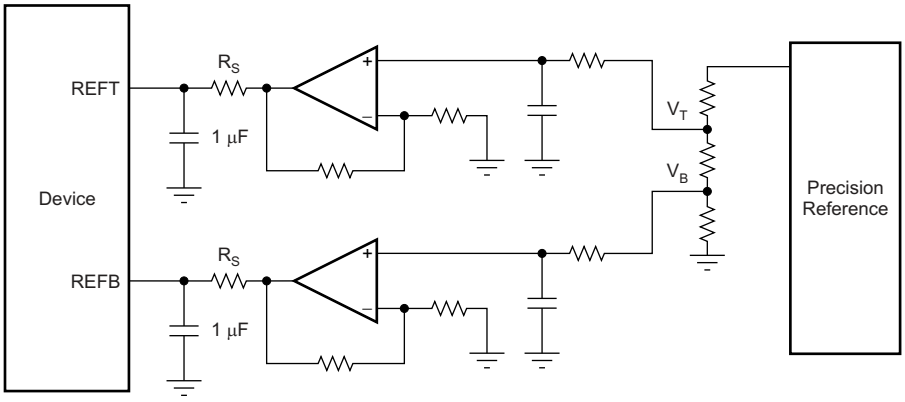


Figure 92. Driving Reference Inputs in External Reference Mode

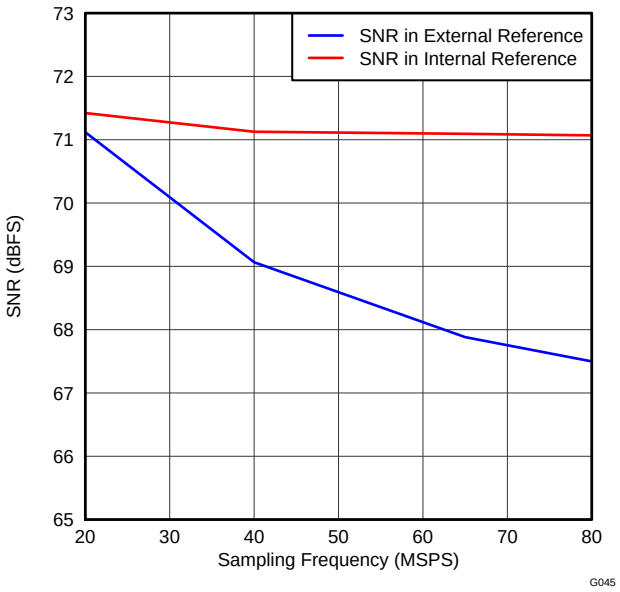


Figure 93. SNR in Internal and External Reference Mode

LOW-FREQUENCY NOISE SUPPRESSION

The low-frequency noise suppression (LFNS) mode is particularly useful in applications where good noise performance is desired in the low-frequency band of dc to 1 MHz. By setting this mode, the low-frequency noise spectrum band around dc is shifted to a similar band around f_S / 2 (or the Nyquist frequency). As a result, the noise spectrum from dc to approximately 1 MHz improves significantly, as shown in Figure 94, Figure 95, and Figure 96.

This function can be selectively enabled in each channel using the LFNS_CH register bits. Figure 94, Figure 95, and Figure 96 show the effect of this mode on the spectrum.

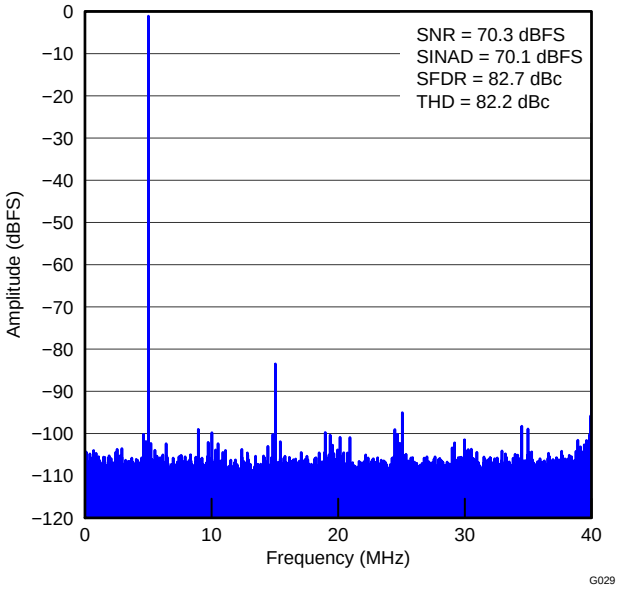


Figure 94. Full-Band FFT, 5-MHz Input (80-MHz FS with LFNS Enabled)

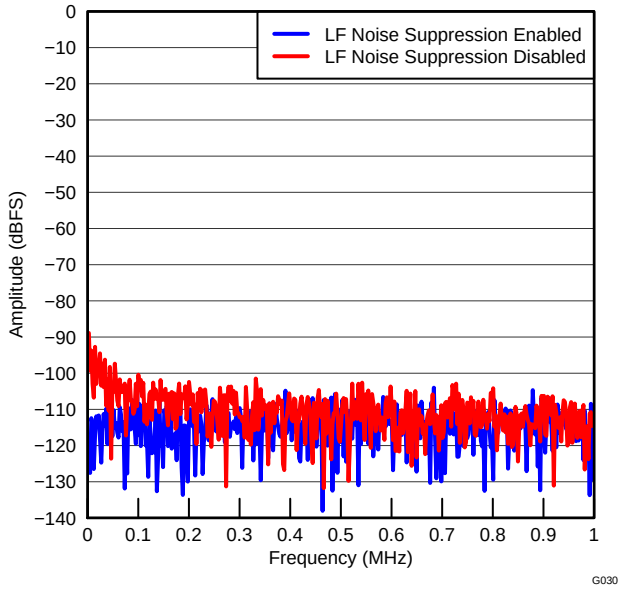


Figure 95. 0-MHz to 1-MHz FFT, 5-MHz Input (80-MHz FS with LFNS Enabled)

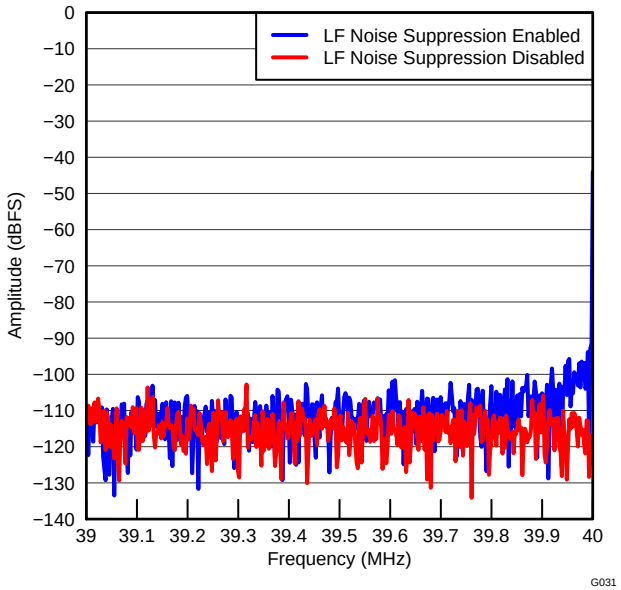


Figure 96. 39-MHz to 40-MHz FFT, 5-MHz Input (80-MHz FS with LFNS Enabled)

DIGITAL PROCESSING BLOCKS

The device integrates a set of commonly-used digital functions that can be used to ease system design. These functions are shown in Figure 97 and are described in the following sections.

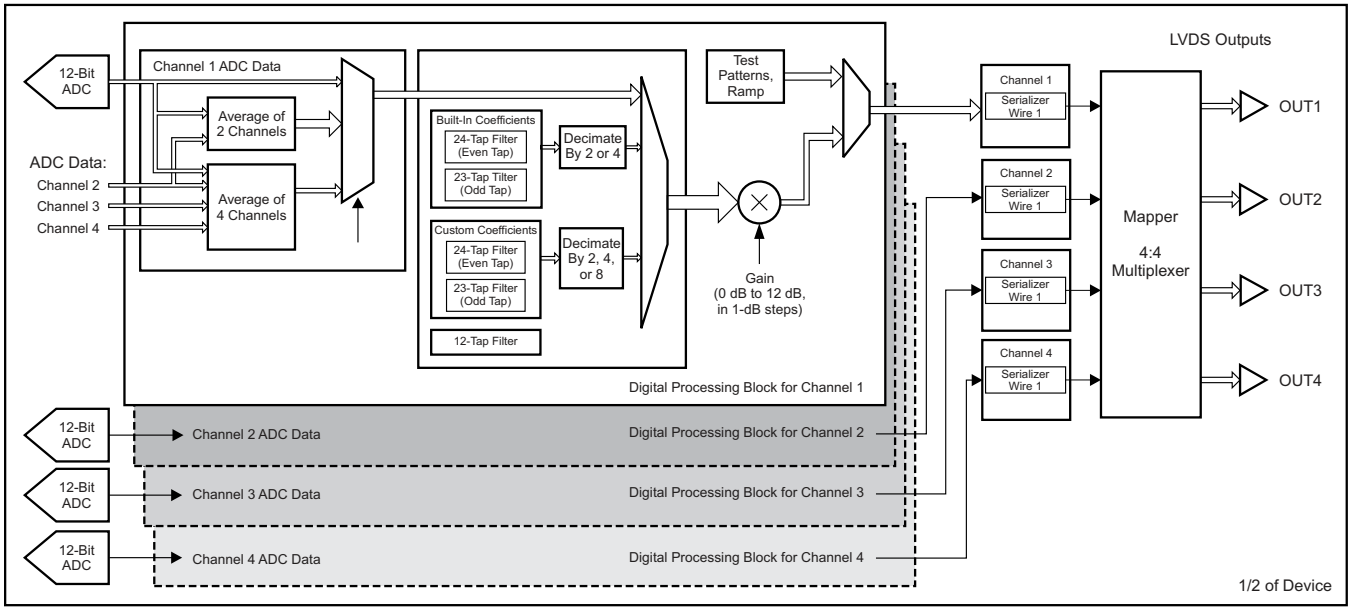


Figure 97. Digital Processing Block Diagram

Digital Gain

The device includes programmable digital gain settings from 0 dB to 12 dB, in 1-dB steps. The benefit of digital gain is obtaining improved SFDR performance. However, SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades by approximately 1 dB. Therefore, gain can be used to trade-off between SFDR and SNR.

For each gain setting, the supported analog input full-scale range scales proportionally, as shown in Table 57. After reset, the device comes up in 0-dB gain mode. To use other gain settings, program the GAIN_CHn[3:0] register bits.

Table 57. Analog Full-Scale Range Across Gains

GAIN_CHn[3:0]	DIGITAL GAIN (dB)	ANALOG FULL-SCALE INPUT (V_{PP})
0000	0	2
0001	1	1.78
0010	2	1.59
0011	3	1.42
0100	4	1.26
0101	5	1.12
0110	6	1
0111	7	0.89
1000	8	0.8
1001	9	0.71
1010	10	0.63
1011	11	0.56
1100	12	0.5
Other combinations	Do not use	—

Digital Filter

The digital processing block includes the option to filter and decimate the ADC data outputs digitally. Various filters and decimation rates are supported: decimation rates of 2, 4, and 8, and low-pass, high-pass, and band-pass filters are available.

The filters are internally implemented as 24-tap symmetric finite impulse response (FIR) filters (even-tap) using the predefined coefficients of Equation 5:

y(n) =

$$\left[\frac{1}{2^{11}}\right] \times [h0.x(n) + h1.x(n-1) + h2.x(n-2) + ... + h11.x(n-11) + h12.x(n-12) + ... + h1.x\ (n-22) + h0.x(n-23)] \quad (5)$$

Alternatively, some filters can be configured as 23-tap symmetric FIR filters (odd-tap), as described in Equation 6:

y(n) =

$$\left[\frac{1}{2^{11}}\right] \times [h0.x(n) + h1.x(n-1) + h2.x(n-2) + ... + h10.x(n-10) + h11.x(n-11) + h10.x(n-12) + ... + h1.x\ (n-21) + h0.x(n-22)] \quad (6)$$

In Equation 5 and Equation 6, h0 through h11 are 12-bit, signed, twos complement representations of the coefficients (–2048 to +2047). x(n) is the filter input data sequence and y(n) is the filter output sequence.

Details of the registers used for configuring the digital filters are described in the digital filter registers (registers 29h, 2Eh, 2Fh, 30h, 31h, and 38h) and Table 58. Table 58 gives a summary of the register bits to be used for each filter type.

Table 58. Digital Filters

DECIMATION	TYPE OF FILTER	DATA_ RATE	DEC_RATE _CHn(1)	FILTER_ TYPE_CHn	ODD_ TAP_CH*n*	USE_ FILTER_ CH*n*	EN_ CUSTOM_ FILT_CH*n*	EN_DIG_ FILTER
Decimate-by-2	Built-in, low-pass, odd-tap filter (pass band = 0 to f_S / 4)	01	000	000	1	1	0	1
	Built-in, high-pass, odd-tap filter (pass band = 0 to f_S / 4)	01	000	001	1	1	0	1
Decimate-by-4	Built-in, low-pass, even-tap filter (pass band = 0 to f_S / 8)	10	001	010	0	1	0	1
	Built-in, first band-pass, even-tap filter (pass band = f_S / 8 to f_S / 4)	10	001	011	0	1	0	1
	Built-in, second band-pass, even-tap filter (pass band = f_S / 4 to 3 f_S / 8)	10	001	100	0	1	0	1
	Built-in, high-pass, odd-tap filter (pass band = 3 f_S / 8 to f_S / 2)	10	001	101	1	1	0	1
Decimate-by-2	Custom filter (user-programmable coefficients)	01	000	000	0 or 1	1	1	1
Decimate-by-4	Custom filter (user-programmable coefficients)	10	001	000	0 or 1	1	1	1
Decimate-by-8	Custom filter (user-programmable coefficients)	11	100	000	0 or 1	1	1	1
12-tap filter, no decimation	Custom filter (user-programmable coefficients)	00	011	000	0	1	1	1

(1) The DEC_RATE_CH*n* value must be the same for all channels.

Predefined Coefficients

The built-in filter types (low pass, high pass, and band pass) use predefined coefficients. The frequency response of the built-in filters is shown in Figure 98 and Figure 99.

The predefined coefficients for the decimate-by-2 and decimate-by-4 filters are listed in Table 59 and Table 60, respectively.

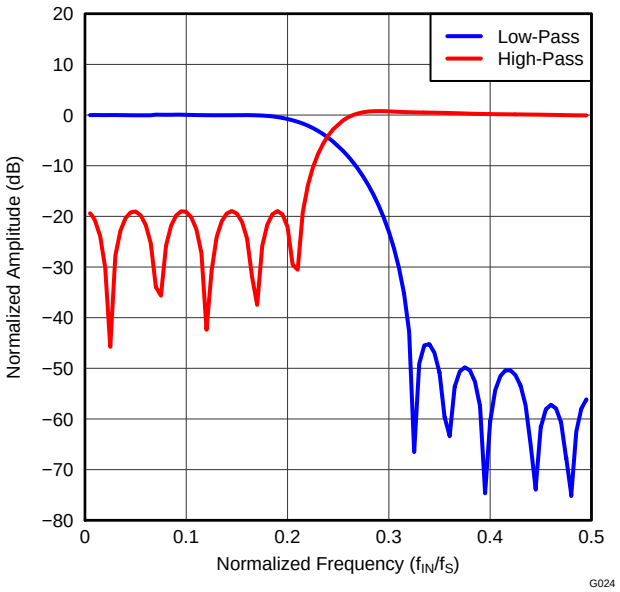


Figure 98. Filter Response (Decimate-by-2)

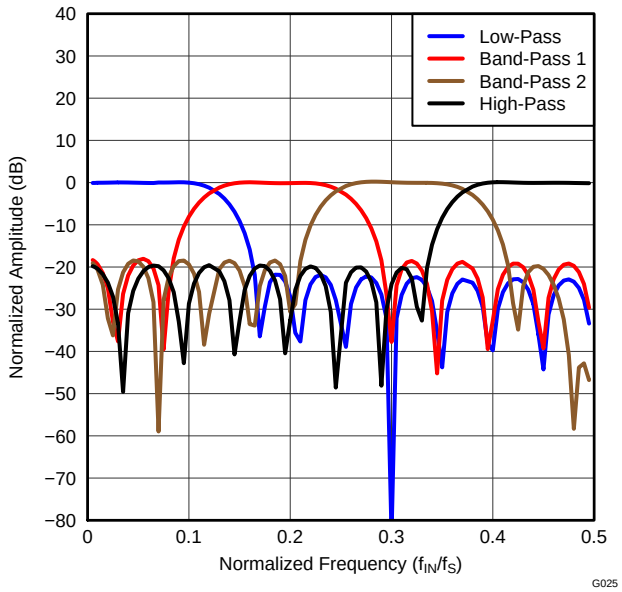


Figure 99. Filter Response (Decimate-by-4)

Table 59. Predefined Coefficients for Decimate-by-2 Filters

COEFFICIENTS	DECIMATE-BY-2 FILTERS	
	LOW-PASS	HIGH-PASS
h0	3	–22
h1	0	–65
h2	5	–52
h3	1	30
h4	–27	66
h5	–2	–35
h6	73	–107
h7	3	38
h8	–178	202
h9	–4	–41
h10	636	–644
h11	1024	1061

Table 60. Predefined Coefficients for Decimate-by-4 Filters

COEFFICIENTS	DECIMATE-BY-4 FILTERS			
	LOW-PASS	1st BAND-PASS	2nd BAND-PASS	HIGH-PASS
h0	–17	–7	–34	40
h1	–50	19	–34	–15
h2	71	–47	–101	–95
h3	46	127	43	22
h4	24	73	58	–8
h5	–42	0	–28	–81
h6	–100	86	–5	106
h7	–97	117	–179	–62
h8	8	–190	294	–97
h9	202	–464	86	310
h10	414	–113	–563	–501
h11	554	526	352	575

Custom Filter Coefficients

In addition to the built-in filters described in the *Predefined Coefficients* section, customers also have the option of using their own custom, 12-bit, signed coefficients. Because of the symmetric FIR implementation of the filters, only 12 coefficients can be specified with the configurations in Equation 5 or Equation 6. These coefficients (h0 to h11) must be configured in the custom coefficient registers, as shown in Equation 7:

$$\text{Register Content} = \text{12-Bit Signed Representation of (Real Coefficient Value} \times 2^{11}) \quad (7)$$

The 12 custom coefficients must be loaded into 12 separate registers for each channel (refer to the custom coefficient registers, 5Ah to B9h). The MSB bit of each coefficient register determines whether built-in filters or custom filters are used. If the EN_CUSTOM_FILT MSB bit is reset to '0', then built-in filter coefficients are used. Otherwise, custom coefficients are used.

Custom Filter without Decimation

Another mode is available that enables the use of the digital filter without decimation. In this mode, the filter behaves similar to a 12-tap symmetric FIR filter, as shown in Equation 8:

$$y(n) = \left[\frac{1}{2^{11}}\right] \times [h6.x(n) + h7.x(n-1) + h8.x(n-2) + h9.x(n-3) + h10.x(n-4) + h11.x(n-5) + h11.x(n-6) + h10.x(n-7) + h9.x(n-8) + h8.x(n-9) + h7.x(n-10) + h6.x\,(n-11)] \quad (8)$$

In Equation 8, h6 through h11 are 12-bit, signed, twos complement representations of the coefficients (–2048 to +2047). x(n) is the filter input data sequence and y(n) is the filter output sequence.

In this mode, because the filter is implemented as a 12-tap symmetric FIR, only six custom coefficients must be specified and loaded in registers h6 to h11 (refer to the custom coefficient registers, 5Ah to B9h). To enable this mode, use the register setting specified in bit 15 of registers AEh to B9h.

Digital High-Pass Filter

In addition to the 12 tap filters described previously, the digital processing block also includes a separate high-pass filter for each channel. The high-pass corner frequency can be programmed using bits D[14:10] in register 2Eh.

Digital Averaging

The device includes an averaging function where the ADC digital data from two (or four) channels can be averaged. The averaged data are output on specific LVDS channels. Table 61 shows the combinations of the input channels that can be averaged and the LVDS channels on which the averaged data are available.

Table 61. Using Channel Averaging

AVERAGED CHANNELS	OUTPUT WHERE AVERAGED DATA ARE AVAILABLE AT	REGISTER SETTINGS
1, 2	OUT1	Set AVG_OUT1 = 10 and EN_CHANNEL_AVG = 1
1, 2	OUT3	Set AVG_OUT3 = 11 and EN_CHANNEL_AVG = 1
3, 4	OUT4	Set AVG_OUT4 = 10 and EN_CHANNEL_AVG = 1
3, 4	OUT2	Set AVG_OUT2 = 11 and EN_CHANNEL_AVG = 1
1, 2, 3, 4	OUT1	Set AVG_OUT1 = 11 and EN_CHANNEL_AVG = 1
1, 2, 3, 4	OUT4	Set AVG_OUT4 = 11 and EN_CHANNEL_AVG = 1
5, 6	OUT5	Set AVG_OUT5 = 10 and EN_CHANNEL_AVG = 1
5, 6	OUT7	Set AVG_OUT7 = 11 and EN_CHANNEL_AVG = 1
7, 8	OUT8	Set AVG_OUT8 = 10 and EN_CHANNEL_AVG = 1
7, 8	OUT6	Set AVG_OUT6 = 11 and EN_CHANNEL_AVG = 1
5, 6, 7, 8	OUT5	Set AVG_OUT5 = 11 and EN_CHANNEL_AVG = 1
5, 6, 7, 8	OUT8	Set AVG_OUT8 = 11 and EN_CHANNEL_AVG = 1

Performance with Digital Processing Blocks

In applications where higher SNR performance is desired, digital processing blocks (such as averaging and decimation filters) can be used advantageously to achieve higher performance. Table 62 shows the improvement in SNR that can be achieved compared to the default value, using these modes.

Table 62. SNR Improvement Using Digital Processing

MODE	TYPICAL SNR (dB)(1)	TYPICAL IMPROVEMENT IN SNR (dB)
Default	70.4	NA
With decimate-by-2 filter enabled	75.4	5
With decimate-by-4 filter enabled	76.7	6.3
With two channels averaged	75	4.6
With four channels averaged	75.8	5.4

(1) In all modes (except default), 14x serialization is used to capture data.

PROGRAMMABLE MAPPING BETWEEN INPUT CHANNELS AND OUTPUT PINS

The device has eight pairs of LVDS channel outputs. The mapping of ADC channels to LVDS output channels is programmable to allow for flexibility in board layout. Control register mapping is shown in Table 63. The eight LVDS channel outputs are split into two groups of four LVDS pairs. Within each group, four ADC input channels can be multiplexed to the four LVDS pairs.

Table 63. Mapping Control Registers

ADDRESS (Hex)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
50	1												X	X	X	X	MAP_Ch1234_to_OUT1
	1				X	X	X	X									MAP_Ch1234_to_OUT2
51	1								X	X	X	X					MAP_Ch1234_to_OUT3
52	1												X	X	X	X	MAP_Ch1234_to_OUT4
53	1								X	X	X	X					MAP_Ch5678_to_OUT5
54	1												X	X	X	X	MAP_Ch5678_to_OUT6
	1				X	X	X	X									MAP_Ch5678_to_OUT7
55	1								X	X	X	X					MAP_Ch5678_to_OUT8

Input channels 1 to 4 can be mapped to any LVDS output (OUT1 to OUT4) using the MAP_CH1234_TO_OUTn bits, as shown in Table 64.

Table 64. Mapping Analog Inputs IN1-IN4 to LVDS Outputs OUT1-4

MAP_CH1234_TO_OUTN[3:0](1)	MAPPING
0000	ADC input channel IN1 to OUT*n*
0010	ADC input channel IN2 to OUT*n*
0100	ADC input channel IN3 to OUT*n*
0110	ADC input channel IN4 to OUT*n*
1xxx	LVDS output buffer OUT*n* powered down

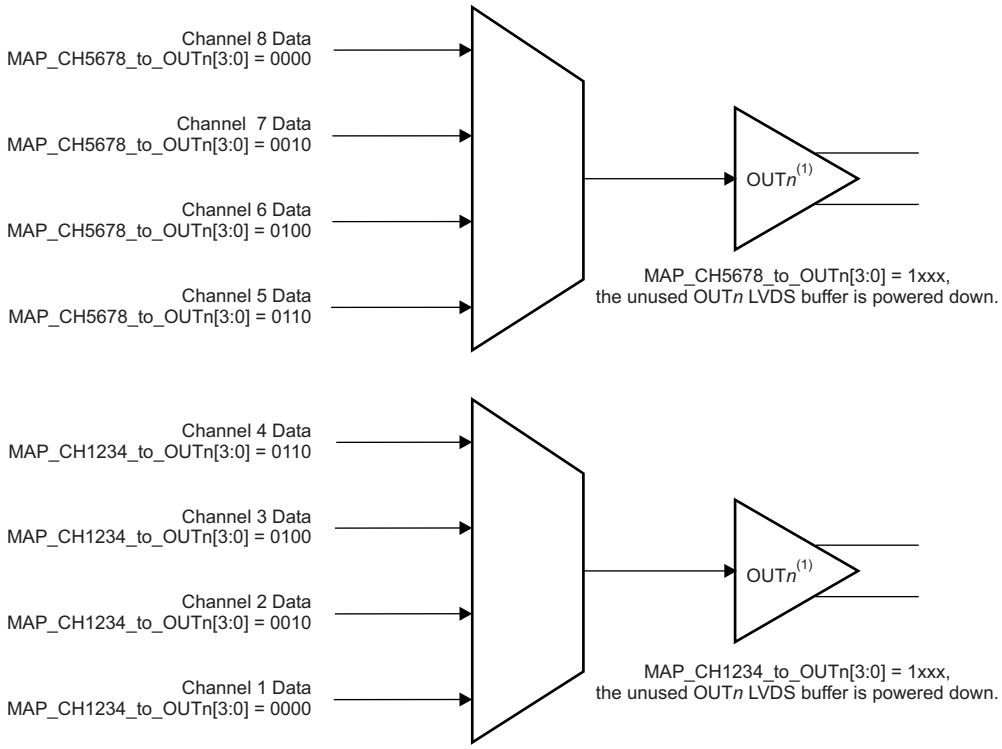
(1) n = 1, 2, 3, or 4.

Similarly, input channels 5 to 8 can be mapped to any LVDS output (OUT5 to OUT8) using the MAP_CH5678_TO_OUTn bits, as shown in Table 65. Both multiplexing options are controlled by registers 50h to 55h. The channel mapping block diagram is illustrated in Figure 100.

Table 65. Mapping analog inputs IN8-IN8 to LVDS outputs OUT5-8

MAP_CH5678_TO_OUTN[3:0](1)	MAPPING
0000	ADC input channel IN8 to OUT*n*
0010	ADC input channel IN7 to OUT*n*
0100	ADC input channel IN6 to OUT*n*
0110	ADC input channel IN5 to OUT*n*
1xxx	LVDS output buffer OUT*n* powered down

(1) n = 5, 6, 7, or 8.



(1) For channels 1 to 4, n = 1, 2, 3, 4. For channels 5 to 8, n = 5, 6, 7, 8.

Figure 100. Channel Mapping

The default mapping is shown in Table 66.

Table 66. Default Mapping After Reset

ANALOG INPUT CHANNEL	LVDS OUTPUT
Channel IN1	OUT1
Channel IN2	OUT2
Channel IN3	OUT3
Channel IN4	OUT4
Channel IN5	OUT5
Channel IN6	OUT6
Channel IN7	OUT7
Channel IN8	OUT8

SYNCHRONIZATION USING THE SYNC PIN

The SYNC pin can be used to synchronize:

- The data output across channels within the same device or
- The data from channels across multiple devices when decimation filters are used
- The odd and even ADC sampling instants across multiple devices in interleaving mode

When decimation filters are used (if the decimate-by-2 filter is enabled, for example), then effectively the device outputs one digital code for every two analog input samples. If the SYNC pulse is not used, then the filters are not synchronized (even within a device). When the filters are not synchronized, one channel may be transmitting codes corresponding to input samples N, N+1, and so on, while another channel may be transmitting codes corresponding to N+1, N+2, and so on.

To achieve synchronization across multiple devices, the SYNC pulse must arrive at all ADS5296A devices at the same time (as shown in Figure 101). The ADS5296A generates an internal synchronization signal that resets the internal clock dividers used by the decimation filter and in the interleaving mode. Using the SYNC signal in this manner ensures that all channels output digital codes corresponding to the same set of input samples.

Synchronizing the filters using the SYNC pin is enabled by default. No register bits are required to be written. The TP_HARD_SYNC register bit must be reset to '0' for this mode to function properly. As shown in Figure 101, the SYNC rising edge can be positioned anywhere within the window. SYNC width must be at least one clock cycle.

In addition, SYNC can also be used to synchronize the RAMP test patterns across channels. In order to synchronize the test patterns, TP_HARD_SYNC must be set to '1'. Setting TP_HARD_SYNC to '1' actually disables the sync of the filters.

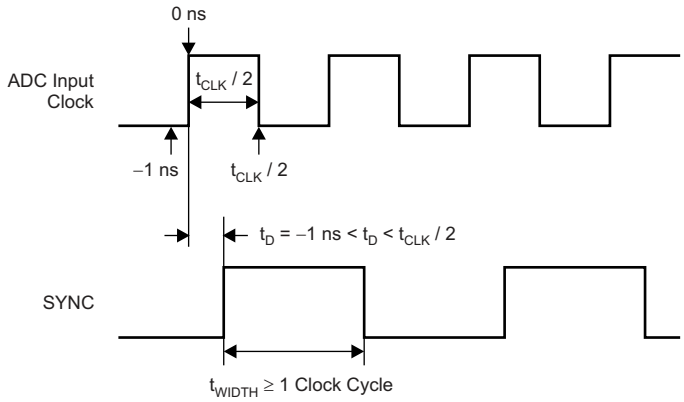


Figure 101. SYNC Timing Diagram

Synchronizing ADC Sampling Instants (Non-Interleaving mode)

Note that in the non-interleaved mode, the SYNC cannot be used to synchronize the ADC sampling instants across devices. All channels within a single device sample the analog inputs simultaneously. To ensure that channels across two devices sample the analog inputs simultaneously, the input clock must be routed to both devices with an identical length. This layout ensures that the input clocks arrive at both devices at the same time.

DIGITAL OUTPUT INTERFACE

SERIAL LVDS INTERFACE

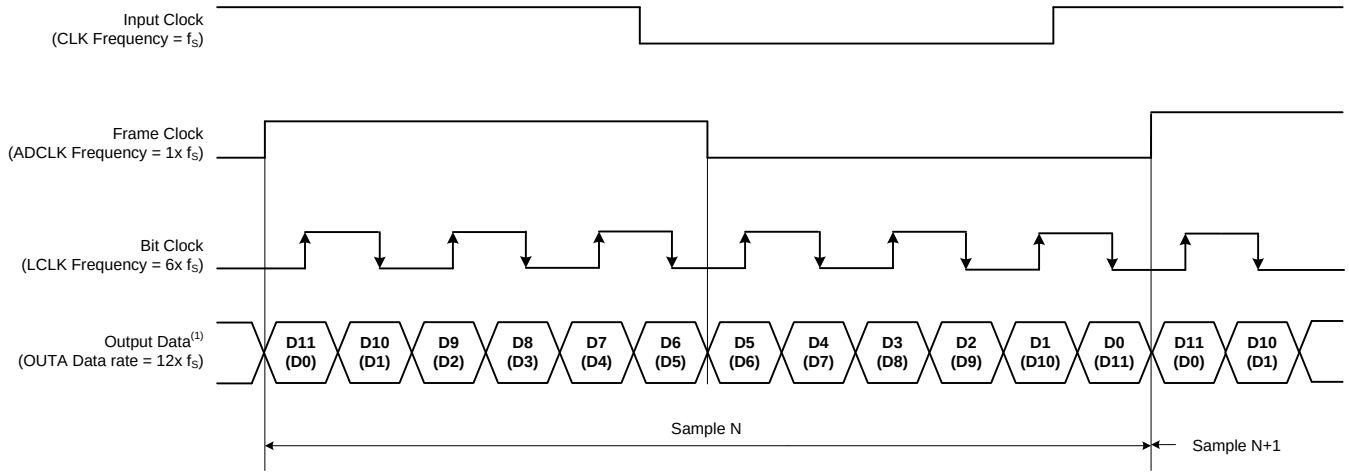
The ADS5296A offers several flexible output options, making the device easy to interface to an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA). Each option can be easily programmed using the serial interface. A summary of all available options is listed in Table 67 along with the default values after power-up and reset. Following Table 67, each option is described in detail.

Table 67. Summary of Output Interface Options

FEATURE	OPTIONS	DEFAULT AFTER POWER-UP AND RESET	BRIEF DESCRIPTION
Serialization factor	12x	12x	
	10x	12x	
	14x		To be used with digital processing functions, such as averaging and decimation filers.
DDR bit clock frequency	6x, 5x, 7x	6x	For 12x, 10x, and 14x serialization factors respectively.
Frame clock frequency	1x sample rate	1x	

12x Serialization with DDR Bit Clock and 1x Frame Clock

The 12-bit ADC data are serialized and output over one LVDS pair per channel along with a 6x bit clock and a 1x frame clock, as shown in Figure 102. The output data rate is a 12x sample rate, and maximum data rates up to 960 Mbps are supported.

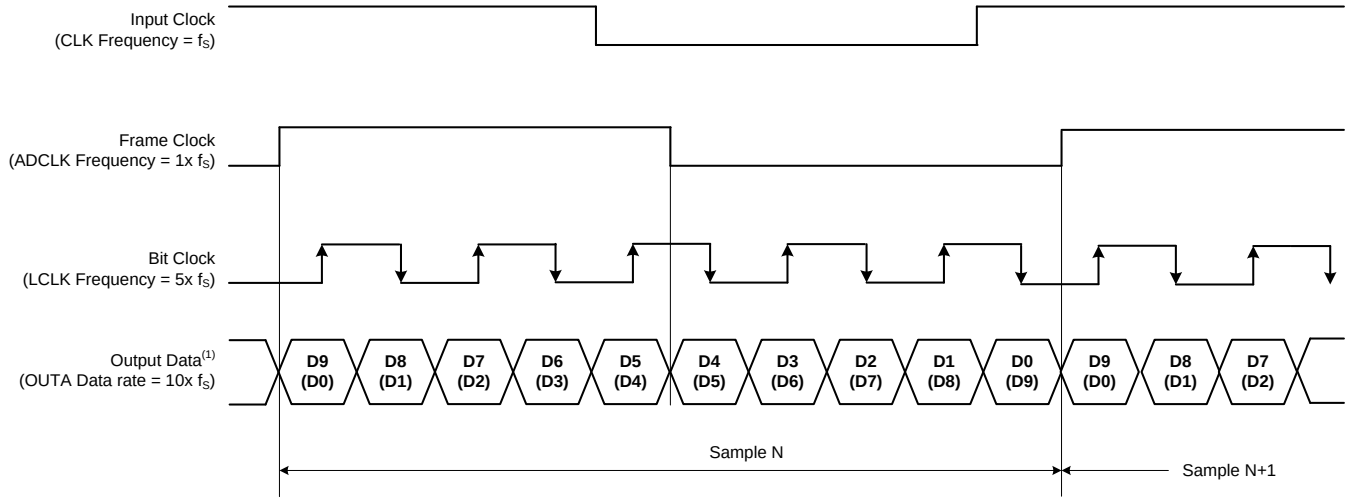


(1) The upper data bit is the MSB-first mode data bit and the lower data bit is the LSB-first mode data bit.

Figure 102. LVDS Output Interface Timing Diagram (12x Serialization)

10x Serialization with DDR Bit Clock and 1x Frame Clock

The 10 upper bits of the 12-bit ADC data are serialized and output over one LVDS pair per channel along with a 5x bit clock and a 1x frame clock, as shown in Figure 103. The output data rate is a 10x sample rate, and maximum data rate ups to 1 Gbps are supported.



(1) The upper data bit is the MSB-first mode data bit and the lower data bit is the LSB-first mode data bit.

Figure 103. LVDS Output Interface Timing Diagram (10x Serialization)

PROGRAMMABLE LCLK PHASE

The device enables the edge of the output bit clock (LCLK) to be programmed with the PHASE_DDR register bits. The default value of PHASE_DDR after reset is '10'. The default phase is shown in Figure 104.

The phase can also be changed by changing the value of the PHASE_DDR[1:0] bits, as shown in Figure 105.

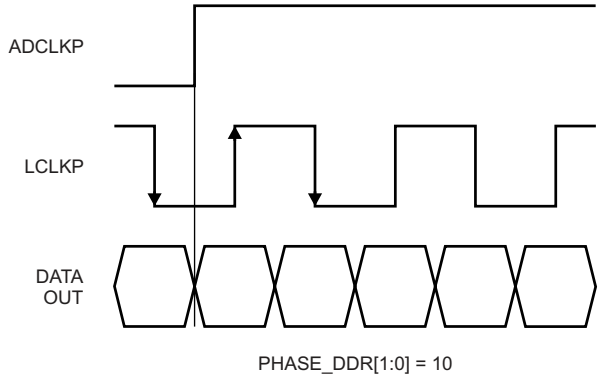


Figure 104. Default LCLK Phase

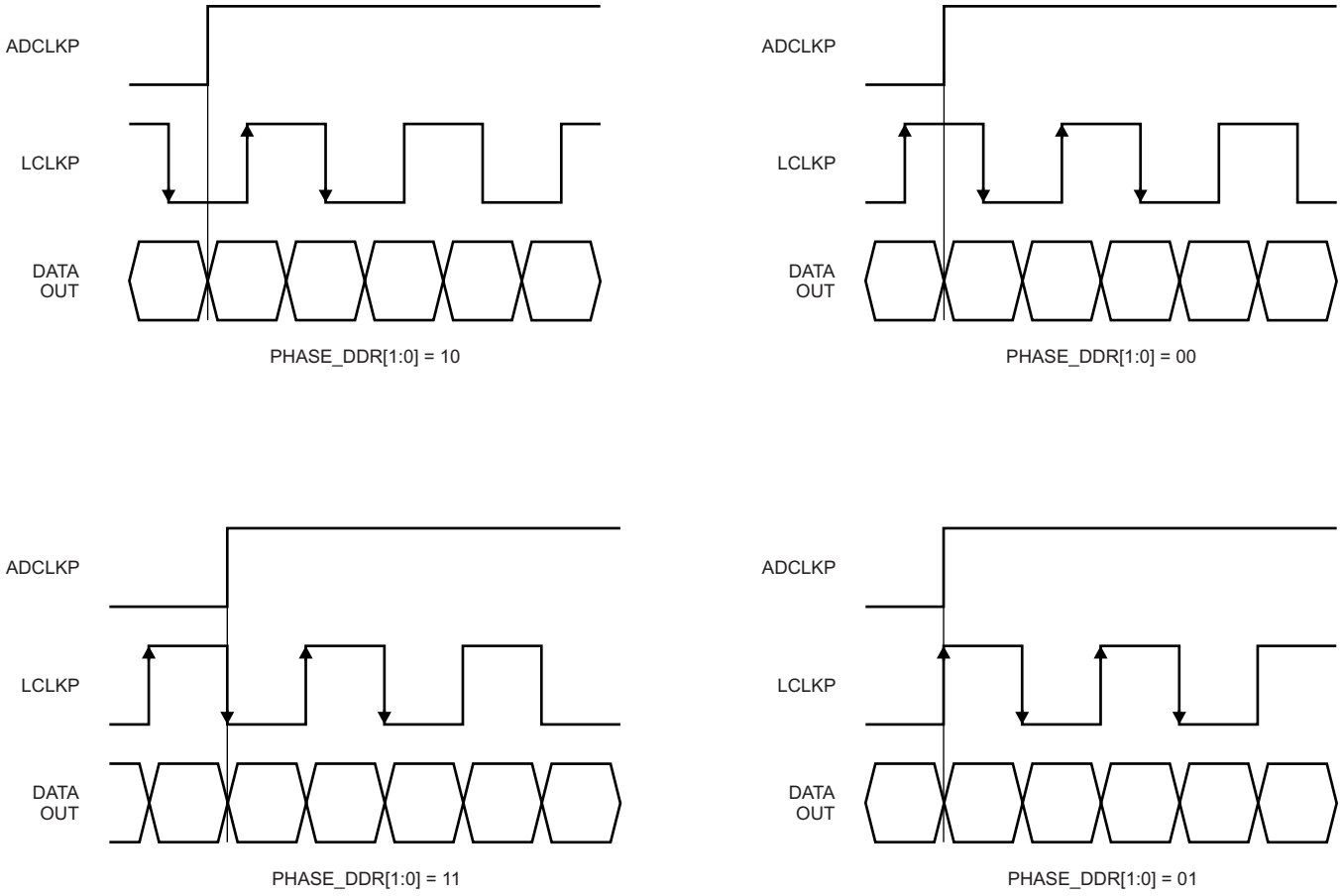


Figure 105. Programmable LCLK Phases

PROGRAMMABLE LVDS OUTPUT CLOCK AND DATA DELAYS

The device enables the edges of the output data and output bit clock to be delayed with the DELAY_DATA and DELAY_LCLK register bits.

Figure 106 details the timing of the output data and clock edge movements. Table 68 and Table 69 show the register settings and corresponding delay values for the data and clock edge movements.

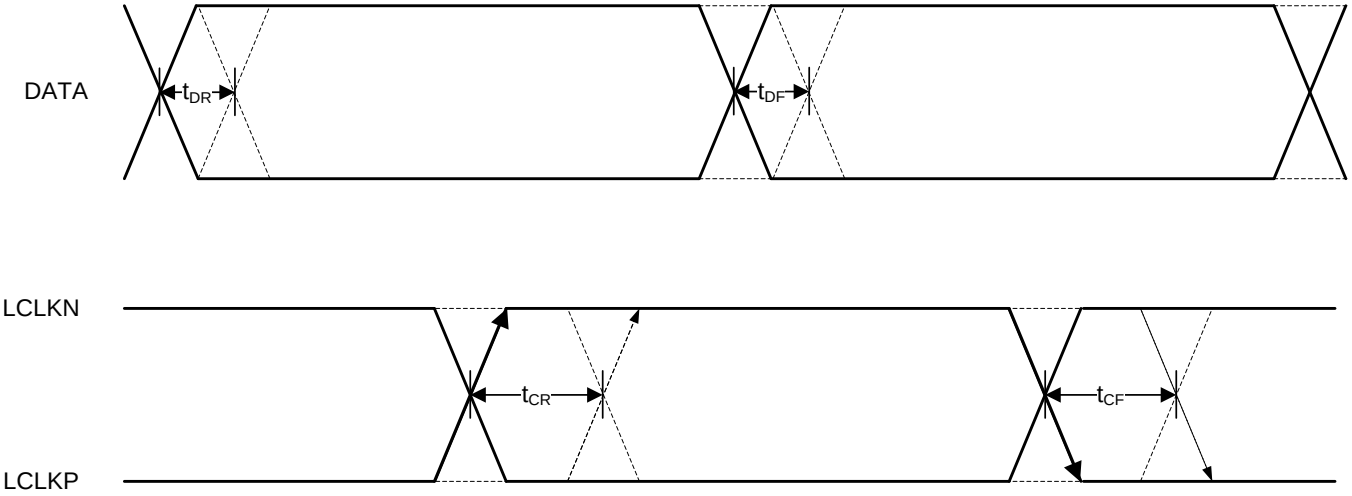


Figure 106. LVDS Interface Output Data and Clock Edge Movement

Table 68. LVDS Interface Output Data Delay Settings(1)

DELAY_DATA_R[1:0]		DATA DELAY, RISING CLOCK EDGE(2) (t_{DR}, typical, ps)	DELAY_DATA_F[1:0]		DATA DELAY, FALLING CLOCK EDGE(2) (t_{DF}, typical, ps)
0	0	0	0	0	0
0	1	33	0	1	33
1	0	72	1	0	72
1	1	120	1	1	120

(1) Delay settings are the same for both 10x and 12x serialization modes.
(2) Positive value indicates that the data edge is delayed with respect to the clock, resulting in lower setup time and higher hold time

Table 69. LVDS Interface Output Clock Delay Settings(1)

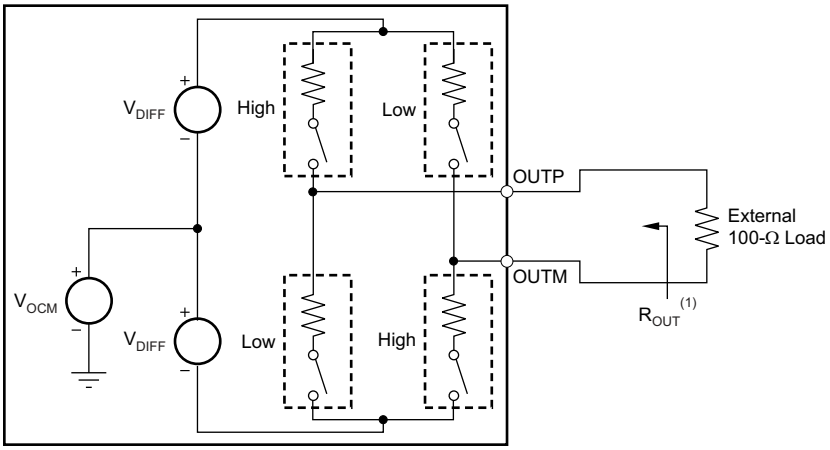
DELAY_LCLK_R[2:0]			CLOCK RISING EDGE DELAY(2) (t_{CR}, typical, ps)	DELAY_LCLK_F[2:0]			CLOCK FALLING EDGE DELAY(2) (t_{CF}, typical, ps)
0	0	0	-106	0	0	0	-120
0	0	1	-73	0	0	1	-87
0	1	0	-34	0	1	0	-48
0	1	1	14	0	1	1	0
1	0	0	0	1	0	0	-14
1	0	1	53	1	0	1	39
1	1	0	96	1	1	0	82
1	1	1	138	1	1	1	124

(1) Delay settings are the same for both 10x and 12x serialization modes.
(2) Negative value indicates that the clock edge is advanced with respect to the data edge, resulting in lower setup time and higher hold time. Positive value indicates that the clock edge is delayed with respect to the data edge, resulting in higher setup time and lower hold time

LVDS OUTPUT DATA AND CLOCK BUFFERS

The equivalent circuit of each LVDS output buffer is shown in Figure 107. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.

The V_{DIFF} voltage is nominally 400 mV, resulting in an output swing of ±400 mV with a 100-Ω external termination. The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, this impedance helps improve signal integrity.



(1) R_{OUT} = 100 Ω.

Figure 107. LVDS Buffer Equivalent Circuit

OUTPUT DATA FORMAT

Two output data formats are supported: twos complement and offset binary. These formats can be selected by the BTC_MODE serial interface register bit. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overload, the 12-bit output data (D[11:0]) is FFFh in offset binary output format and 7FFh in twos complement output format. For a negative input overload, the output data is 000h in offset binary output format and 800h in twos complement output format.

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. Refer to the EVM User Guide, *ADS5295, 8-Channel ADC Evaluation Module,* (SLAU442) for details on layout and grounding.

Supply Decoupling

Minimal external decoupling can be used without loss in performance because the device already includes internal decoupling. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed as close as possible to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to the digital ground internally. Therefore, the exposed pad must be soldered to the ground plane for best thermal and electrical performance.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth: The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay: The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (jitter): The sample-to-sample variation in aperture delay.

Clock Pulse Width (duty cycle): The duty cycle of a clock signal is the ratio of the time that the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate: The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate, unless otherwise noted.

Minimum Conversion Rate: The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL): An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL): INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function, measured in units of LSBs.

Gain Error: Gain error is the deviation of the actual ADC input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}, respectively. To a first-order approximation, the total gain error is (E_{TOTAL} ~ E_{GREF} + E_{GCHAN}). For example, if E_{TOTAL} = ±0.5%, then the full-scale input varies from [(1 – 0.5 / 100) × FS_{IDEAL}] to [(1 + 0.5 / 100) × FS_{IDEAL}].

Offset Error: Offset error is the difference, given in number of LSBs, between the actual average ADC idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift: The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference of T_{MAX} – T_{MIN}.

Signal-to-Noise Ratio (SNR): SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SNR = 10\ Log^{10} \frac{P_S}{P_N} \quad (9)$$

Signal-to-Noise and Distortion (SINAD): SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components, including noise (P_N) and distortion (P_D), but excluding dc. SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SINAD = 10\ Log^{10} \frac{P_S}{P_N + P_D} \quad (10)$$

Effective Number of Bits (ENOB): ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (11)$$

Total Harmonic Distortion (THD): THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D). THD is typically given in units of dBc (dB to carrier).

$$THD = 10\ Log^{10} \frac{P_S}{P_N} \quad (12)$$

Spurious-Free Dynamic Range (SFDR): SFDR is the ratio of power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3): IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2 f_1 – f_2$ or $2 f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

AC Power-Supply Rejection Ratio (AC PSRR): AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20 \text{ Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad \text{(Expressed in dBc)} \tag{13}$$

Voltage Overload Recovery: The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This recovery is tested by separately applying a sine-wave signal with 6-dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR): CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$CMRR = 20 \text{ Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad \text{(Expressed in dBc)} \tag{14}$$

CROSSTALK: (only for multichannel ADCs) Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from a channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5296ARGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5296	Samples
ADS5296ARGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5296	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

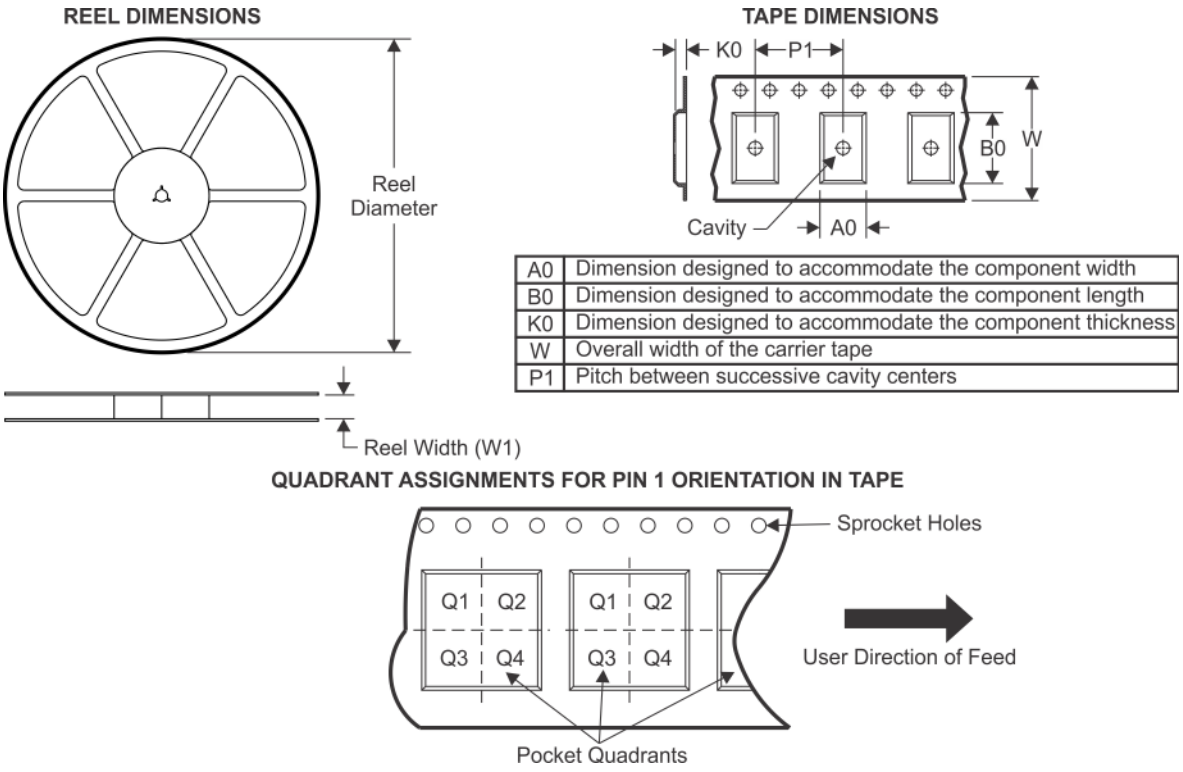
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

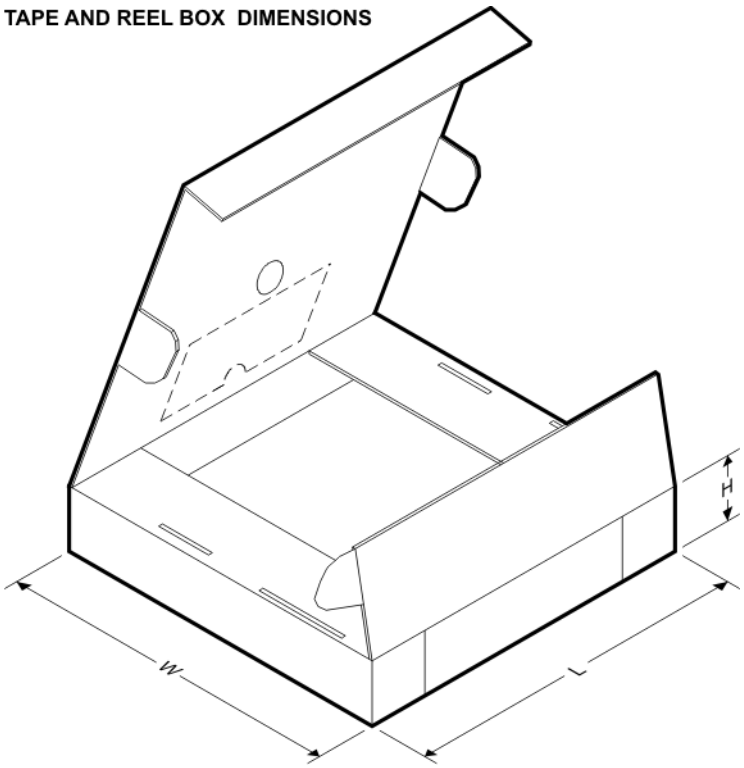


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5296ARGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5296ARGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

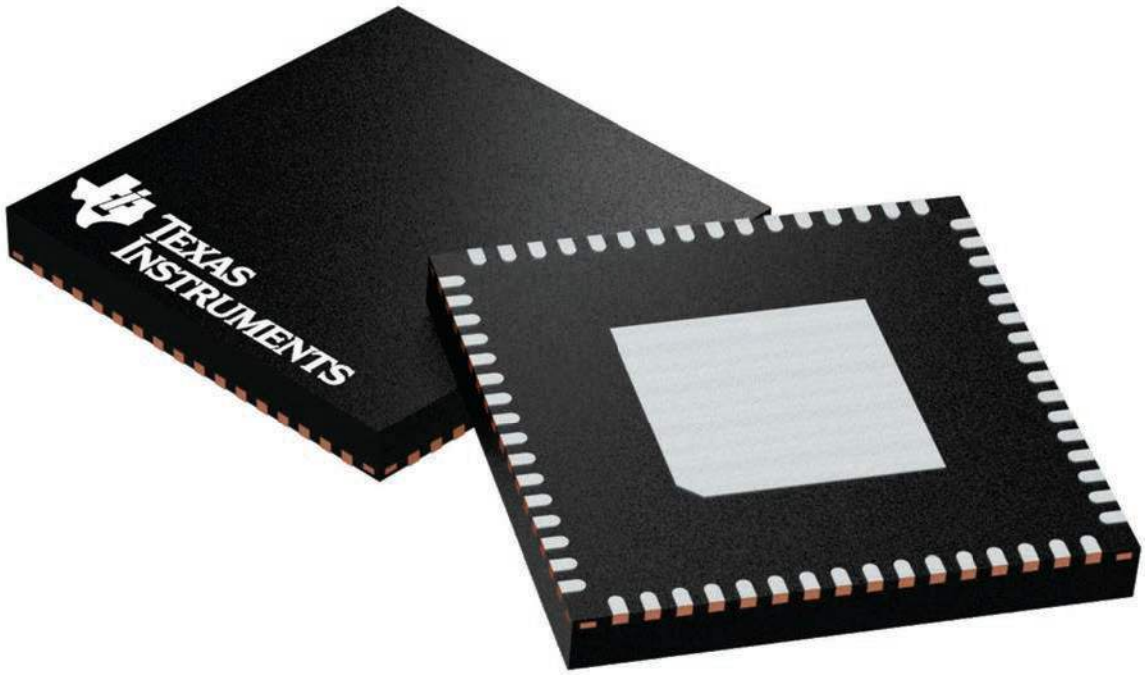
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

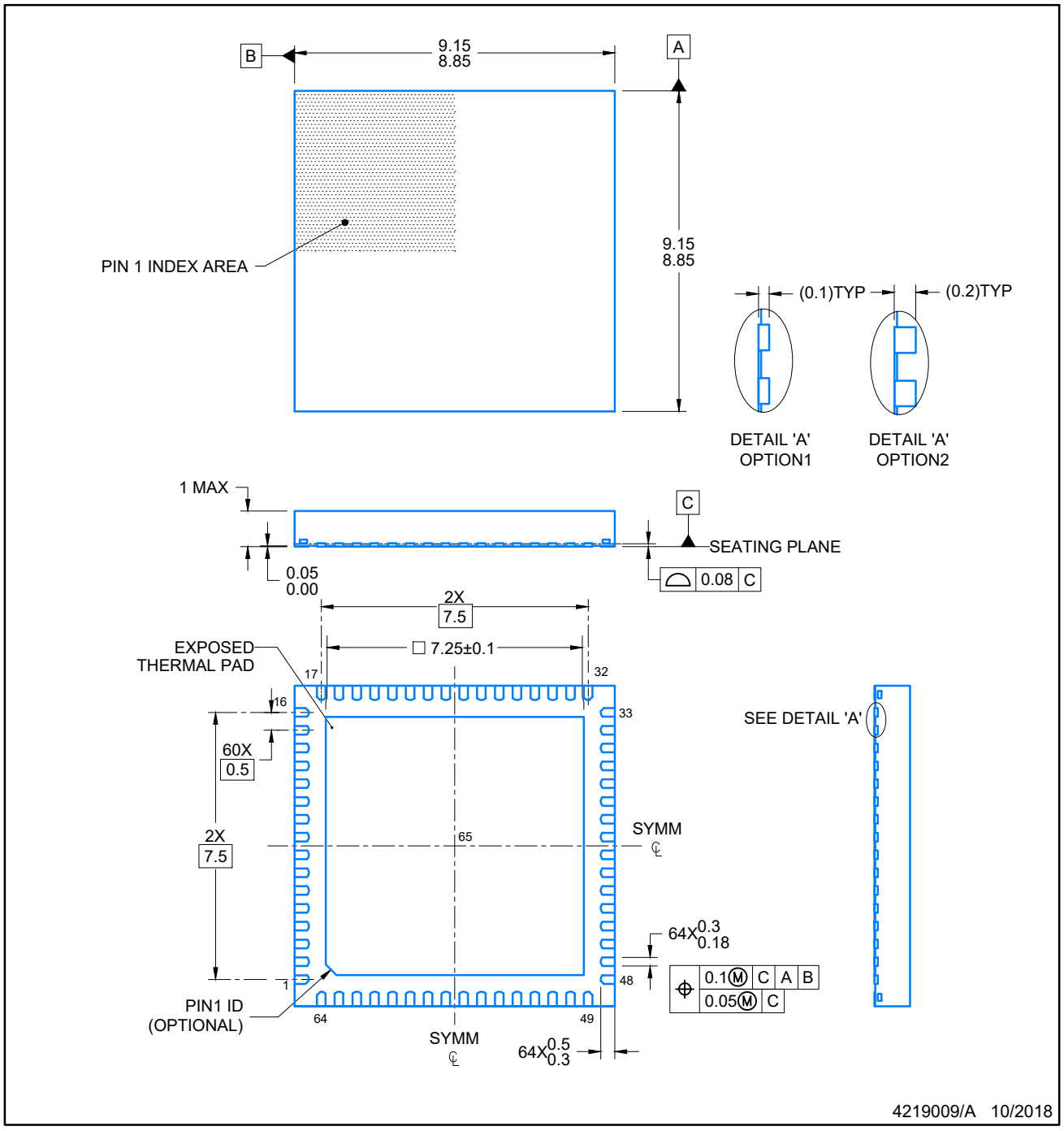
4224597/A

PACKAGE OUTLINE

RGC0064A

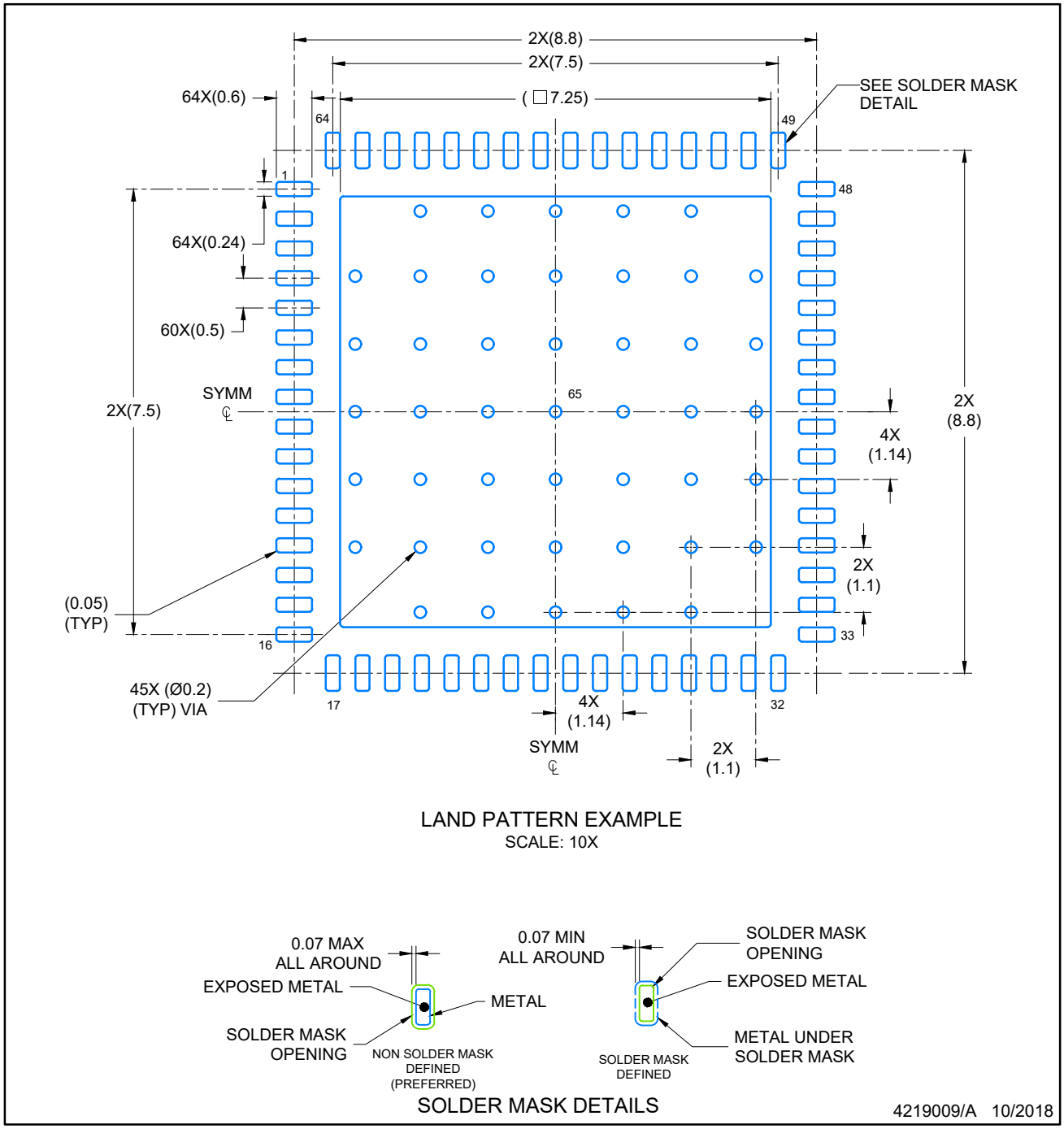
VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 10X

SOLDER MASK DETAILS

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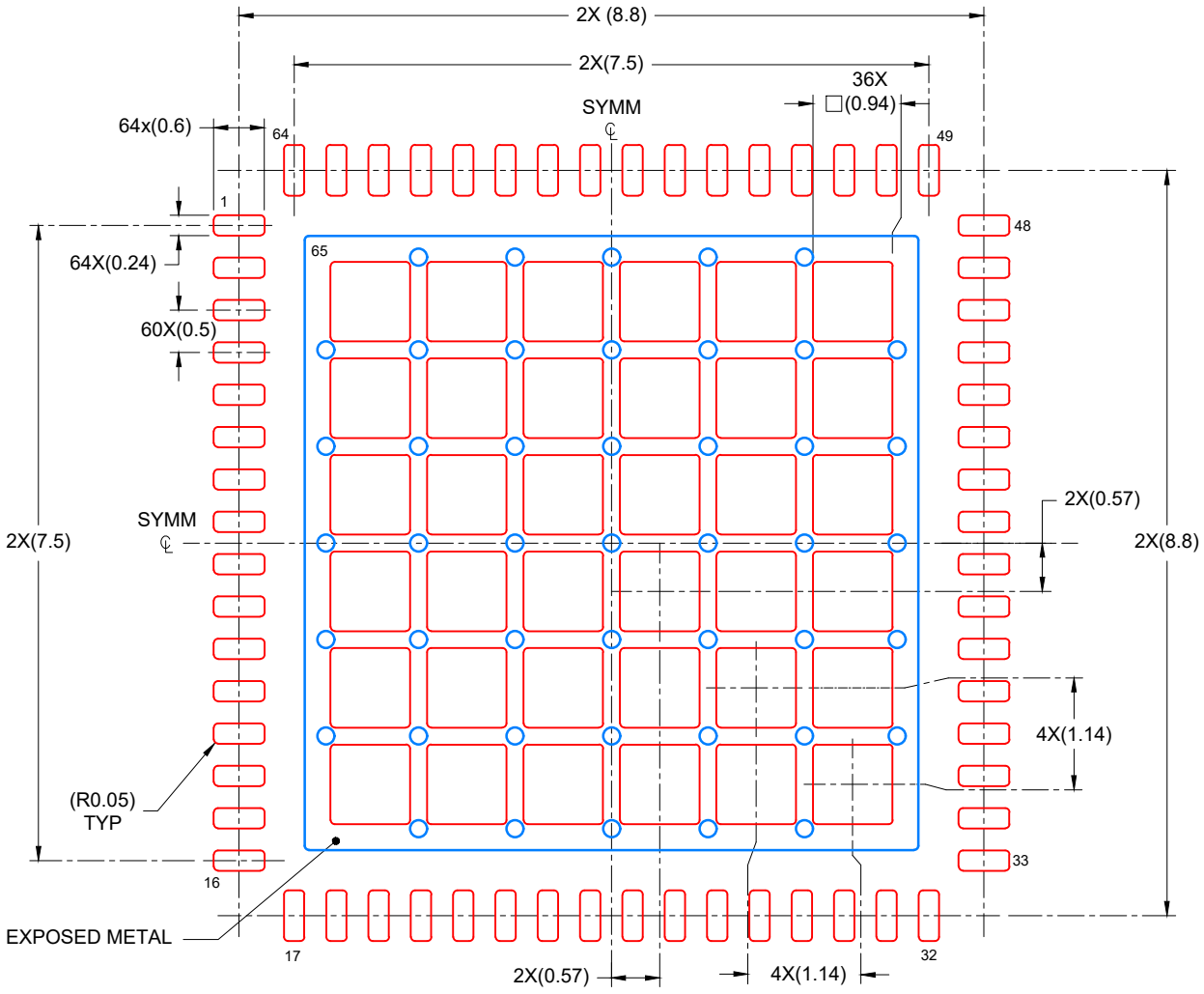
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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