

# CSD13306W 12 V N Channel NexFET™ Power MOSFET

## 1 Features

- Ultra Low on Resistance
- Low  $Q_g$  and  $Q_{gd}$
- Small Footprint 1 x 1.5 mm
- Low Profile 0.62 mm Height
- Pb Free
- RoHS Compliant
- Halogen Free

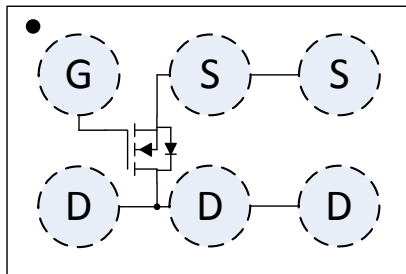
## 2 Applications

- Battery Management
- Load Switch
- Battery Protection

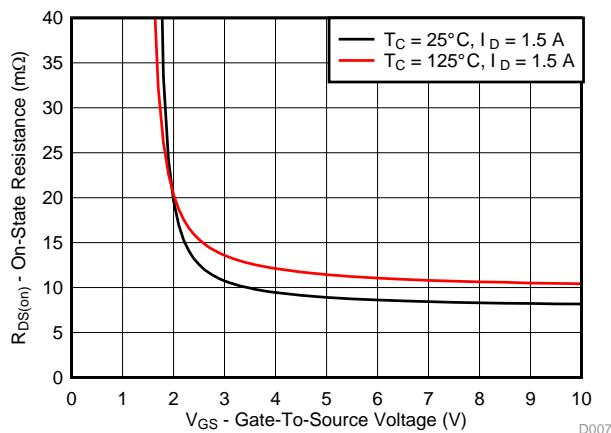
## 3 Description

This 8.8 m $\Omega$ , 12 V, N-Channel device is designed to deliver the lowest on resistance and gate charge in a small 1 x 1.5 mm outline with excellent thermal characteristics and an ultra low profile.

Top View

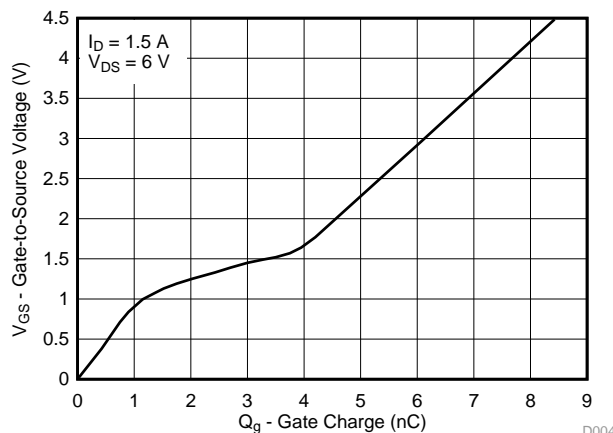


$R_{DS(on)}$  vs  $V_{GS}$



D007

Gate Charge



D004

## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	12		V
$Q_g$	Gate Charge Total (4.5 V)	8.6		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	3.0		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	12.9	m $\Omega$
		$V_{GS} = 4.5\text{ V}$	8.8	m $\Omega$
$V_{GS(th)}$	Voltage Threshold	1.0		V

## Ordering Information<sup>(1)</sup>

Device	Qty	Media	Package	Ship
CSD13306W	3000	7-Inch Reel	1.0 mm x 1.5 mm Wafer Level Package	Tape and Reel
CSD13306WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	12	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 10$	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	3.5	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	44	A
$P_D$	Power Dissipation <sup>(3)</sup>	1.9	W
$T_{stg}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range		

(1) Device Operating at a temperature of  $105^\circ\text{C}$

(2) Min Cu Typ  $R_{\theta JA} = 230^\circ\text{C/W}$ , Pulse width  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$

(3) Max Cu Typ  $R_{\theta JA} = 65^\circ\text{C/W}$



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>6 Device and Documentation Support</b> .....	<b>7</b>
<b>2 Applications</b> .....	<b>1</b>	6.1 Trademarks .....	7
<b>3 Description</b> .....	<b>1</b>	6.2 Electrostatic Discharge Caution .....	7
<b>4 Revision History</b> .....	<b>2</b>	6.3 Glossary .....	7
<b>5 Specifications</b> .....	<b>3</b>	<b>7 Mechanical, Packaging, and Orderable Information</b> .....	<b>8</b>
5.1 Electrical Characteristics .....	3	7.1 CSD13306W Package Dimensions .....	8
5.2 Thermal Information .....	3	7.2 Tape and Reel Information .....	9
5.3 Typical MOSFET Characteristics .....	4		

## 4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  unless otherwise stated

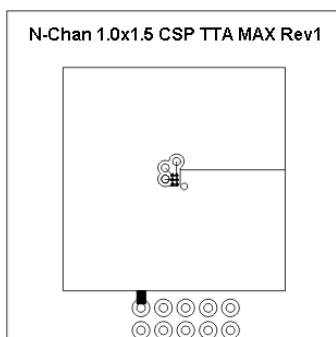
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	12			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 10\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.7	1.0	1.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}, I_D = 1.5\text{ A}$		12.9	15.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}$		8.8	10.2	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 1.2\text{ V}, I_D = 1.5\text{ A}$		15		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V}, f = 1\text{ MHz}$		1050	1370	pF
$C_{OSS}$	Output Capacitance			324	421	pF
$C_{RSS}$	Reverse Transfer Capacitance			226	294	pF
$R_g$	Gate Resistance		4.2	8.4		$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 6\text{ V}, I_D = 1.5\text{ A}$		8.6	11.2	nC
$Q_{gd}$	Gate Charge Gate-to-Drain			3.0		nC
$Q_{gs}$	Gate Charge Gate-to-Source			1.1		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.2		nC
$Q_{OSS}$	Output Charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		3.3		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1.5\text{ A}$ $R_G = 4\ \Omega$		7		ns
$t_r$	Rise Time			11		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
$t_f$	Fall Time			8		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_S = 1.5\text{ A}, V_{GS} = 0\text{ V}$		0.7	1.0	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 6\text{ V}, I_F = 1.5\text{ A}, di/dt = 200\text{ A}/\mu\text{s}$		14.8		nC
$t_{rr}$	Reverse Recovery Time			23		ns

### 5.2 Thermal Information

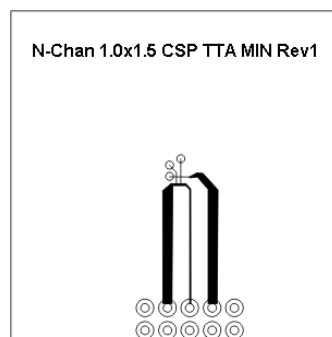
 $T_A = 25^\circ\text{C}$  unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)</sup>		230		$^\circ\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance <sup>(2)</sup>		65		

(1) Device mounted on FR4 material with minimum Cu mounting area

(2) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.


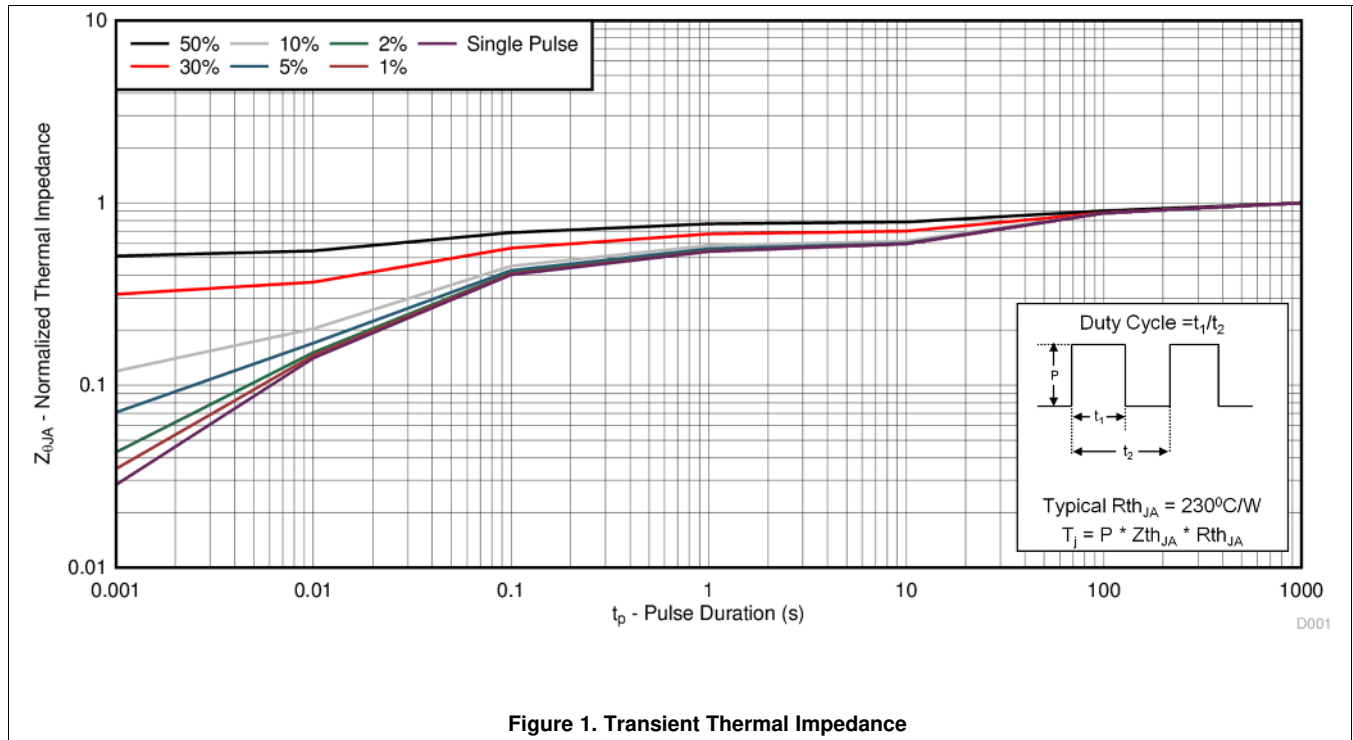
Typ  $R_{\theta JA} = 65^\circ\text{C}/\text{W}$   
when mounted on  
1 inch<sup>2</sup> of 2 oz. Cu.



Typ  $R_{\theta JA} = 230^\circ\text{C}/\text{W}$   
when mounted on  
minimum pad area of  
2 oz. Cu.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

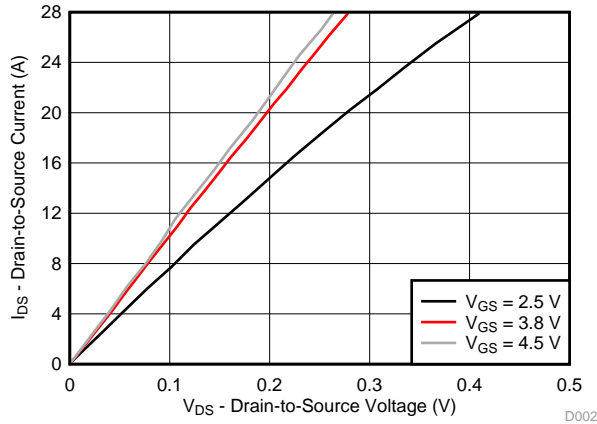


Figure 2. Saturation Characteristics

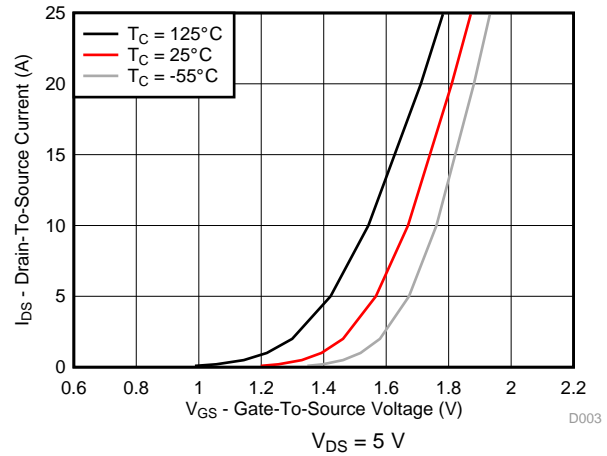


Figure 3. Transfer Characteristics

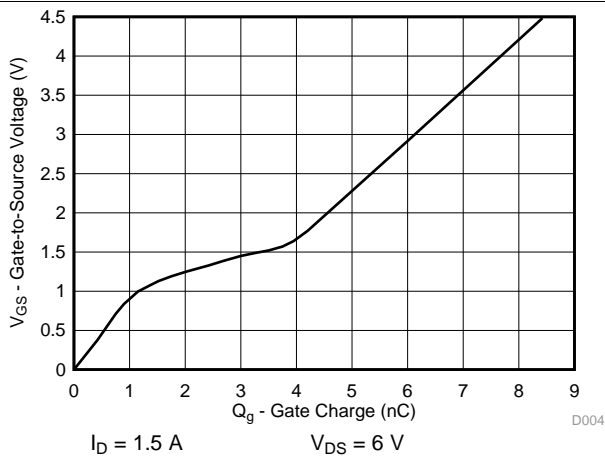


Figure 4. Gate Charge

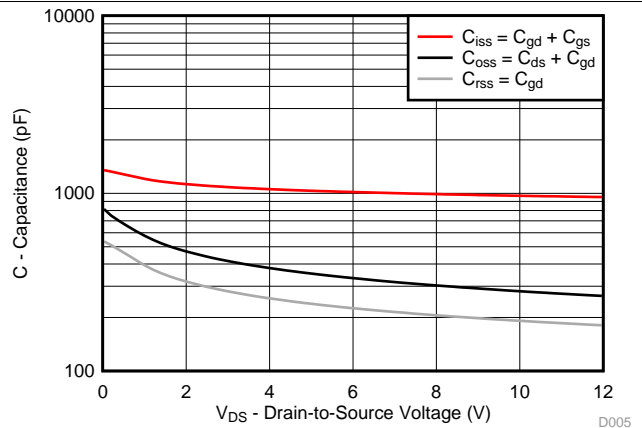


Figure 5. Capacitance

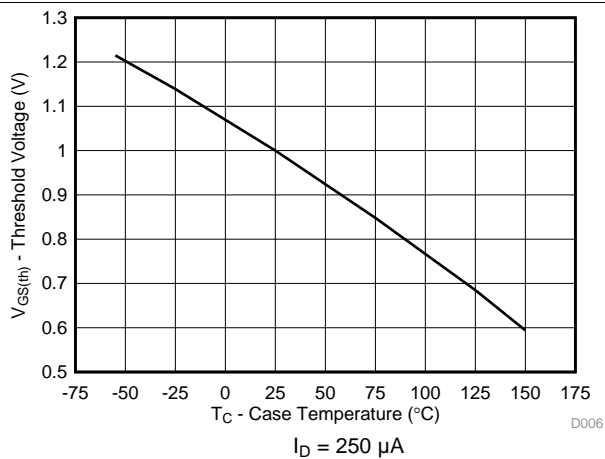


Figure 6. Threshold Voltage vs Temperature

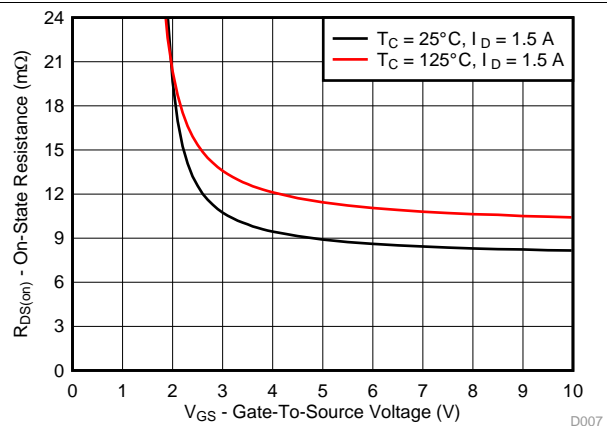
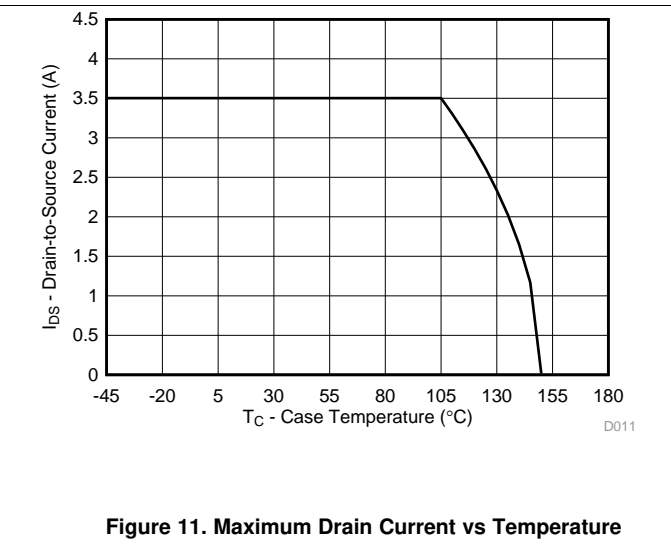
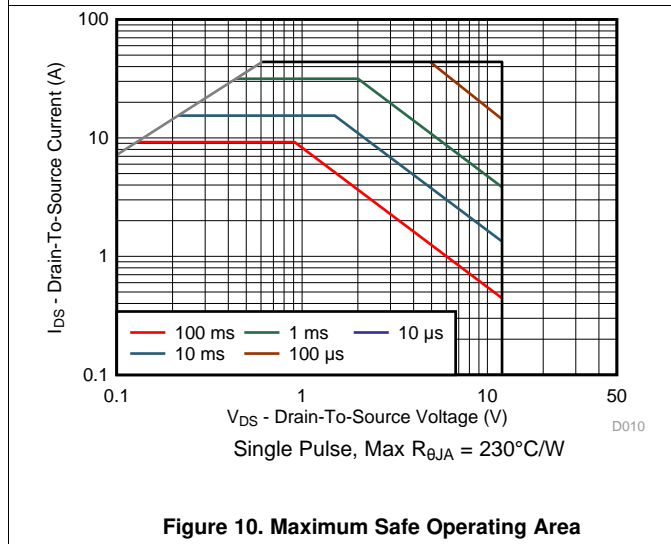
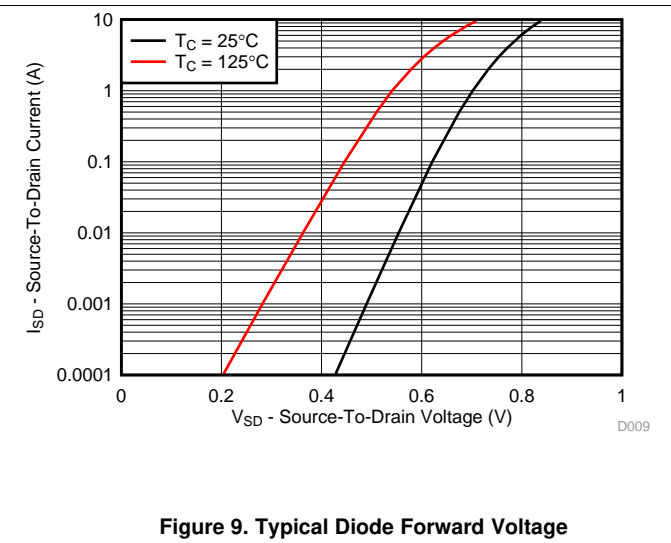
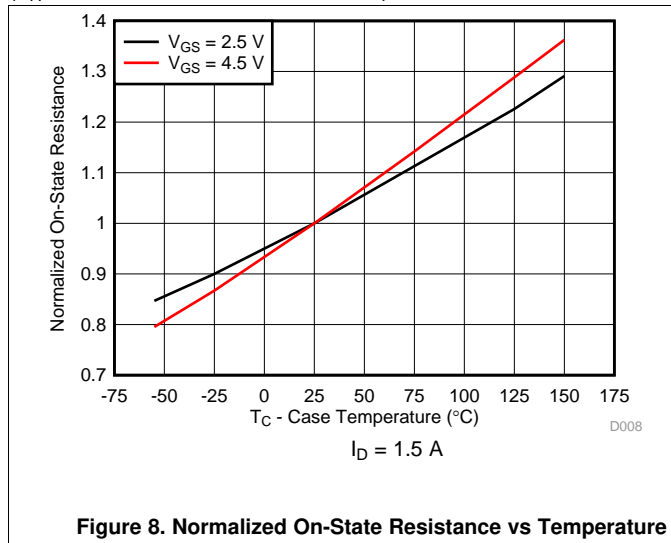


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

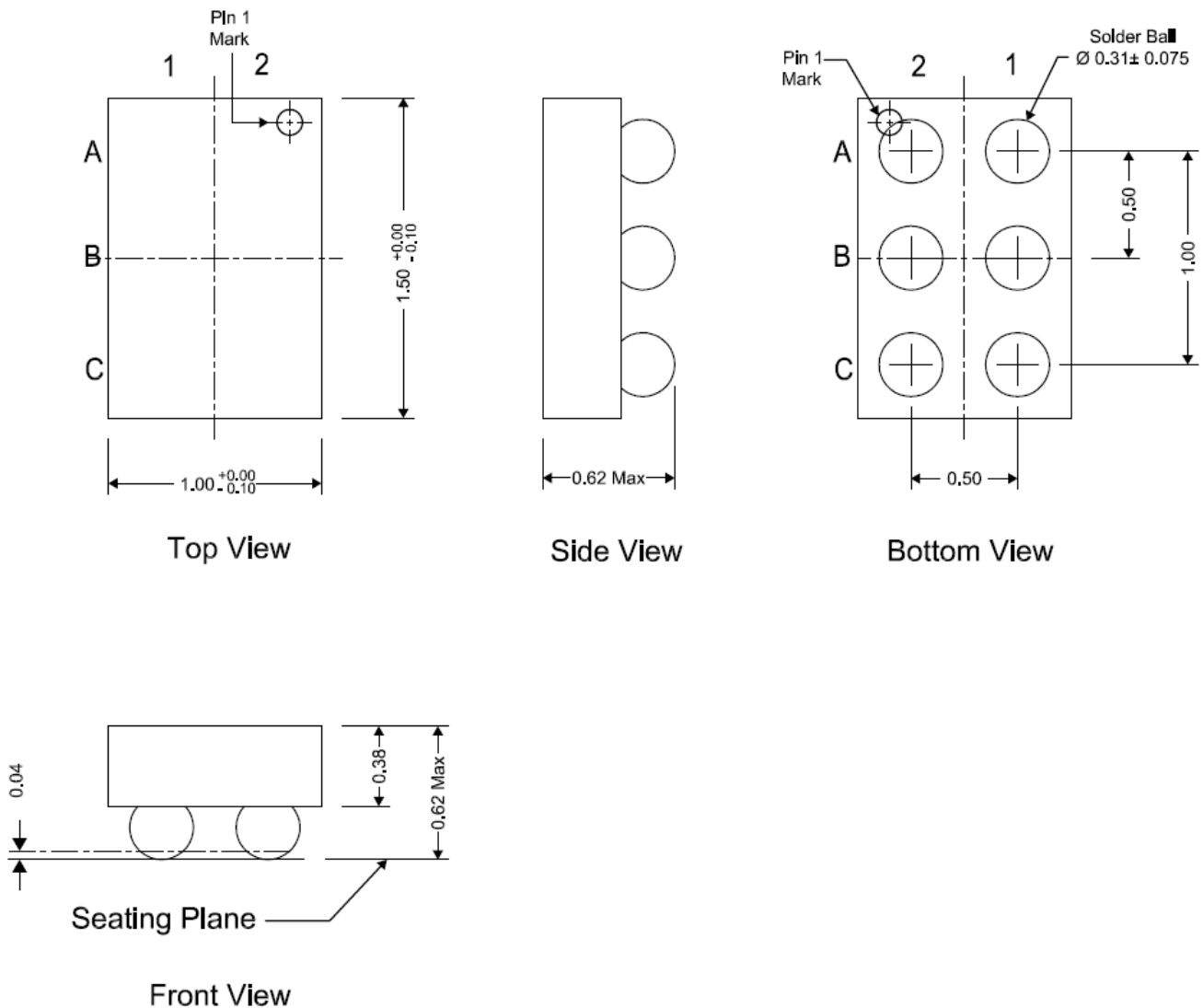
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 CSD13306W Package Dimensions



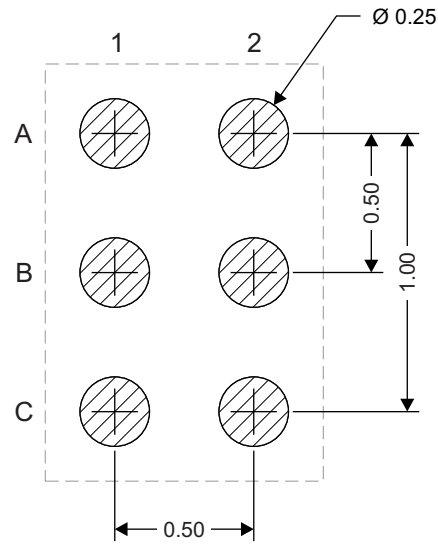
NOTE: All dimensions are in mm (unless otherwise specified)

**Pinout**

POSITION	DESIGNATION
C2, B2	Source
A2	Gate
A1, B1, C1	Drain



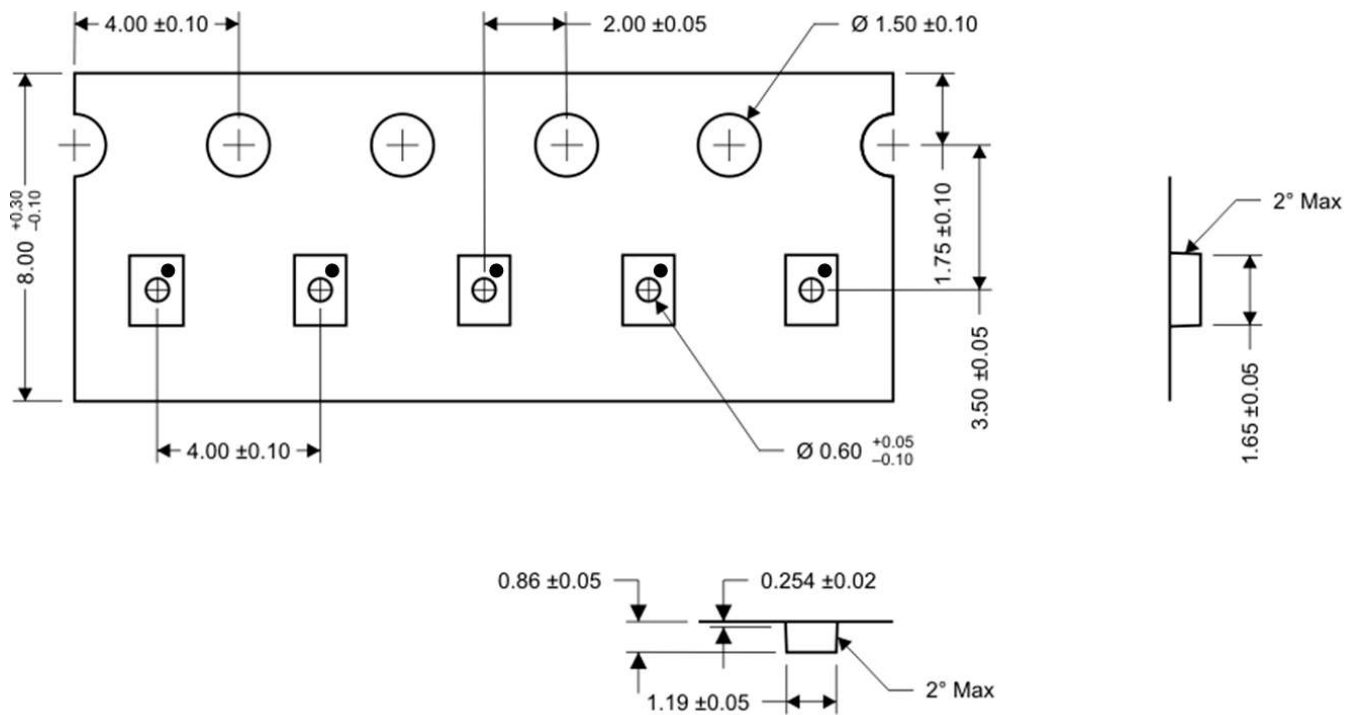
### Land Pattern Recommendation



M0158-01

NOTE: All dimensions are in mm (unless otherwise specified)

### 7.2 Tape and Reel Information



M0159-01

NOTE: All dimensions are in mm (unless otherwise specified)

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13306W	ACTIVE	DSBGA	YZC	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		13306	<a href="#">Samples</a>
CSD13306WT	ACTIVE	DSBGA	YZC	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	13306	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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