LT3040EDD
20V, 200mA, Ultralow Noise, Ultrahigh PSRR Precision DAC/Reference Buffer

DESCRIPTION

Demo board DC2783A features the LT®3040, a 200mA high performance, robust voltage reference/DAC buffer. LT3040 has ultralow output noise, ultrahigh power supply rejection ratio (PSRR) and low dropout voltage for powering noise sensitive, high accuracy systems.

DC2783A has two inputs: V^+ and V_{IN}. V^+ supplies power to the buffer, operating over a range from 2V to 20V. V_{IN} is the regulation set-point for the output with a range from 0V to 15V. Current limit is programmable by connecting a resistor, R3, from ILIM to GND. The ILIM can also serve as a current monitor pin with a range from 0V to 300mV.

LT3040 has fast start capability. Connecting FS pin across an input low pass filter resistor, R2, fast starts the LT3040. Fast start circuitry is typically triggered active if $V_{FS} - V_{IN} \geq 100mV$ and stays active until $V_{FS} - V_{IN} \leq 7mV$. If fast start functionality is not needed, connect FS to V_{IN} by setting R2 to 0Ω and applying the input voltage at FS.

LT3040 has a fault flag to indicate faults at the output. Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback and thermal limit with hysteresis.

The LT3040 datasheet gives a complete description of the part, operation and applications information. The datasheet must be read in conjunction with this Demo Manual for demonstration circuit DC2783A. The LT3040 is assembled in a 12-lead MSOP and a 10-lead (3mm x 3mm) plastic DFN package with an exposed pad on the bottom-side of the IC. Proper board layout is essential for maximum thermal performance.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range (V^+)	I_{OUT} = 150mA, V_{OUT} = 3.3V	3.8		20	VDC
Supply Voltage Range* (V^+)	I_{OUT} = 200mA, V_{OUT} = 3.3V	3.8		15.5	VDC
Dropout Voltage	$V^+ = V_{IN}$ = 3.3V, I_{OUT} = 200mA		0.35		VDC
Shutdown Supply Current (Iv^+)	JP1 = OFF, V^+= 5V		0.3		µA

*The maximum supply input voltage for 200mA load current is set by the 60°C temperature rise of LT3040 on the demo circuit. Higher input voltage can be reached if larger copper area or force-air cooling is applied. The output current is also limited by the differential of supply input and output voltage, please refer the datasheet for details.

BOARD PHOTO

QUICK START PROCEDURE

Demonstration circuit DC2783A is easy to set up to evaluate the performance of the LT3040EDD. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Connect Load between the VOUT and GND terminals.

2. With power off, connect the supply power to the V^+ and GND terminals.

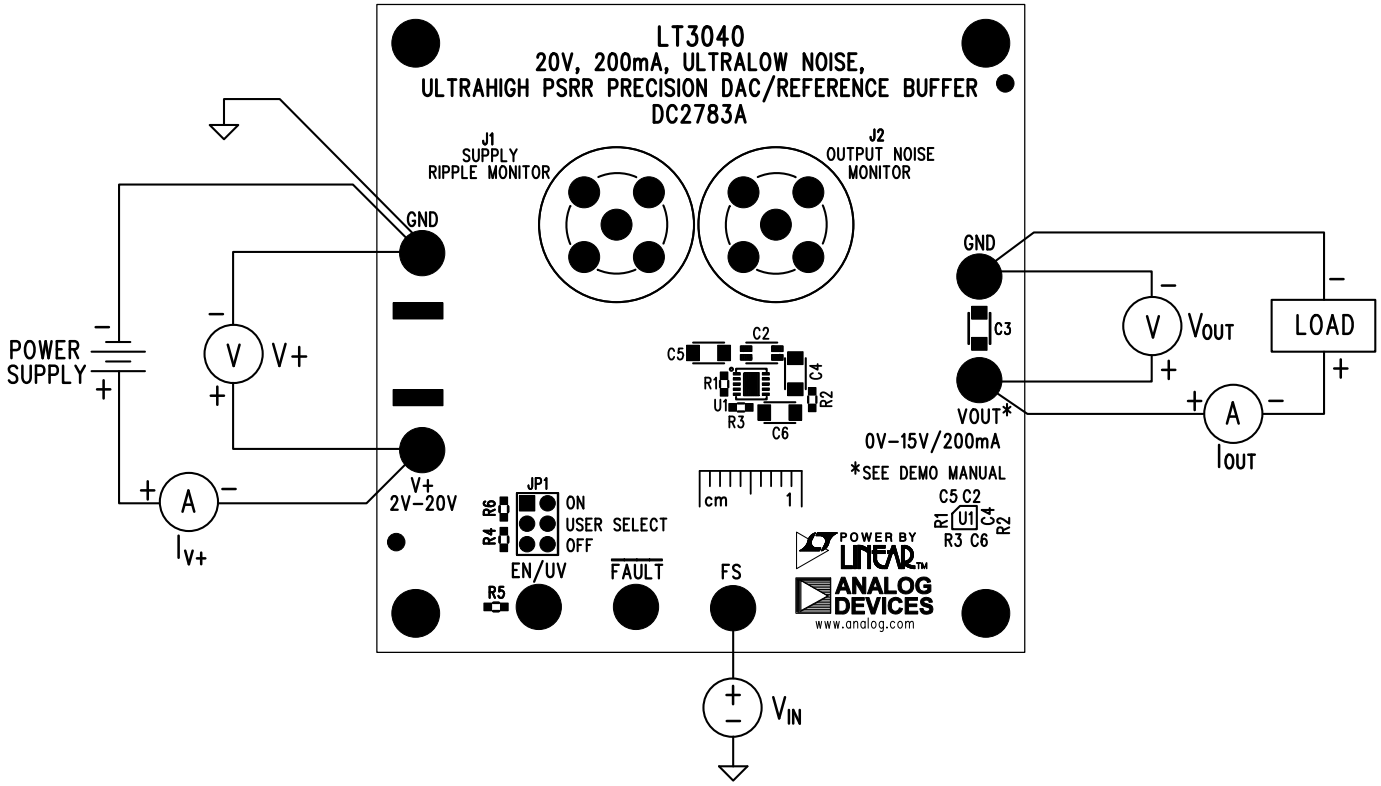
3. Connect the input voltage VIN at FS pin.

4. Make sure the shunt of JP1 is at ON option.

5. Turn the input power supply on and make sure the voltage is between 3.8V and 20V.

6. To measure the output noise, please refer to Application Note AN70 and AN159 for more precise techniques for measuring the output noise and PSRR.

7. R4 and R5 can define an accurate undervoltage lockout (UVLO) threshold when the shunt of JP1 at USER SELECT option.



*The maximum output current will be limited by internal current limit based on differential voltage of supply and output voltage, please refer to the datasheet.

Figure 1. Test procedure setup drawing for DC2783A

PCB LAYOUT

Best PSRR Performance: PCB Layout for Supply Trace

For applications where the LT3040 is supplied by an upstream switching converter, placing a capacitor directly at the LT3040's supply pin (V^+) results in AC current (at the switching frequency) to flow near the LT3040. Without careful attention to PCB layout, this relatively high frequency switching current generates an Electromagnetic Field (EMF) that couples to the LT3040 output, thereby degrading its effective PSRR. While highly dependent on the PCB, the switching pre-regulator, input capacitor size, among other factors, the PSRR degradation can easily be 30dB at 1MHz. This degradation is present even if the LT3040 is de-soldered from the board, because it effectively degrades the PSRR of the PC board itself. While negligible for conventional low PSRR LDOs or Voltage Buffers, LT3040's ultrahigh PSRR requires careful attention to higher order parasitics in order to realize the full performance offered by the voltage buffer.

The LT3040 demo board alleviates this degradation in PSRR by using a specialized layout technique. On layer 3, the supply trace (V^+) is highlighted in red, with the return path (GND) highlighted on the bottom layer together with supply capacitor C1. When an AC voltage is applied to the board, AC current flows on this path, thus generating EMF. This EMF couples to the output capacitor C2 and related traces, making PSRR appear worse than it actually is. **With the input trace directly above the return path, the EMFs are in opposite directions and consequently cancel each other out. Making sure these traces exactly overlap each other maximizes the cancellation effect and thus provides the maximum PSRR offered by the regulator.**

If the Voltage Reference or DAC used as an input to LT3040 is also powered by the switching regulator, similar layout technique should be used to connect the supply and return paths of these devices. Although the input filter created by R2 and C4 is supposed to attenuate the ripple at the input of the buffer (V_{IN}), minimizing the ripple fed through the Voltage Reference or DAC at the FS pin of LT3040 will result in the best PSRR performance possible.

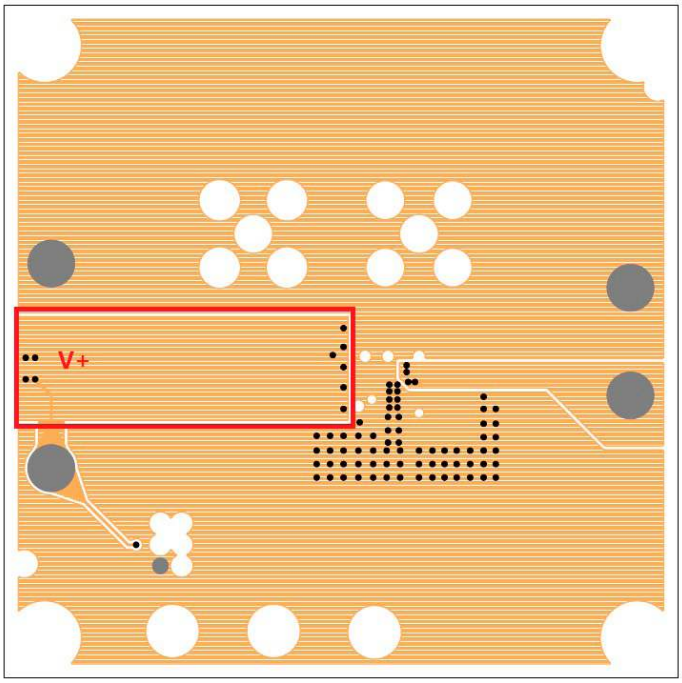


Figure 2. Layer 3 of DC2783A

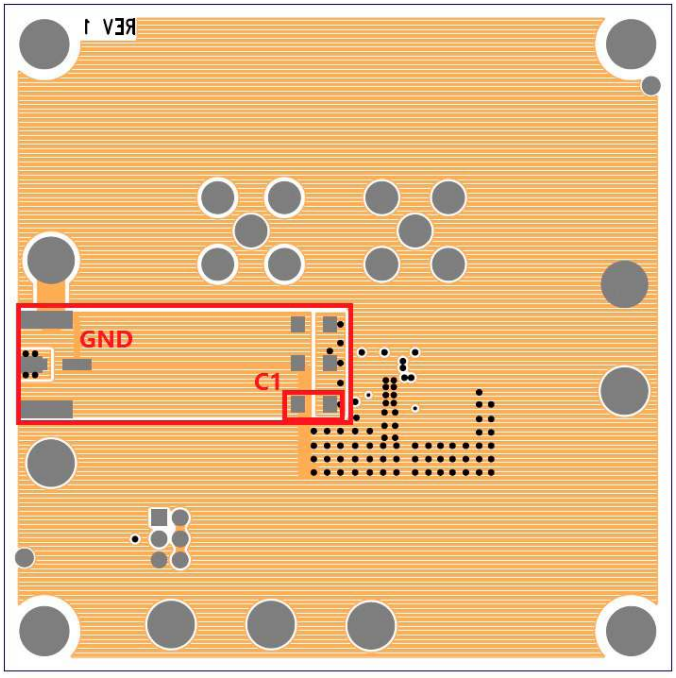


Figure 3. Bottom Layer of DC2783A

PCB LAYOUT

PCB Layout for Output Capacitor C2

For best accuracy and stability of the part, parasitic resistance and inductance should be minimized between the output capacitor and VFB and GND connections. Kelvin connecting the GND side of the input (VIN) capacitor (C4) to the GND of the output capacitor (C2) is also important. The solder joint that exists between the output capacitor terminal and pads on the board adds extra resistance and inductance. To minimize the effect of these parasitics, split capacitor pads are utilized. Pad 4 connects to the VFB pin, and Pad 1 connects to the input voltage capacitor ground. With the small current flowing through these connections, the impact of the solder joint on sensing accuracy and stability is eliminated.

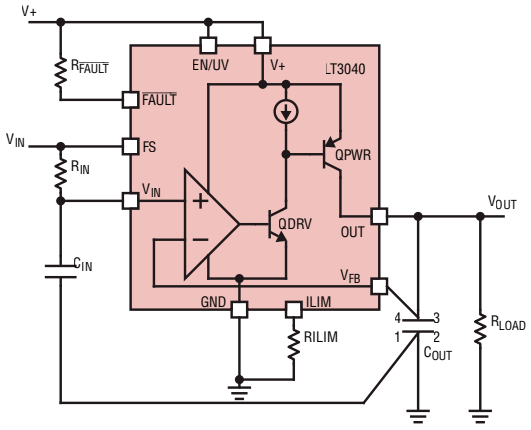


Figure 4. C2 and C4 connections for best performance

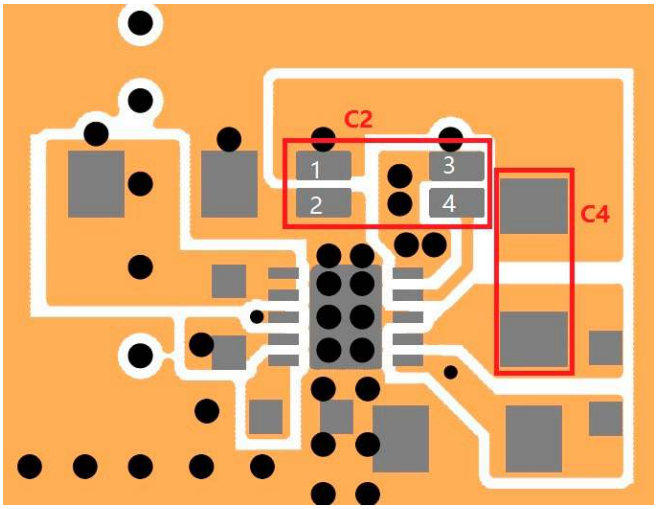
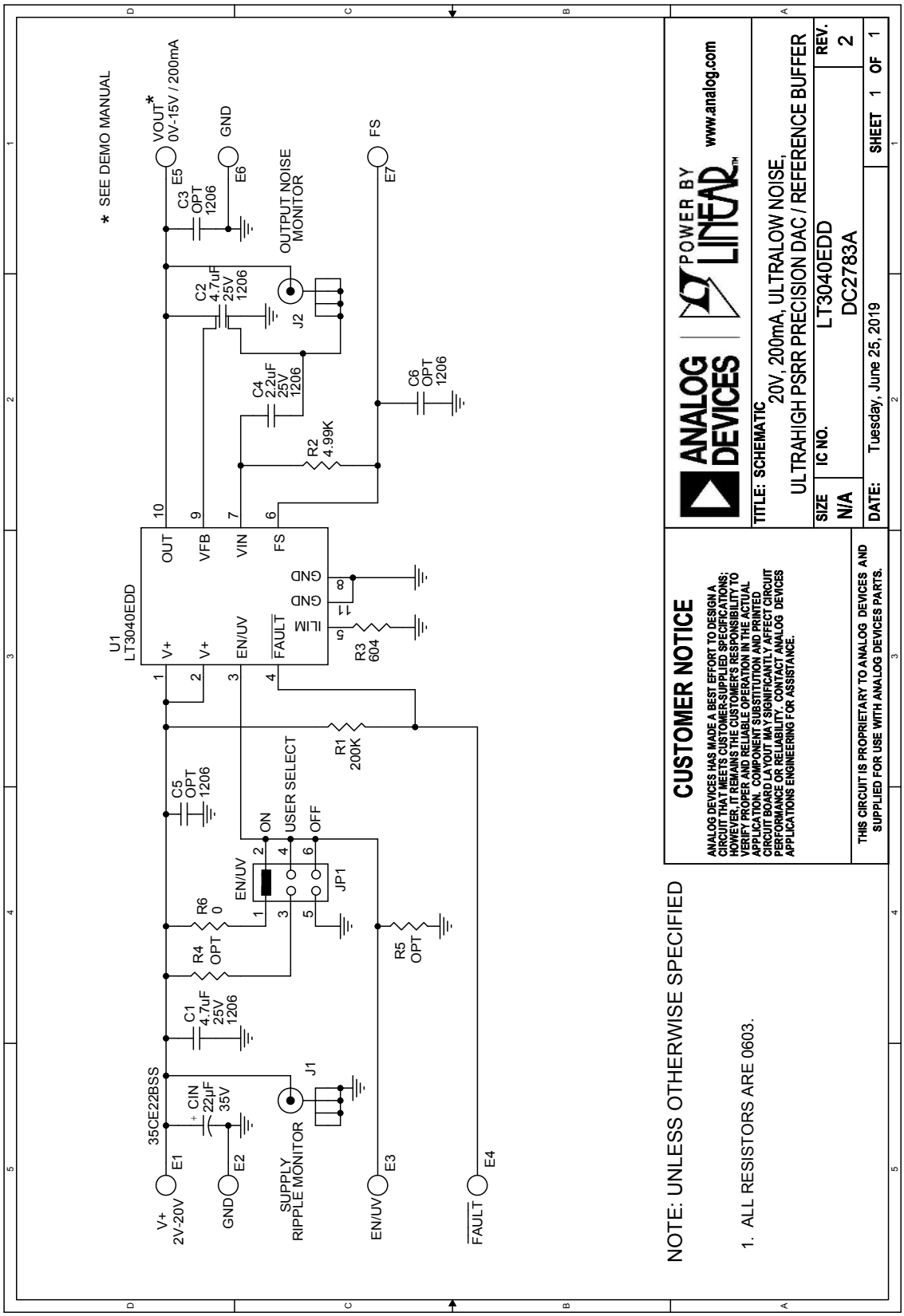


Figure 5. Split Pads for C2

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN	CAP., ALUM., 22µF, 35V, 5X5.4MM	SUN ELECTRONIC INDUSTRIES CORP., 35CE22BSS
2	2	C1, C2	CAP., X7R, 4.7uF, 25V, 10%, 1206	MURATA, GRM31CR71E475KA88L
3	1	C4	CAP., X7R, 2.2uF, 25V, 10%, 1206	MURATA, GRM31MR71E225KA93L
4	1	R1	RES., 200K, 1/10W, 1%, 0603	VISHAY, CRCW0603200KFKEA
5	1	R2	RES., 4.99K, 1/10W, 1%, 0603	VISHAY, CRCW06034K99FKEA
6	1	R3	RES., 604, 1/10W, 1%, 0603	PANASONIC, ERJ-3EKF6040V
7	1	R6	RES., 0 OHM, 1/4W, 0603	VISHAY, CRCW06030000Z0EA
8	1	U1	I.C., LT3040EDD, 10DFN	ANALOG DEVICES INC., LT3040EDD#PBF
Additional Demo Board Circuit Components				
9	0	C3, C5, C6(OPT)	CAP., OPTION, 1206	
10	0	R4, R5(OPT)	RES., OPTION, 0603	
Hardware: For Demo Board Only				
11	7	E1-E7	TESTPOINT, TURRET, .094"	MILL-MAX, 2501-2-00-80-00-00-07-0
12	1	JP1	HEADER 3 PIN 0.079 DOUBLE ROW	WURTH ELEKTRONIK, 62000621121
13	1	XJP1	SHUNT, .079" CENTERf	WURTH ELEKTRONIK, 60800213421
14	2	J1, J2	CONN, BNC, 5 PINS	CONNEX, 112404
15	4	MH1-MH4	STAND-OFF, NYLON, 6.4mm	WURTH ELEKTRONIK, 702931000

SCHEMATIC DIAGRAM



ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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