



# PSMN7R5-60YL

N-channel 60 V, 7.5 mΩ logic level MOSFET in LFPAK56

20 November 2015

Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

## 2. Features and benefits

- Advanced TrenchMOS provides low  $R_{DS(on)}$  and low gate charge
- Logic level gate operation
- Avalanche rated, 100% tested
- LFPAK provides maximum power density in a Power SO8 package

## 3. Applications

- Synchronous rectifier in LLC topology
- Chargers & adaptors with  $V_{out} < 10$  V
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	60	V
$I_D$	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; <a href="#">Fig. 2</a>	-	-	86	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; <a href="#">Fig. 1</a>	-	-	147	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 20$ A; $T_j = 25$ °C; <a href="#">Fig. 11</a>	-	6	7.5	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10$ V; $I_D = 20$ A; $V_{DS} = 48$ V; $T_j = 25$ °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	60.6	-	nC
$Q_{GD}$	gate-drain charge	$V_{GS} = 5$ V; $I_D = 20$ A; $V_{DS} = 48$ V; $T_j = 25$ °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	9.7	-	nC

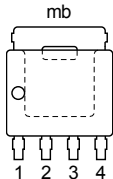
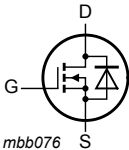
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 86\text{ A}$ ; $V_{sup} \leq 60\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped; <a href="#">Fig. 4</a>	[1][2]	-	-	76.5 mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Refer to application note AN10273 for further information.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LFAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN7R5-60YL	LFAK56; Power-SO8	Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads	SOT669

## 7. Limiting values

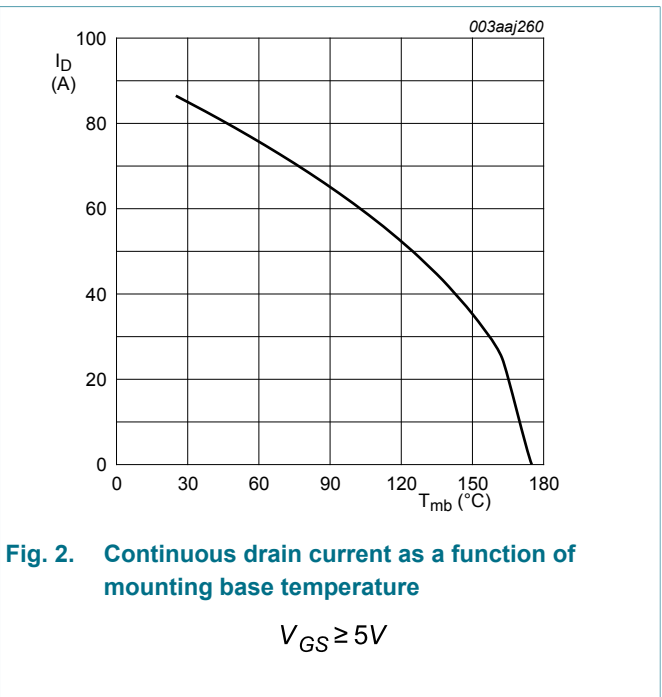
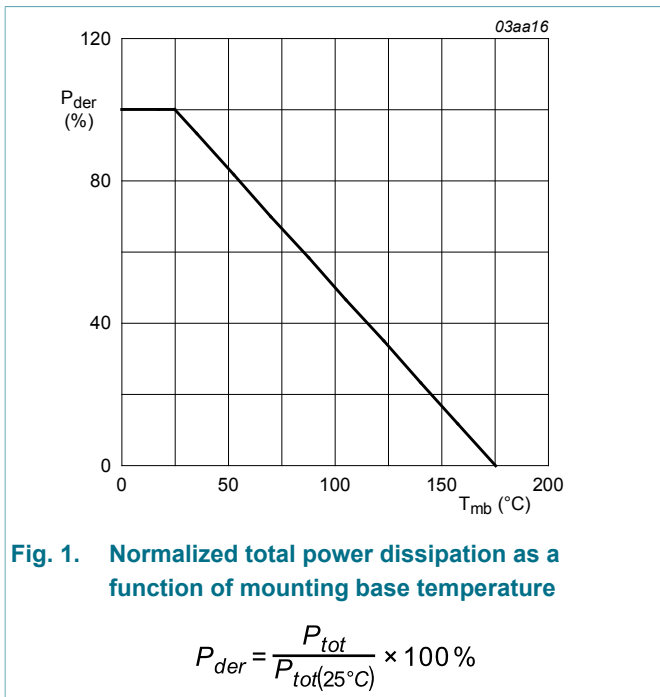
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	147	W
$I_D$	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 2</a>	-	86	A
		$T_{mb} = 100\text{ }^\circ\text{C}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 2</a>	-	61	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; pulsed; $t_p \leq 10\ \mu\text{s}$ ; <a href="#">Fig. 3</a>	-	346	A

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	86	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	346	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 86 A; V <sub>sup</sub> ≤ 60 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 4</a>	[1][2]	-	76.5 mJ

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.



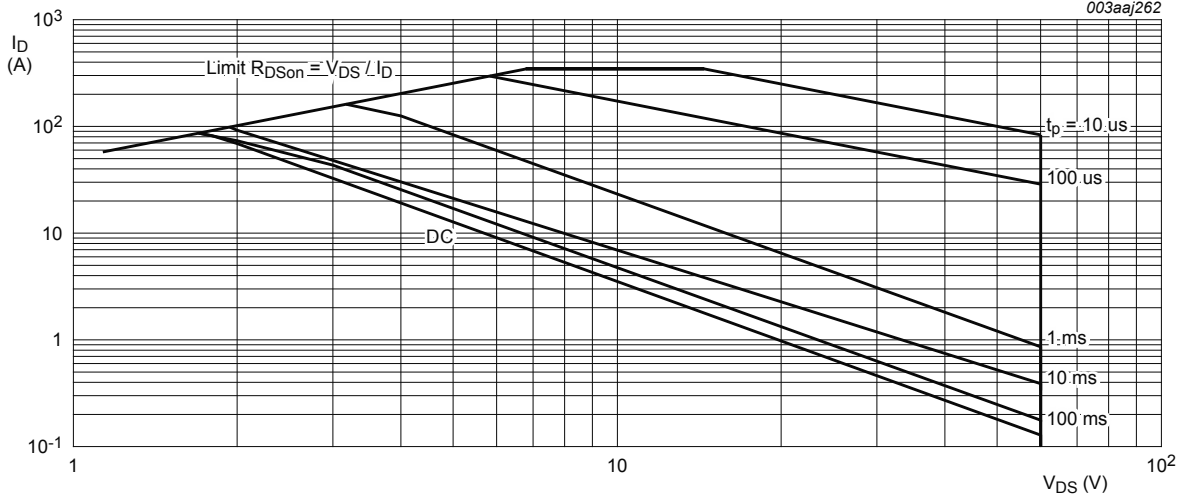


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is a single pulse

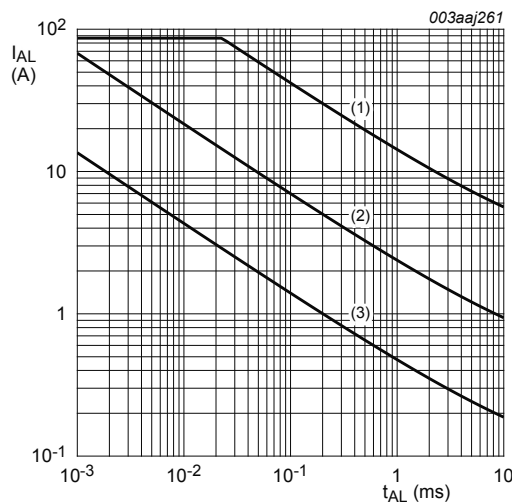


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_j(\text{init}) = 25^\circ\text{C}$ ; (2)  $T_j(\text{init}) = 150^\circ\text{C}$ ; (3) Repetitive Avalanche

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.02	K/W

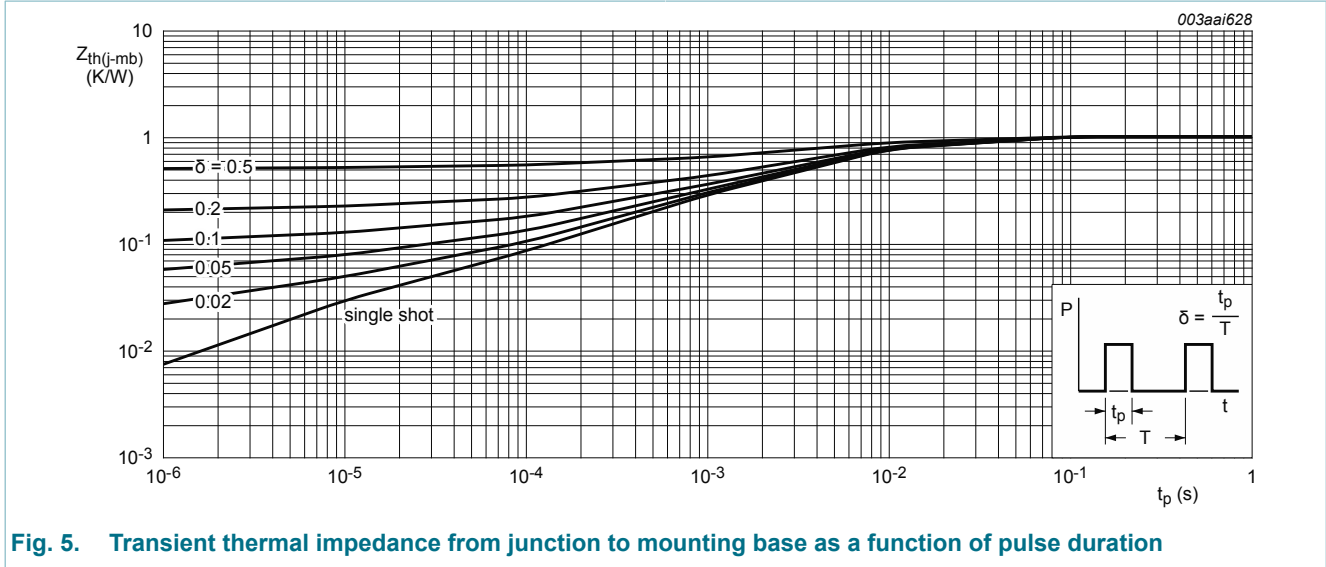


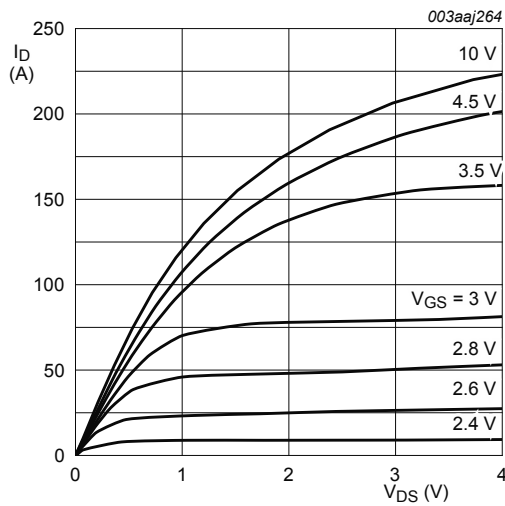
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 9. Characteristics

Table 6. Characteristics

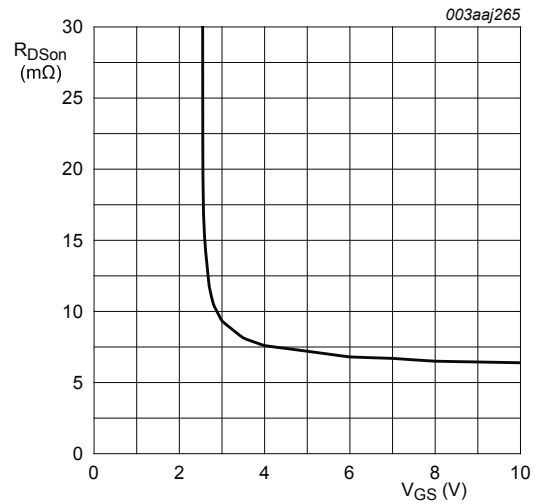
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.05	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 20 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	6.8	8.7	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	6	7.5	mΩ
		$V_{GS} = 5 V; I_D = 20 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 11</a>	-	-	19.7	mΩ
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 20 A; V_{DS} = 48 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 14</a>	-	31	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$I_D = 20\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	60.6	-	nC
$Q_{GS}$	gate-source charge	$I_D = 20\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 5\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	9	-	nC
$Q_{GD}$	gate-drain charge		-	9.7	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	3435	4570	pF
$C_{oss}$	output capacitance		-	295	355	pF
$C_{rss}$	reverse transfer capacitance		-	150	205	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 45\text{ V}; R_L = 2\text{ }^\Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}$	-	17	-	ns
$t_r$	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	42	-	ns
$t_f$	fall time		-	26	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 20\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.82	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	24	-	ns
$Q_r$	recovered charge		-	22.3	-	nC



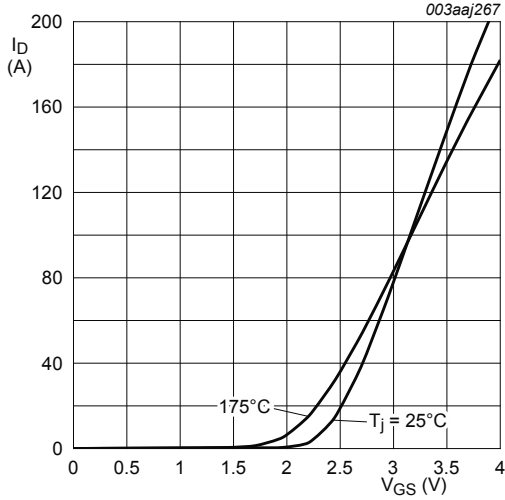
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



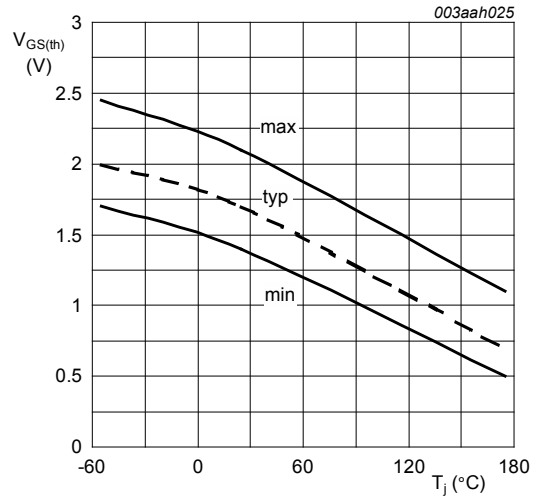
$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



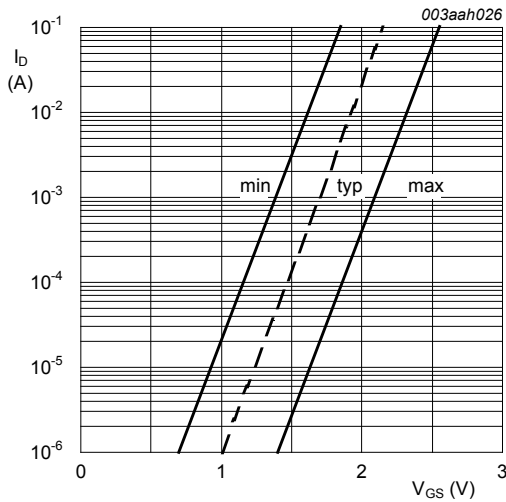
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$$V_{DS} = 10V$$



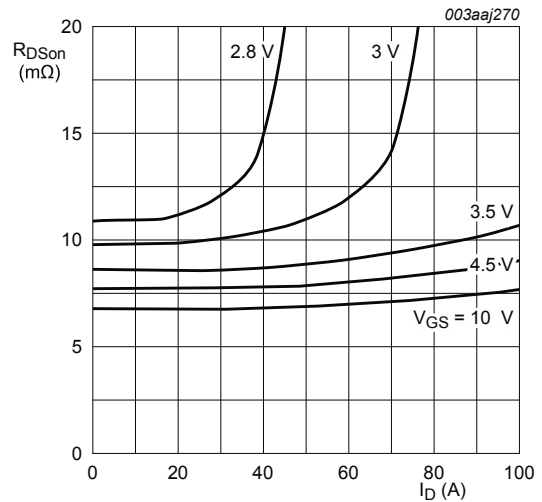
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



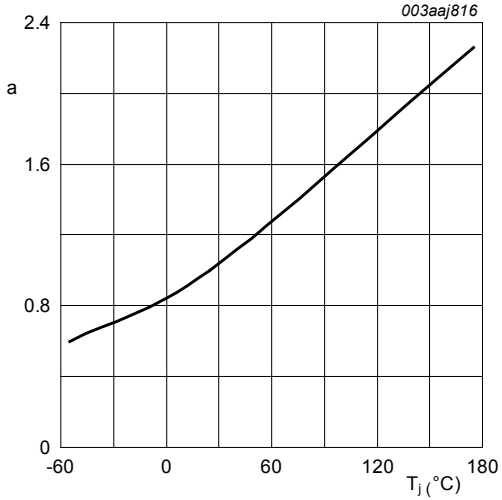
**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ\text{C}; V_{DS} = 5V$$



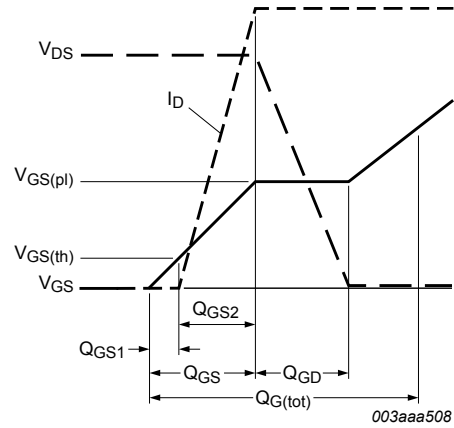
$$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

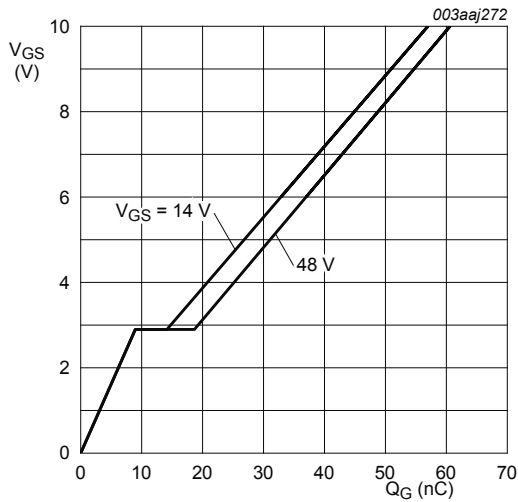


**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

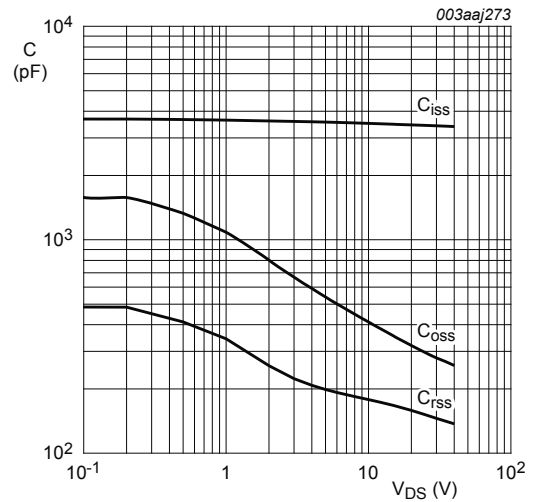


**Fig. 13. Gate charge waveform definitions**



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

$$T_j = 25^{\circ}\text{C}; I_D = 20\text{A}$$



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$



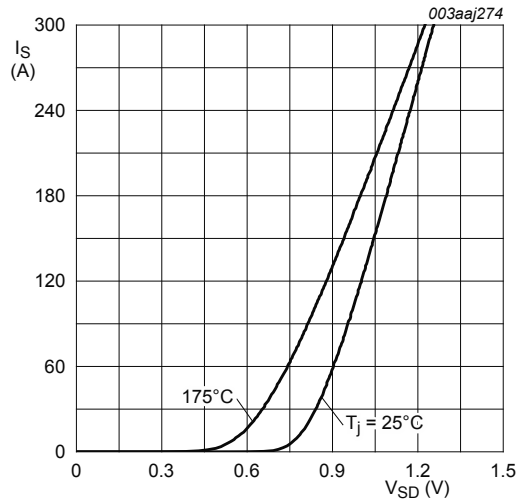
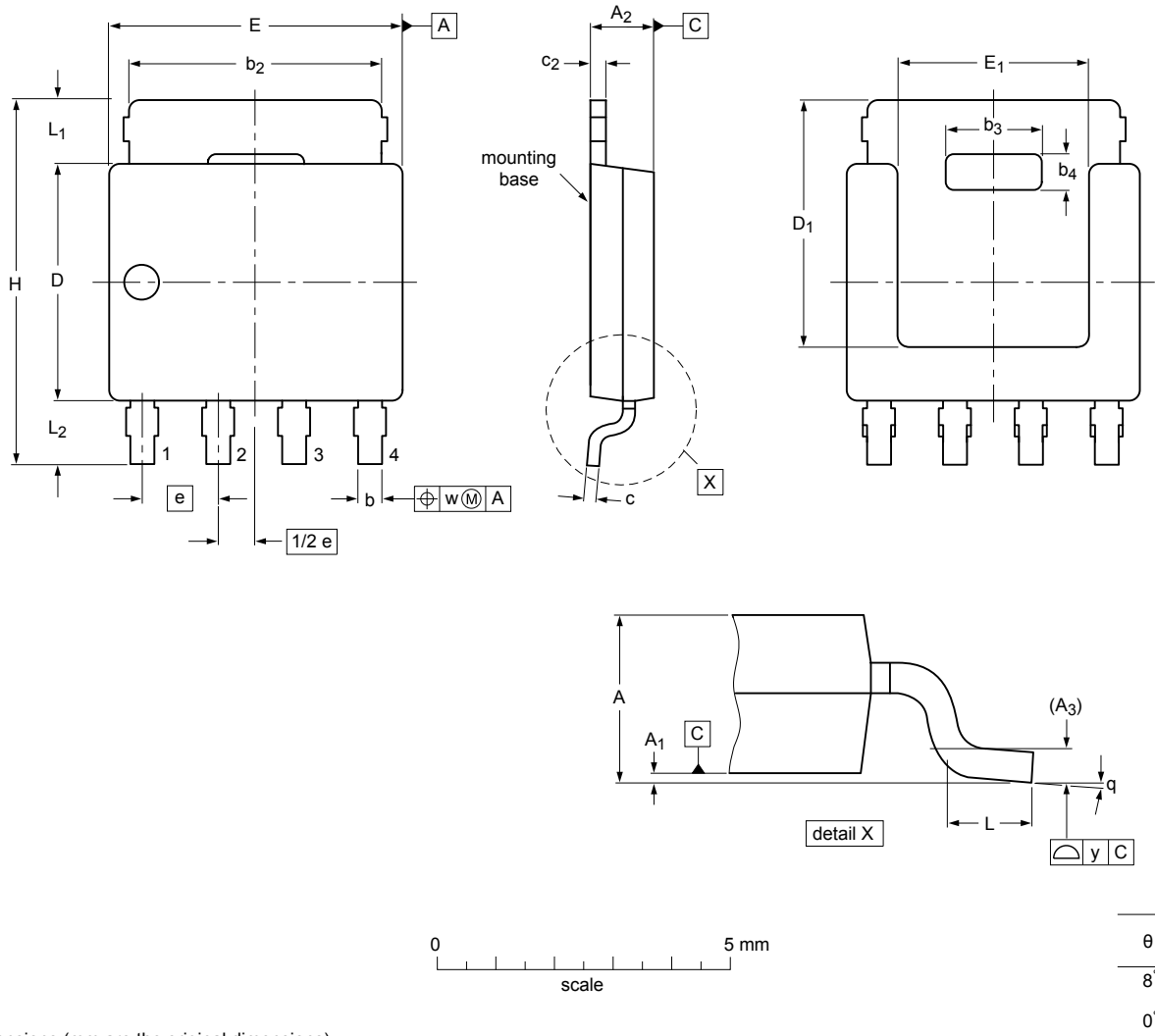


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

### 10. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit <sup>(1)</sup>	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 11. Legal information

### 11.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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