



MM54HCT240/MM74HCT240 Inverting Octal TRI-STATE® Buffer

MM54HCT241/MM74HCT241 Octal TRI-STATE Buffer

MM54HCT244/MM74HCT244 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT240/MM74HCT240 is an inverting buffer and the MM54HCT244/MM74HCT244 is a non-inverting

buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers. MM54HCT241/MM74HCT241 is also a non-inverting buffer similar to the 244 except that the 241 has one active high enable, each again controlling 4 buffers.

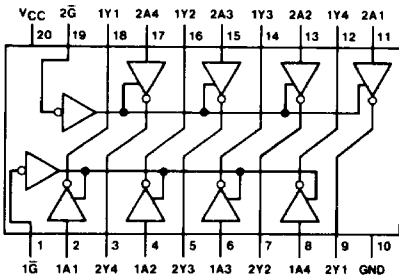
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- TTL input compatible
- Typical propagation delay: 14 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μ A
- High output drive current: 6 mA (min)

Connection Diagrams

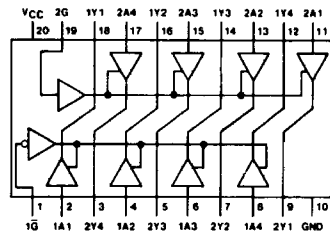
Dual-In-Line Packages



Top View

Order Number MM54HCT240* or MM74HCT240*

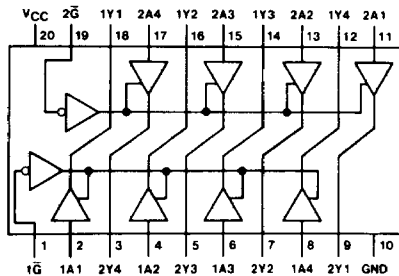
TL/F/5365-1



Top View

Order Number MM54HCT241* or MM74HCT241*

TL/F/5365-2



Top View

Order Number MM54HCT244* or MM74HCT244*

TL/F/5365-3

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to V _{CC} + 1.5V
DC Output Voltage (V _{OUT})	-0.5 to V _{CC} + 0.5V
Clamp Diode Current (I _{IK} , I _{OK})	± 20 mA
DC Output Current, per pin (I _{OUT})	± 35 mA
DC V _{CC} or GND Current, per pin (I _{CC})	± 70 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T _L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	4.5	5.5	V
DC Input or Output Voltage (V _{IN} , V _{OUT})	0	V _{CC}	V
Operating Temp. Range (T _A)			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times (t _r , t _f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ± 10% (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		74HCT	54HCT	Units
			Typ	Guaranteed Limits		T _A = -40 to 85°C	
V _{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V _{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum High Level Output Voltage	V _{IN-EE} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 6.0 mA, V _{CC} = 4.5V I _{OUT} = 7.2 mA, V _{CC} = 5.5V	V _{CC}	V _{CC} - 0.1	V _{CC} - 0.1	V _{CC} - 0.1	V
			4.2	3.98	3.84	3.7	V
			5.2	4.98	4.84	4.7	V
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 6.0 mA, V _{CC} = 4.5V I _{OUT} = 7.2 mA, V _{CC} = 5.5V	0	0.1	0.1	0.1	V
			0.2	0.26	0.33	0.4	V
			0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}		± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum TRI-STATE Output Leakage Current	V _{OUT} = V _{CC} or GND G̅ = V _{IH} G = V _{IL}		± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA		8.0	80	160	μA
		V _{IN} = 2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

Truth Tables

'HCT240

1G̅	1A	1Y	2G̅	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

'HCT241

1G̅	1A	1Y	2G̅	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

'HCT244

1G̅	1A	1Y	2G̅	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

AC Electrical Characteristics MM54HCT240/MM74HCT240, MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244 $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $T_A = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	14	18	ns
t_{PZL} , t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF $R_L = 1$ k Ω	20	30	ns
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF $R_L = 1$ k Ω	16	25	ns

AC Electrical Characteristics MM54HCT240/MM74HCT240, MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244 $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT	54HCT	Units	
			Typ	Guaranteed Limits				
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF	14	20	25	30	ns	
		$C_L = 150$ pF	20	28	35	42	ns	
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω	$C_L = 50$ pF	21	30	38	45	ns
			$C_L = 150$ pF	26	42	53	63	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω $C_L = 50$ pF	16	25	32	38	ns	
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	6	12	15	18	ns	
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF	
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF	
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\bar{G} = V_{CC}$, $G = GND$	5				pF	
		$\bar{G} = GND$, $G = V_{CC}$	90				pF	

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams

