# PM150CL1B060

**FLAT-BASE TYPE**
**INSULATED PACKAGE**

## PM150CL1B060

### FEATURE

Inverter + Drive & Protection IC

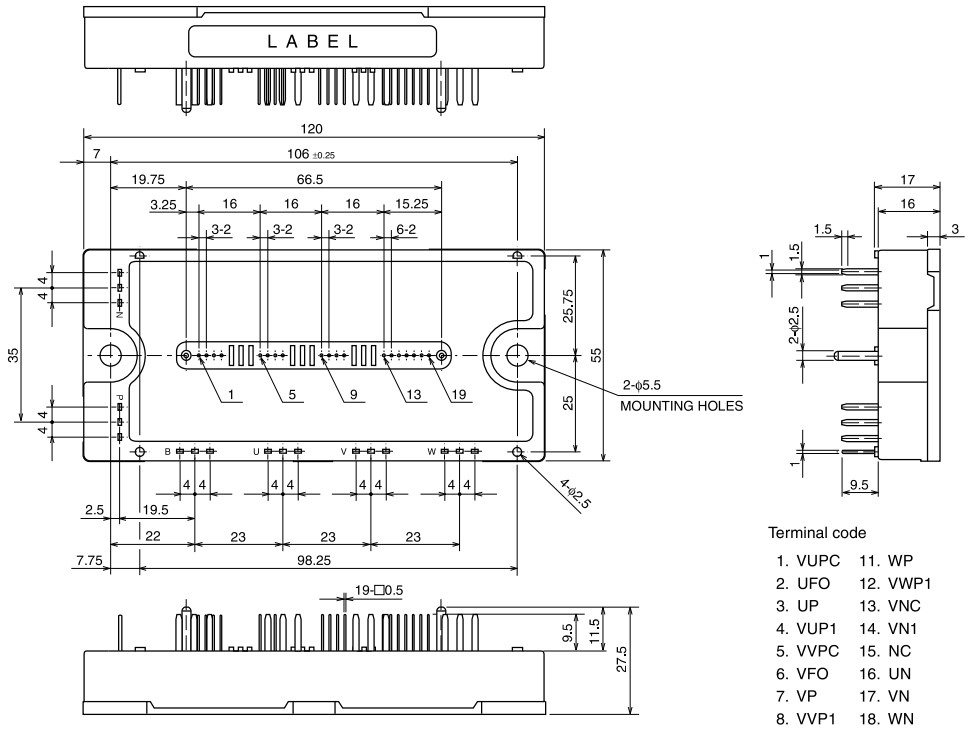
a) Adopting new 5th generation Full-Gate CSTBT$^{TM}$ chip
b) The over-temperature protection which detects the chip surface temperature of CSTBT$^{TM}$ is adopted.
c) Error output signal is possible from all each protection upper and lower arm of IPM.
d) Compatible L-series package.

- 3$\phi$ 150A, 600V Current-sense and temperature sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
- UL Recognized

## APPLICATION

General purpose inverter, servo drives and other motor controls

**PACKAGE OUTLINES** **Dimensions in mm**



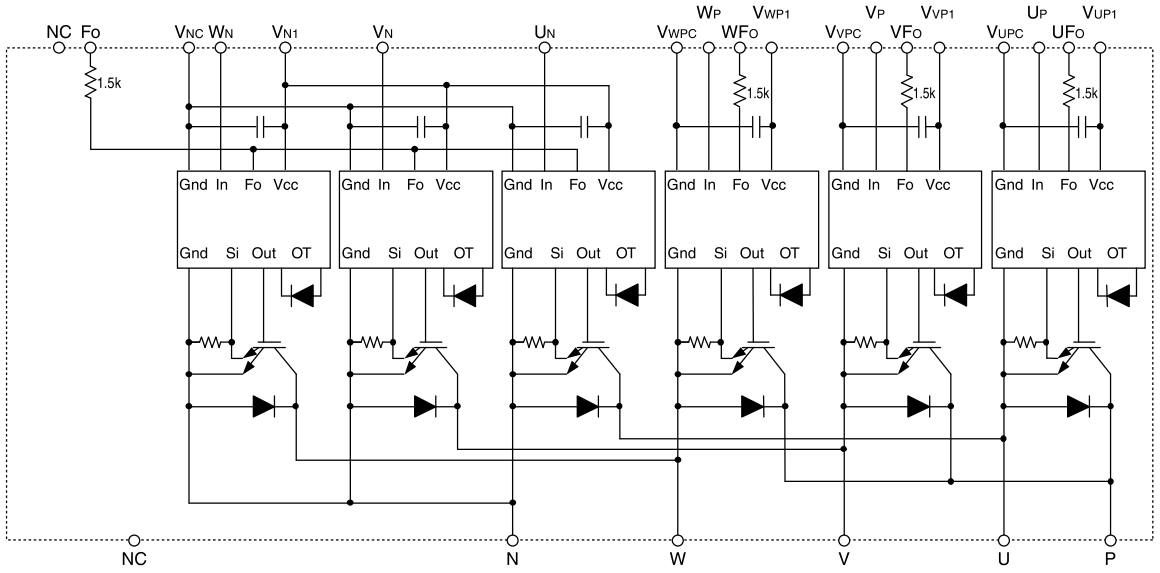

Terminal code

| | |
|---|---|
| 1. VUPC | 11. WP |
| 2. UFO | 12. VWP1 |
| 3. UP | 13. VNC |
| 4. VUP1 | 14. VN1 |
| 5. VVPC | 15. NC |
| 6. VFO | 16. UN |
| 7. VP | 17. VN |
| 8. VVP1 | 18. WN |
| 9. VWPC | 19. Fo |
| 10. WFO | |



MITSUBISHI ELECTRIC

## INTERNAL FUNCTIONS BLOCK DIAGRAM




**MAXIMUM RATINGS** ($T_j$ = 25°C, unless otherwise noted)

**INVERTER PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CES}$ | Collector-Emitter Voltage | $V_D$ = 15V, $V_{CIN}$ = 15V | 600 | V |
| ±$I_C$ | Collector Current | $T_C$ = 25°C (Note-1) | 150 | A |
| ±$I_{CP}$ | Collector Current (Peak) | $T_C$ = 25°C | 300 | A |
| $P_C$ | Collector Dissipation | $T_C$ = 25°C (Note-1) | 500 | W |
| $T_j$ | Junction Temperature | | –20 ~ +150 | °C |

*: Tc measurement point is just under the chip.

**CONTROL PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_D$ | Supply Voltage | Applied between : $V_{UP1}$-$V_{UPC}$, $V_{VP1}$-$V_{VPC}$ $V_{WP1}$-$V_{WPC}$, $V_{N1}$-$V_{NC}$ | 20 | V |
| $V_{CIN}$ | Input Voltage | Applied between : $U_P$-$V_{UPC}$, $V_P$-$V_{VPC}$, $W_P$-$V_{WPC}$ $U_N$ • $V_N$ • $W_N$-$V_{NC}$ | 20 | V |
| $V_{FO}$ | Fault Output Supply Voltage | Applied between : $U_{FO}$-$V_{UPC}$, $V_{FO}$-$V_{VPC}$, $W_{FO}$-$V_{WPC}$ $F_O$-$V_{NC}$ | 20 | V |
| $I_{FO}$ | Fault Output Current | Sink current at $U_{FO}$, $V_{FO}$, $W_{FO}$, $F_O$ terminals | 20 | mA |

## TOTAL SYSTEM

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC(PROT)}$ | Supply Voltage Protected by SC | $V_D$ = 13.5 ~ 16.5V<br>Inverter Part, $T_j$ = +125°C Start | 400 | V |
| $V_{CC(surge)}$ | Supply Voltage (Surge) | Applied between : P-N, Surge value | 500 | V |
| $T_{stg}$ | Storage Temperature | | –40 ~ +125 | °C |
| $V_{iso}$ | Isolation Voltage | 60Hz, Sinusoidal, Charged part to Base, AC 1 min. | 2500 | $V_{rms}$ |

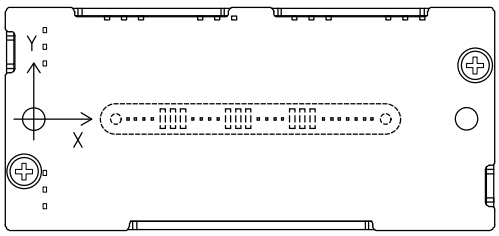
## THERMAL RESISTANCES

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $R_{th(j-c)Q}$ | Junction to case Thermal Resistances | Inverter IGBT part (per 1 element) (Note-1) | — | — | 0.25 | °C/W |
| $R_{th(j-c)F}$ | | Inverter FWDi part (per 1 element) (Note-1) | — | — | 0.41 | |
| $R_{th(c-f)}$ | Contact Thermal Resistance | Case to fin, (per 1 module)<br>Thermal grease applied (Note-1) | — | — | 0.038 | |

* If you use this value, $R_{th(f-a)}$ should be measured just under the chips.

(Note-1) Tc (under the chip) measurement point is below. (unit : mm)

| arm / axis | UP | | VP | | WP | | UN | | VN | | WN | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IGBT | FWDi | IGBT | FWDi | IGBT | FWDi | IGBT | FWDi | IGBT | FWDi | IGBT | FWDi |
| X | 27.8 | 27.8 | 65.5 | 65.5 | 87.5 | 87.5 | 38.8 | 38.8 | 54.5 | 54.5 | 76.5 | 76.5 |
| Y | –8.4 | 1.6 | –8.4 | –0.2 | –8.4 | –0.2 | 8.0 | –0.4 | 8.0 | –0.4 | 8.0 | –0.4 |




Bottom view

## ELECTRICAL CHARACTERISTICS ($T_j$ = 25°C, unless otherwise noted)

### INVERTER PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $V_D$ = 15V, $I_C$ = 150A<br>$V_{CIN}$ = 0V, Pulsed (Fig. 1) | $T_j$ = 25°C | — | 1.75 | 2.35 | V |
| | | | $T_j$ = 125°C | — | 1.75 | 2.35 | |
| $V_{EC}$ | FWDi Forward Voltage | –$I_C$ = 150A, $V_D$ = 15V, $V_{CIN}$ = 15V (Fig. 2) | | — | 1.7 | 2.8 | V |
| $t_{on}$ | Switching Time | $V_D$ = 15V, $V_{CIN}$ = 0V↔15V<br>$V_{CC}$ = 300V, $I_C$ = 150A<br>$T_j$ = 125°C<br>Inductive Load (Fig. 3,4) | | 0.3 | 0.8 | 2.0 | µs |
| $t_{rr}$ | | | | — | 0.4 | 0.8 | |
| $t_{c(on)}$ | | | | — | 0.4 | 1.0 | |
| $t_{off}$ | | | | — | 1.0 | 2.3 | |
| $t_{c(off)}$ | | | | — | 0.3 | 1.0 | |
| $I_{CES}$ | Collector-Emitter Cutoff Current | $V_{CE}$ = $V_{CES}$, $V_D$ = 15V (Fig. 5) | $T_j$ = 25°C | — | — | 1 | mA |
| | | | $T_j$ = 125°C | — | — | 10 | |

## CONTROL PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $I_D$ | Circuit Current | $V_D$ = 15V, $V_{CIN}$ = 15V | $V_{N1}$-$V_{NC}$ | — | 6 | 12 | mA |
| | | | $V^*_{P1}$-$V^*_{PC}$ | — | 2 | 4 | |
| $V_{th(ON)}$ | Input ON Threshold Voltage | Applied between : $U_P$-$V_{UPC}$, $V_P$-$V_{VPC}$, $W_P$-$V_{WPC}$ | | 1.2 | 1.5 | 1.8 | V |
| $V_{th(OFF)}$ | Input OFF Threshold Voltage | $U_N$ • $V_N$ • $W_N$-$V_{NC}$ | | 1.7 | 2.0 | 2.3 | |
| SC | Short Circuit Trip Level | −20 ≤ $T_j$ ≤ 125°C, $V_D$ = 15V (Fig. 3,6) | | 300 | — | — | A |
| $t_{off(SC)}$ | Short Circuit Current Delay Time | $V_D$ = 15V (Fig. 3,6) | | — | 0.2 | — | µs |
| OT | Over Temperature Protection | Detect Temperature of IGBT chip | Trip level | 135 | — | — | °C |
| $OT_{(hys)}$ | | | Hysteresis | — | 20 | — | |
| UV | Supply Circuit Under-Voltage Protection | −20 ≤ $T_j$ ≤ 125°C | Trip level | 11.5 | 12.0 | 12.5 | V |
| $UV_r$ | | | Reset level | — | 12.5 | — | |
| $I_{FO(H)}$ | Fault Output Current | $V_D$ = 15V, $V_{CIN}$ = 15V (Note-2) | | — | — | 0.01 | mA |
| $I_{FO(L)}$ | | | | — | 10 | 15 | |
| $t_{FO}$ | Minimum Fault Output Pulse Width | $V_D$ = 15V (Note-2) | | 1.0 | 1.8 | — | ms |

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

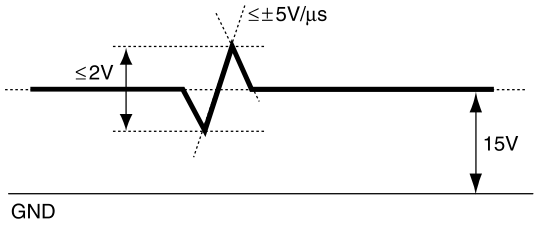
## MECHANICAL RATINGS AND CHARACTERISTICS

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| — | Mounting torque | Mounting part screw : M5 | 2.5 | 3.0 | 3.5 | N • m |
| — | Weight | — | — | 340 | — | g |

## RECOMMENDED CONDITIONS FOR USE

| Symbol | Parameter | Condition | Recommended value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Applied across P-N terminals | ≤ 400 | V |
| $V_D$ | Control Supply Voltage | Applied between : $V_{UP1}$-$V_{UPC}$, $V_{VP1}$-$V_{VPC}$ $V_{WP1}$-$V_{WPC}$, $V_{N1}$-$V_{NC}$ (Note-3) | 15.0 ± 1.5 | V |
| $V_{CIN(ON)}$ | Input ON Voltage | Applied between : $U_P$-$V_{UPC}$, $V_P$-$V_{VPC}$, $W_P$-$V_{WPC}$ | ≤ 0.8 | V |
| $V_{CIN(OFF)}$ | Input OFF Voltage | $U_N$ • $V_N$ • $W_N$-$V_{NC}$ | ≥ 9.0 | |
| $f_{PWM}$ | PWM Input Frequency | Using Application Circuit of Fig. 8 | ≤ 20 | kHz |
| $t_{dead}$ | Arm Shoot-through Blocking Time | For IPM's each input signals (Fig. 7) | ≥ 2.0 | µs |

(Note-3) With ripple satisfying the following conditions: dv/dt swing ≤ ±5V/µs, Variation ≤ 2V peak to peak



## PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage ($V_D$), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above $V_{CES}$ rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

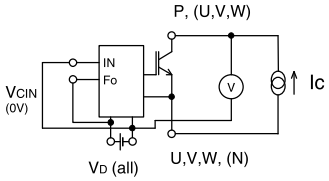



Fig. 1 $V_{CE(sat)}$ Test

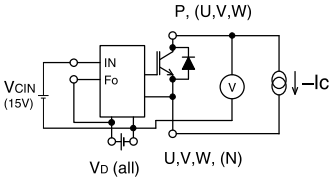



Fig. 2 $V_{EC}$, ($V_{FM}$) Test

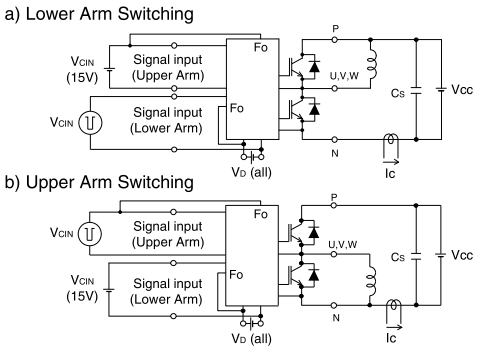



Fig. 3 Switching time and SC test circuit

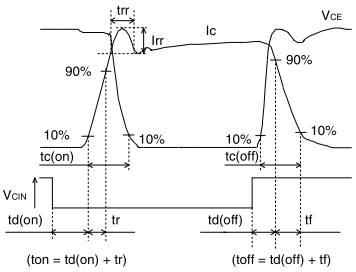



Fig. 4 Switching time test waveform

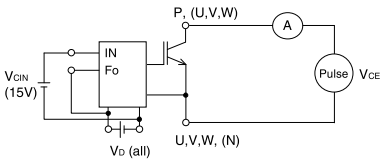



Fig. 5 $I_{CES}$ Test

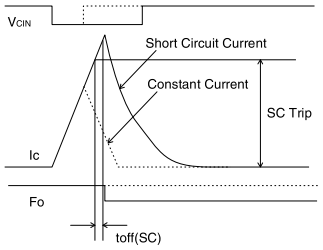
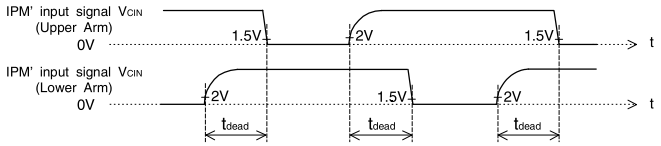



Fig. 6 SC test waveform




1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

Fig. 7 Dead time measurement point example

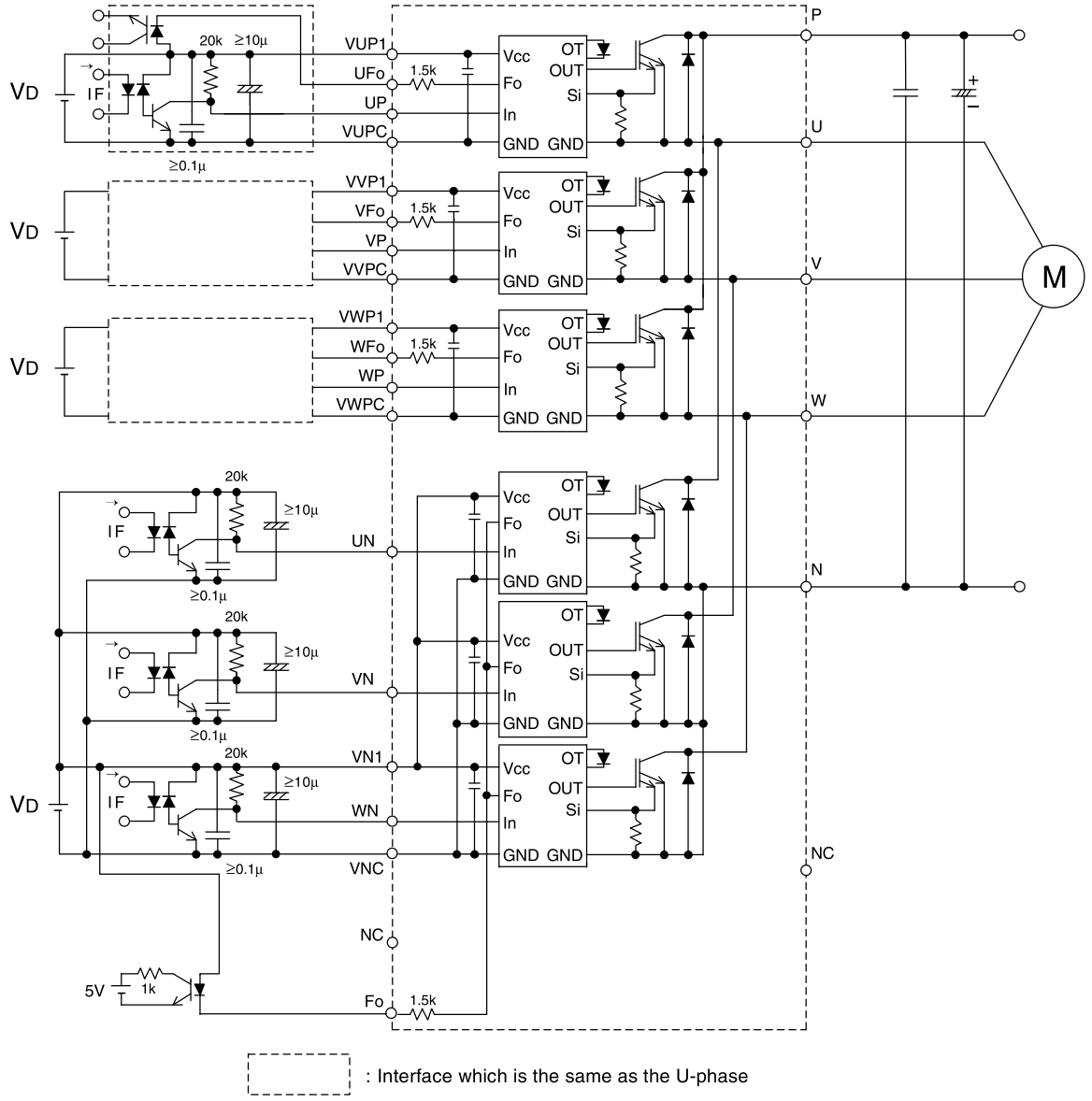


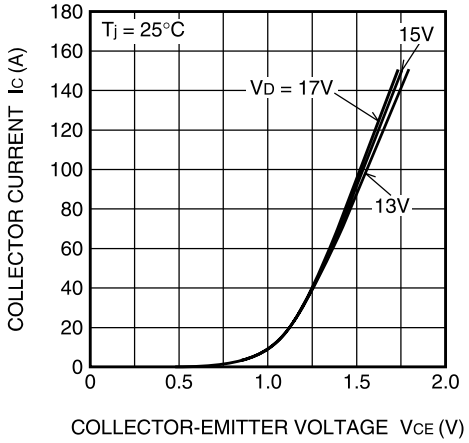

Fig. 8 Application Example Circuit

**NOTES FOR STABLE AND SAFE OPERATION ;**

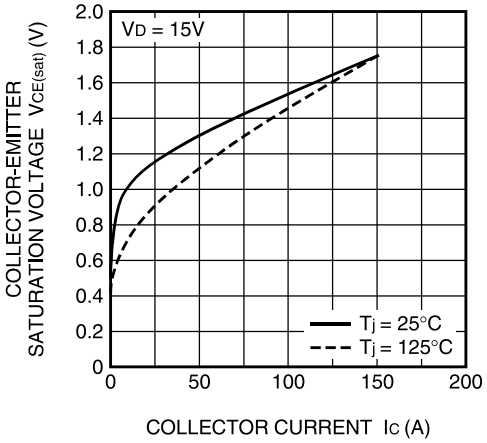
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}$, $t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies ($V_D$). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

## PERFORMANCE CURVES

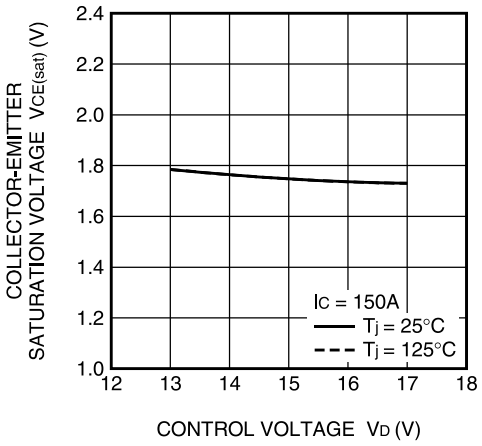
### OUTPUT CHARACTERISTICS (TYPICAL)



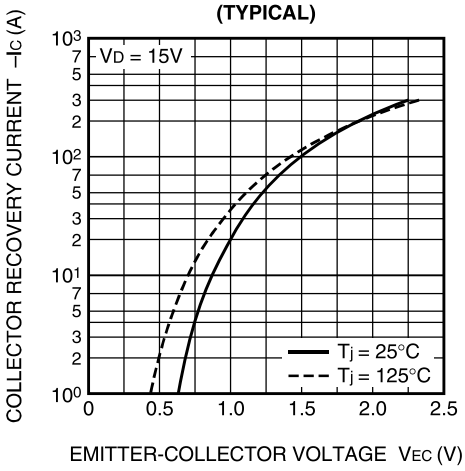

### COLLECTOR-EMITTER SATURATION VOLTAGE (VS. Ic) CHARACTERISTICS (TYPICAL)



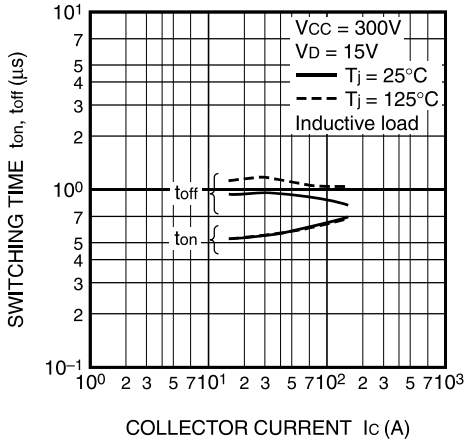

### COLLECTOR-EMITTER SATURATION VOLTAGE (VS. VD) CHARACTERISTICS (TYPICAL)



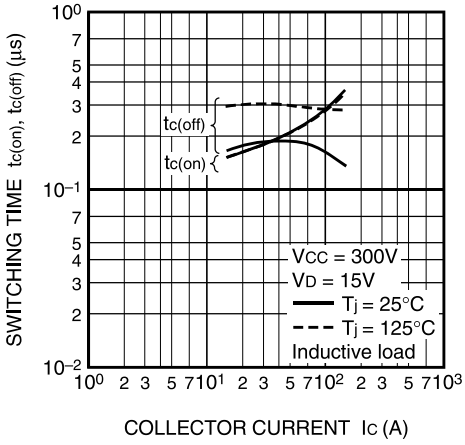

### DIODE FORWARD CHARACTERISTICS (TYPICAL)



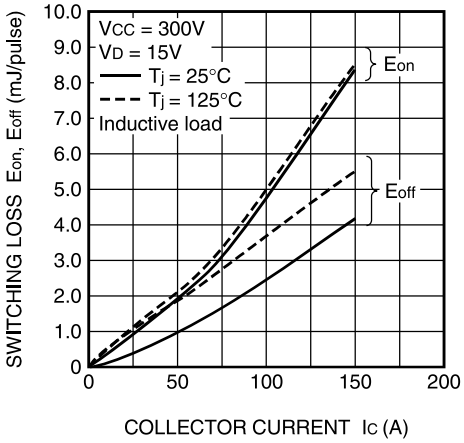

### SWITCHING TIME (ton, toff) CHARACTERISTICS (TYPICAL)



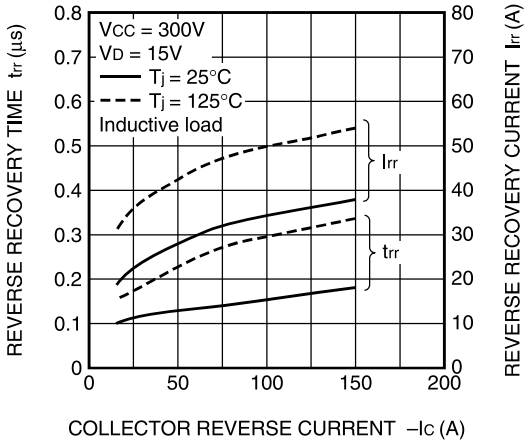

### SWITCHING TIME (tc(on), tc(off)) CHARACTERISTICS (TYPICAL)



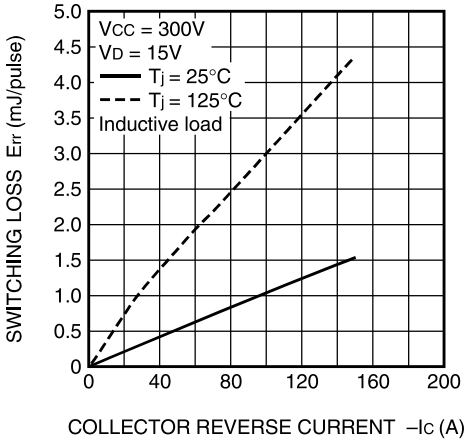
**SWITCHING LOSS CHARACTERISTICS (TYPICAL)**



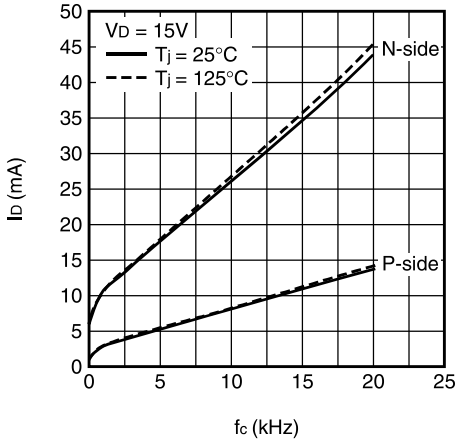

**DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)**



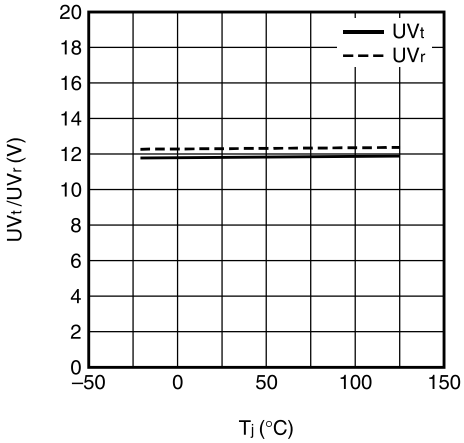

**SWITCHING RECOVERY LOSS CHARACTERISTICS (TYPICAL)**



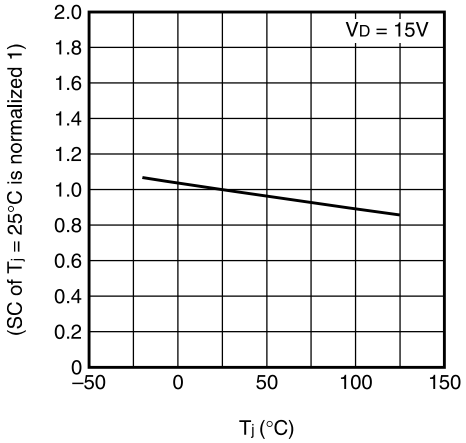

**ID VS. fc CHARACTERISTICS (TYPICAL)**



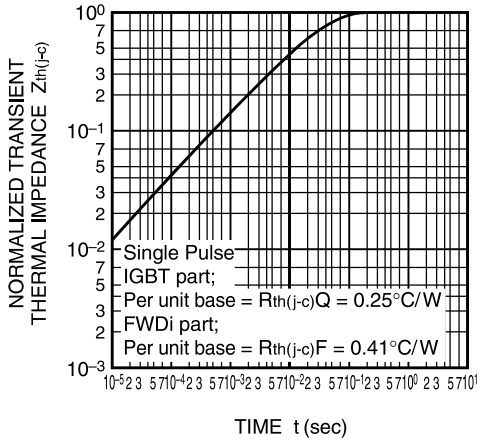

**UV TRIP LEVEL VS. Tj CHARACTERISTICS (TYPICAL)**




**SC TRIP LEVEL VS. Tj CHARACTERISTICS (TYPICAL)**



**TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (TYPICAL)**



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