ConnectCore™ 9P 9360 Hardware Reference

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Digi International, Inc.
11001 Bren Road East
Minnetonka, MN 55343 U.S.A.
United States: +1 877 912-3444
Other locations: +1 952 912-3444

www.digiembedded.com

Contents

Using this Guide

This guide provides information about the Digi ConnectCore 9P 9360 embedded core module.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

Digi information

Documentation updates

Please always chech the product specific section on the Digi support website for the most current revision of this document: www.digiembedded.com/support.

Contact information

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To contact Digi International by	Use
Mail	Digi International 11001 Bren Road East Minnetonka, MN 55343 U.S.A
World Wide Web	http://www.digiembedded.com/support/
email	http://www.digiembedded.com/support/
Telephone (U.S.)	(952) 912-3444 or (877) 912-3444
Telephone (other locations)	+1 (952) 912-3444 or (877) 912-3444

Change Log

1. Added change log.
2. Revised website address in contact information table.
3. Revised documentation updates section.
4. Removed specific OS reference from the Using This Guide chapter.
5. Corrected document title, footer, and all other mentions of the product name to read ConnectCore 9P 9360, rather than ConnectCore 9P.
6. Improved the module top view image within the Module Specifications section of Appendix A to make the pinout information clear.
7. Corrected typo of pin GPIO32 within the Multiplexed GPIO Pins table and typo of external interrupt EIRQ0 in the External Interrupts section.

About the Module

CHAPTER 1

The ConnectCore 9P 9360 is part of the ConnectCore embedded core processor module family. Built on leading NetSilicon® 32-bit NET+ARM technology, the network-enabled ConnectCore 9P family provides a modular and scalable core processor solution that significantly minimizes hardware and software design risk. This module combines superior performance and a complete set of integrated peripherals and component connectivity options in a compact and versatile form factor.

The ConnectCore 9P 9360 embedded module offers up to 128 MB RAM and 128 MB NAND flash, an integrated 10/100 Mb Ethernet MAC/PHY, up to four configurable UART/SPI ports, an online I^2C bus software interface, 73 shared GPIO ports for application-specific use, and an external 18-bit address/32-bit data bus interface for added component integration flexibility.

The ConnectCore 9P 9360 processor contains the NS9360 microprocessor. For information about the NS9360, see the *NS9360 Hardware Reference* available through your Jump Start kit.

Features and functionality

- 32-bit NET+ARM (ARM926EJ-S) RISC processor NS9750 @ 177MHz or 155MHz
- Up to 128 MB NAND Flash and 128 MB SD RAM
- 8 general purpose timers/counters or 4 PWM functions
- Up to 73 GPIO port options
- ARM9 core with memory management unit (MMU)

- Two 120-pin connectors
- Up to four RS232 serial interfaces with UART and SPI mode
- Integrated USB 2.0 compliant Host/Device interface
- Integrated 10/100Mbps Ethernet MAC/PHY
- I^2C interface, 100KHz and 400KHz
- On-board JTAG interface

Module variations

The ConnectCore 9P 9360 module is currently available in these standard variations:

- CPU speed 177MHz, 16MB SDRAM, 32MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 177MHz, 32MB SDRAM, 32MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 177MHz, 64MB SDRAM, 64MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 177MHz, 128MB SDRAM, 128MB NAND flash, 8KB SPI boot EEPROM, 8KB i^2C EEPROM, RTC, 0° C min / 70° C max
- CPU speed 155MHz, 32MB SDRAM, 32MB NAND flash, 8KB SPI boot EEPROM, 8KB I^2C EEPROM, RTC, -40° C min / 85° C max

Module pinout

The module has two 120 pole connectors, X1 and X2. The next tables describe each pin, its properties, and its use on the development board.

Pinout legend:

Type		
	I	Input
	O	Output
	I/O	Input or output
	P	Power

Pinout legend:

RESET state		
	PUW	Weak pullup to switched 3.3V in CPU on module
	PU10	Pull up 10K to switched 3.3V on module

Pinout legend: Other values

- dup: Some signals are multiplexed to two (or more) different GPIO pins, to maximize the number of possible applications. Duplicate signals are indicated by *(dup)* after the signal name. Using the primary pin and the duplicate pin for the same function is not recommended.
- SW: Indicates GPIO pins that have their external signal path switched off when RESET# is asserted. The format used is *GPIOSWnn*.
- #: Indicates that this signal is active low.

X1 Connector

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
1	GND	P									Common GND return
2	RSTIN#	I									PU10
3	PWRGOOD	I/O									
4	RSTOUT#	O									
5	TCK	I	JTAG								PU10
6	TMS	I	JTAG								PU10
7	TDI	I	JTAG								PU10
8	TDO	O	JTAG								PU10
9	TRST#	I	JTAG								PU10
10	CONF0 / DEBUGEN#	I									PU10 Debug enable 0 = Debug enabled, TRST# isolated from SRST#
11	CONF1 / NAND_ FWP#	I									PU10 NAND Flash write protect 0 = NAND Flash write protected
12	CONF2 / OCD_EN#	I									PU10 Enables OCD mode; use with CONF0 Pullup 10K to +3.3V on module
13	CONF3 / not used	I									Not connected
14	CONF4 GPIO38, 2K2 series	I/O	BIT28 GEN_ID								PU10
15	CONF5 GPIO39, 2K2 series	I/O	Bit29 GEN_ID								PU10
16	CONF6 GPIO40, 2K2 series	I/O	Bit30 GEN_ID								PU10

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
17	CONF7 GPIO41, 2K2 series	I/O	Bit31 GEN_ID								PU10
18	GPIOSW8	I/O		TXDA	SPIA_ DO						PU10
19	GPIO09	I/O		RXDA	SPIA_DI						PUW
20	GPIOSW10	I/O		RTSA#						PWM0 (dup)	PU10
21	GPIO11	I/O		CTSA#						EIRQ2 (dup) Timer 0 (dup)	PUW
22	GPIOSW12	I/O		DTRA#						PWM1 (dup)	PU10
23	GPIO13	I/O		DSRA#						EIRQ0 (dup) PWM2 (dup)	PU10
24	GPIOSW00	I/O		TXDB	SPIB_ DO		DMA0_ DONE (dup)			Timer1 (dup)	PU10
25	GPIO01	I/O		RXDB	SPIB_DI		DMA0_ REQ (dup)			EIRQ0	PUW
26	GPIOSW02	I/O		RTSB#			DMA1_ ACK			Timer0	PU10
27	GPIO03	I/O		CTSB#			DMA0_ REQ#		ACK#		PUW
28	GPIOSW04	I/O		DTRB#			DMA0_ DONE		BUSY		PU10
29	GPIO05	I/O		DSRB#			DMA0_ ACK		ERR		PUW
30	GPIO06	I/O		RIB#	SPIB_ CLK				P_JAM	Timer7 (dup)	PUW
31	GPIO07	I/O		DCDB#	SPIB_ EN#		DMA0_ ACK (dup)			EIRQ1	PUW
32	GPIO72	I/O	WAIT#								
33	GPIO68	I/O	A24 MCKE_0							EIRQ0 (dup)	
34	GPIO69	I/O	A25 MCKE_1							EIRQ1 (dup)	
35	No connect										Reserved for A26
36	No connect										Reserved for A27
37	GPIOSW24	I/O		DTRD#				LCDD0			PUW
38	GPIO25	I/O		DSRD#				LCDD1			PUW
39	GND	P									
40	GPIO26	I/O		RID#	SPID_ CLK			LCDD2		Timer3	PUW

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
41	GPIO27	I/O		DCDD#	SPID_ EN#			LCDD3		Timer4	PUW
42	GPIO28	I/O						LCDD4 LCCD8 (dup)		EIRQ1 (dup)	PUW
43	GPIO29	I/O						LCDD5 LCCD9 (dup)		Timer5	PUW
44	GPIO30	I/O						LCDD6 LCDD10 (dup)		Timer6	PUW
45	GPIO31	I/O						LCDD7 LCDD11 (dup)			PUW
46	GPIO32	I/O						LCDD8	D0	EIRQ2	PUW
47	GPIO33	I/O						LCDD9	D1		PUW
48	GPIO34	I/O				SCL		LCDD10	D2		PUW
49	GPIO35	I/O				SDA		LCDD11	D3		PUW
50	GPIOSW36	I/O						LCDD12	D4	PWM0	PU10
51	GPIOSW37	I/O						LCDD13	D5	PWM1	PU10
52	GPIOSW38	I/O						LCDD14	D6	PWM2	PU10
53	GPIOSW39	I/O						LCDD15	D7	PWM3	PU10
54	GPIOSW40	I/O		TXDC	SPIC_ DO			LCDD16		EIRQ3	PU10
55	GPIOSW41	I/O		RXDC	SPIC_DI			LCDD17			PU10
56	GPIO42	I/O	USB_ EXTPHY_ D+	RTSC#							PUW
57	GPIO43	I/O	USB_ EXTPHY_ D-	CTSC#					DIRCON		PUW
58	GPIOSW44	I/O	USB_ EXTPHY_ OE#	TXDD	SPID_ DO				SELECT		PU10
59	GPIO45	I/O	USB_ EXTPHY_ RCV	RXDD	SPID_DI				STB		PUW
60	GPIO46	I/O	USB_ EXTPHY_ RXD+	RTSD#					ALFD		PUW
61	GPIO47	O	USB_ EXTPHY_ RXD-	CTSD#					INIT#		PUW
62	GPIO18	I/O	Ethernet ECAM_REJ					LCD_ PWREN#		EIRQ3 (dup)	PUW
63	GPIO22	I/O		RIC#	SPIC_ CLK			LCD_AE_ BDE			PUW
64	GPIO21	I/O		DSRC#				LCD_ VSYNC			PUW

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
65	GPIOSW19	I/O	Ethernet ECAM_ REQ				DMA1_ ACK#	LCD_ HSYNC			PU10
66	GPIOSW20	I/O		DTRC#				LCD_CLK			PU10
67	GPIO23	I/O		DCDC#	SPIC_ EN#			LCD_LEN D			PUW
68	A0	O									External address
69	A1	O									External address
70	A2	O									External address
71	A3	O									External address
72	A4	O									External address
73	A5	O									External address
74	A6	O									External address
75	A7	O									External address
76	A8	O									External address
77	A9	O									External address
78	A10	O									External address
79	GND	P									
80	A11	O									External address
81	A12	O									External address
82	A13	O									External address
83	A14	O									External address
84	A15	O									External address
85	A16	O									External address
86	A17	O									External address
87	A18	O									External address
88	A19	O									External address
89	A20	O									External address
90	A21	O									External address
91	GPIO66	O	A22								Set to external address
92	EXT_OE#	O									
93	EXT_WE#	O									
94	GPIO67	O	A23								Set to external address
95	CS0#	O	Chip select								
96	CS2#	O	Chip select								
97	CS3#	O	Chip select								
98	No connect	n/a									
99	PWREN	O									

Pin	Signal	Type	BootStrap (BS) / System / Other	UART	SPI	I2C	DMA	LCD	IEEE 1284	PWM / Timer / IRQ	Notes Reset state
100	No connect	n/a									Reserved as BATT_FLT#
101	GPIO48	I/O	USB_ EXTPHY_ SUSP				DMA1_ REQ		P_SEL	Timer14	PUW
102	GPIO16	I	USB_OVC						P_JAM (dup)		PUW
103	EXT_BE0#	O									External byte lane enable
104	EXT_BE1#	O									External byte lane enable
105	EXT_BE2#	O									External byte lane enable
106	EXT_BE3#	O									External byte lane enable
107	GPIO15	I		DCDA#	SPIA_ EN#			LCD_CLKI N		Timer2	PUW
108	No connect	n/a									
109	No connect	n/a									
110	GPIO14	I		RIA#	SPIA_ CLK					PWM3 (dup) Timer1	
111	GPIO70	O	A26 MCKE_2			SCL					
112	GPIO71	I/O	A27 MCKE_3			SDA					
113	GPIOSW17	I/O	USB_PWR								PU10
114	USB_ INTPHY_P	I/O									USB Host / Device
115	USB_ INTPHY_N	I/O									USB Host / Device
116	VRTC	P									3V RTC battery can be connected here
117	GND	P									
118	3.3V_IN	P									Unswitched 3.3V
119	VLIO	P									**Mobile:** Power from Li-Ion battery **Non-mobile:** Connected to unswitched 3.3V
120	3.3V_IN	P									Unswitched 3.3V

X2 Connector

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
1		No connect	PCI_INTA#			
2	P	GND				
3		No connect	PCI_INTC#			
4		No connect	PCI_INTB#			
5		No connect	PCI_RESET#			
6		No connect	PCI_INTD#			
7		No connect	PCI_GNT0#			
8		GND				
9		No connect	PCI_GNT1#			
10		No connect	PCI_CLKOUT			
11		No connect	PCI_CLKIN			
12		No connect	PCI_GNT2#			
13		No connect	PCI_GNT3#			
14	P	GND				
15		No connect	PCI_AD30			
16		No connect	PCI_REQ0#			
17		No connect	PCI_REQ1#			
18		No connect	PCI_REQ2#			
19		No connect	PCI_REQ3#			
20		No connect	PCI_AD31			
21		No connect	PCI_AD28			
22		No connect	PCI_AD29			
23		No connect	PCI_AD26			
24		No connect	PCI_AD27			
25		No connect	PCI_AD24			
26		No connect	PCI_AD25			
27		No connect	PCI_IDSEL			
28		No connect	PCI_CBE3#			
29		No connect	PCI_AD22			
30		No connect	PCI_ADD23			
31		No connect	PCI_AD20			
32		No connect	PCI_AD21			
33		No connect	PCI_AD18			

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
34		No connect	PCI_AD19			
35		No connect	PCI_AD16			
36		No connect	PCI_AD17			
37		No connect	PCI_FRAME#			
38		No connect	PCI_CBE2#			
39		No connect	PCI_TRDY#			
40	P	GND				
41		No connect	PCI_IRDY#			
42		No connect	PCI_STOP#			
43		No connect	PCI_PAR			
44		No connect	PCI_DEVSEL#			
45		No connect	PCI_AD15			
46		No connect	PCI_PERR#			
47		No connect	PCI_AD13			
48		No connect	PCI_SERR#			
49		No connect	PCI_AD11			
50		No connect	PCI_CBE1#			
51		No connect	PCI_AD9			
52		No connect	PCI_AD14			
53		No connect	PCI_CBE0#			
54		No connect	PCI_AD12			
55		No connect	PCI_AD6			
56		No connect	PCI_AD10			
57		No connect	PCI_AD4			
58		No connect	PCI_AD8			
59		No connect	PCI_AD2			
60		No connect	PCI_AD7			
61		No connect	PCI_AD5			
62		No connect	PCI_AD3			
63		No connect	PCI_AD1			
64		No connect	PCI_AD0			
65		No connect			LCD_CLKIN	
66	I			ETH_TPIN		

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
67	O			ETH_LEDLNK		
68	I			ETH_TPIP		
69	O			ETH_LEDH		
70	O			ETH_TPON		
71	I			ETH_ESD0		
72	O			ETH_TPOP		
73		No connect				Reserved for ETH_EREF
74		No connect				
75		No connect				
76		No connect				
77		No connect				
78		No connect				
79		No connect				
80	P	GND				
81	I/O	D0				Data bus
82	I./O	D1				Data bus
83	I/O	D2				Data bus
84	I/O	D3				Data bus
85	I/O	D4				Data bus
86	I/O	D5				Data bus
87	I/O	D6				Data bus
88	I/O	D7				Data bus
89	I/O	D8				Data bus
90	I/O	D9				Data bus
91	I/O	D10				Data bus
92	I/O	D11				Data bus
93	I/O	D12				Data bus
94	I/O	D13				Data bus
95	I/O	D14				Data bus
96	I/O	D15				Data bus
97	I/O	D16				Data bus
98	I/O	D17				Data bus
99	I/O	D18				Data bus

Pin	Type	Signal	PCI	Ethernet	LCD	Notes
100	I/O	D19				Data bus
101	I/O	D20				Data bus
102	I/O	D21				Data bus
103	I/O	D22				Data bus
104	I/O	D23				Data bus
105	I/O	D24				Data bus
106	I/O	D25				Data bus
107	I/O	D26				Data bus
108	I/O	D27				Data bus
109	I/O	D28				Data bus
110	I/O	D29				Data bus
111	I/O	D30				Data bus
112	I/O	D31				Data bus
113		No connect				Reserved for A28
114		No connect				Reserved for A29
115		No connect				Reserved for A30
116		No connect				Reserved for A31
117		No connect				Reserved
118		No connect				Reserved
119	O	CLKOUT				
120	P	GND				

Configuration pins — CPU

Several pins allow configuration of the CPU before booting. CPU pins have weak pullups (value range is 15-300K) for a default configuration. Most pins do not have configuration options and some are connected for internal configuration on the module. Thirty-two of the 73 GPIO pins allow user-specific configurations, which are latched in the GEN_ID register (address 0xA090 0210) five clock cycles after the rising edge of RESET#. Certain pins are protected; that is, they are not accessible externally until strapping information that is configured on the module is latched.

Important

Normally, you will never need to change the hardware module CPU configuration. Configuring the module incorrectly can prevent the module from booting.

Default module CPU configuration

- Little endian mode selected
- PLL active (PLL bypass not allowed)
- PLL_FS divider set to 2
- PLL_ND multiplier set to 24 (177 MHz), 21 (154 MHz), or 14 (103 MHz)
- Boot from SPI EEPROM (spi.bin)

Configuration pins — Module

Module configuration pins change hardware configuration on the module (HCONF0-3) or are user-specific and are read in the GEN_ID register (SCONF0-3).

Module pin configuration

Bold entries indicate default values.

Signal name	Function	PU/PD	External pin name	Comment
DEBUG_EN#	CPU mode select 0 Disconnects TRST# and PWRFOOD for JTAG and boundary scan debug mode **1 TRST# and PWRGOOD connected for normal mode**	PU 10K	HCONF0	
FWP#	Internal NAND flash write protect 0 Write protect active 1 No write protect	PU 10K	HCONF1	
OCD_EN#	JTAG / Boundary scan function select 0 ARM debug mode, BISTEN# set to high **1 Boundary scan mode, BISTEN# set to low**	PU 10K	HCONF2	Select JTAG mode; DEBUG_EN# has to be low, too
	Not used		HCONF3	No function, no connect
GPIO38	User-defined software configuration pin; can be read in GEN_ID register bit 28, default high		SCONF0	Read bit 28, GEN_ID
GPIO39	User-defined software configuration pin; can be read in GEN_ID register bit 29, default high		SCONF1	Read bit 29, GEN_ID

Signal name	Function	PU/PD	External pin name	Comment
GPIO40	User-defined software configuration pin; can be read in GEN_ID register bit 30, default high		SCONF2	Read bit 30, GEN_ID
GPIO41	User-defined software configuration pin; can be read in GEN_ID register bit 31, default high		SCONF3	Read bit 31, GEN_ID

Recommended combinations of DEBUG_EN# and OCD_EN#

HCONF0	HCONF2	Mode
OFF	OFF	Normal mode
ON	OFF	Debug mode
OFF	ON	Not recommended
ON	ON	OCD mode

Clock generation

Clock frequencies

This table summarizes the clock frequencies for the 177 MHz module.

Crystal:	29.4912 MHz
PLL	
PLL_ND(4:0), PLL multiplier:	b10010, d24, CPU PLL active
PLL_FS(1:0), PLL divider:	b11, d2, CPU PLL active
PLL_IS(1:0), value:	b11, ND16-31, CPU PLL active
Resulting PLL clock:	353.8944 MHz
CPU clock:	176.9472 MHz
AHB, SDRAM, and external clock:	88.4736 MHz
BCLK clock:	44.2368 MHz
UART baud rate clock BBus:	44.2368 MHz
LCD clock:	88.4736 MHz, 44.2368 MHz, 22.1184 MHz, or 11.0592 MHz

Changing the CPU speed

To change the CPU speed, write in these fields in the PLL Configuration register:

- PLL ND SW (NDSW)
- PLL frequency select (FSEL)

- PLL SW change (PLLSW)

Important: When PLL parameters are changed, hardware reset duration is 4 ms for the PLL to stabilize. Applications using this feature need to discriminate between cold start and warm start.

Boot process

The ConnectCore 9P 9360 module is preconfigured to boot with SPI channel B from a serial EEPROM. The serial EEPROM contains memory controller setup for SDRAM bank 0, as well as an initial boot program that moves the boot loading program from NAND flash to SDRAM bank 0 and starts it. The size of the serial SPI EEPROM is 8KB.

Chip selects

The module has eight chip selects: four for dynamic memory and for static memory. Each chip select has a 256MB range.

Chip select memory map

Name	Pin	Address range	Size [Mb]	Use	Comments
SDM_CS0#	B4	0x00000000–0x0FFFFFFF	256	SDRAM bank 0	First bank on module
SDM_CS1#	A3	0x10000000–0x1FFFFFFF	256	SDRAM bank 1	Second bank on module
SDM_CS2#	D5	0x20000000–0x2FFFFFFF	256	No connect	
SDM_CS3#	C4	0x30000000–0x3FFFFFFF	256	No connect	
EXT_CS0#	B3	0x40000000–0x4FFFFFFF	256	External, CS0#	
EXT_CS1#	C1	0x50000000–0x5FFFFFFFF	256	NAND-Flash	Program memory
EXT_CS2#	D2	0x60000000–0x6FFFFFFFF	256	External, CS2#	
EXT_CS3#	E3	0x70000000–0x7FFFFFFF	256	External, CS3#	
Reserved		0x80000000–0x8FFFFFFF	256		
BBus		0x90000000–0x9FFFFFFF	256	BBus memory	
Reserved		0xA0000000–0xA03FFFFF	4		
Bridge		0xA0400000–0xA04FFFFF	1	Bridge	
Reserved		0xA0500000–0xA05FFFFF	1	Reserved	
Ethernet		0xA0600000–0xA06FFFFF	1	Ethernet module	
Memory		0xA0700000–0xA07FFFFF	1	Memory controller	

Name	Pin	Address range	Size [Mb]	Use	Comments
LCD		0xA0800000–0xA08FFFFF	1	LCD controller	
System		0xA0900000–0xA09FFFFF	1	System control module	
Reserved		0xA0A00000–0xFFFFFFFF	1	Reserved	

NAND flash

Access the NAND flash with EXT_CS1#. The FWP# signal write-protects the chip externally.

Onboard flash

The module has 32Mx8, 64Mx8, or 128Mx8 NAND flash onboard. Greater sizes can optionally be populated, if available. The interface to the NAND flash requires 32kB due to use of A13 and A14 for address and command control.

SDRAM banks

The module provides two SDRAM banks, connected to CS4# (D_CS0#) and CS5# (D_CS1#). CS6# (D_CS2#) nd CS7# (D_CS3#) are lost. The module does not provide external SDRAM connection.

The module has one of these SDRAM onboard: 1X4MX32, 2X4MX32, or 4X4M32. A12 is the highest address connected, and the chip select range is 256M.

BA0 and BA1 are connected to A13 and A14, respectively. The SDRAM controller connects the appropriate address line to allow a gapless memory space at different SDRAM sizes.

Using the second SDRAM bank

The module's SPI loader initializes only SDRAM bank 0 with SD_CS0. The second bank cannot be initialized when the system is running from SDRAM because it uses the same registers as the running (first) bank but for different parameters. The Dynamic Memory Control register, in particular, must use set mode command rather than normal mode command while starting the second bank. The initialization routine needs to be run from either NOR flash (if you are booting with flash) or from another memory location.

For example, you can run the initialization routine from the Ethernet TX buffer descriptor RAM, starting at address 0xA0601000 with a space of 256 * 32 bit words. Before using this RAM, however, bit 23 in the Ethernet General Control Register 1 must be set to high to enable the RAM.

Multiplexed GPIO pins

The 73 GPIO pins on the module are multiplexed with these other functions:

- UART and SPI
- USB
- Ethernet
- DMA
- Parallel port IEEE1284
- I^2C (IIC) port
- LCD port
- Timers and interrupt inputs
- Memory bus address and control pins

If a pin is used as GPIO, it "gives up" another function.

Pin notes

- GPIO0 – GPIO48 and GPIO66 – GPIO72 are accessible on the connectors.
- GPIO13 is used for RTC interrupt on the module (allows sharing with open drain ORing).
- GPIO 49 – GPIO65 are used on the module and are not accessible externally.
- All GPIOs are set to GPIO input function after RESET. Use in another function requires configuring the GPIO registers at powerup.

GPIO multiplex table

Some signals are multiplexed to two different GPIO pins, to maximize the number of possible applications. These duplicate signals are marked as *(dup)* in the table. Selecting the primary GPIO pin and the duplicate GPIO pin for the same function is not recommended. If both the primary GPIO pin and duplicate GPIO pin are programmed for the same function, however, the primary GPIO pin has precedence and will be used.

Port name, Function 03 (default at powerup)	Alternate function 00, UART	Alternate function 00, miscellaneous	Alternate function 01	Alternate function 02	On module, default used as
GPIO0	TXDB	SPI_Boot_DO SPIB_DO	DMA0 DONE (dup)	Timer 1 (dup)	TXDB, SPI_Boot_DO, or external SPIB_DO
GPIO1	RXDB	SPI_Boot_DI SPIB_DI	DMA0 REQ (dup)	EIRQ0	RXDB, SPI_Boot_DI, or external SPIB_DI
GPIO2	RTSB#		Timer 0	DMA1 ACK	RTSB#, DMA
GPIO3	CTSB#		1284 ACK#	DMA0 REQ	CTSB#, DMA

Port name, Function 03 (default at powerup)	Alternate function 00, UART	Alternate function 00, miscellaneous	Alternate function 01	Alternate function 02	On module, default used as
GPIO4	DTRB#		1284 BUSY	DMA0 DONE	DTRB#
GPIO5	DSRB#		1284 ERR	DMA0 ACK	DSRB#, DMA
GPIO6	RIB#	SPI_Boot_CLK SPIB_CLK External RXCLK_A	1284 P_JAM	Timer 7 (dup)	RIB#, SPI_Boot_CLK, or external SPIB_CLK
GPIO7	DCDB#	SPI Boot CE# SPIB_CE# External TXCLK_A	DMA0 Ack (dup)	EIRQ1	DCDB#, SPI_Boot_CE#, or external SPIB_CE#
GPIO8	TXDA	SPIA_DO	Reserved	Reserved	TXDA, SPI A
GPIO9	RXDA	SPIA_DI	Reserved	Reserved	RXDB, SPI A
GPIO10	RTSA#		Reserved	PWM0 (dup)	GPIO10
GPIO11	CTSA#		EIRQ2 (dup)	Timer 0 (dup)	GPIO11
GPIO12	DTRA#		Reserved	PWM1 (dup)	GPIO12
GPIO13	DSRA#		EIRQ0 (dup)	PWM2 (dup)	EIRQ0 connected to RTC_INT# on module
GPIO14	RIA#	SPIA_CLK External RXCLK_B	Timer 1	PWM3 (dup)	SPI A
GPIO15	DCDA#	SPIA_EN# External TXCLK B	TImer 2	LCD_CLKIN	SPI A
GPIO16		USB overcurrent	1284 P_JAM (dup)	Reserved	USB_OVCUR
GPIO17		USB power relay	Reserved	Reserved	USB_PREL
GPIO18		Ethernet CAM reject	LCD PWREN	EIRQ3 (dup)	LCD
GPIO19		Ethernet CAM request	LCD HSYNC	DMA1 ACK (dup)	LCD
GPIO20	DTRC#		LCD CLK	Reserved	LCD
GPIO21	DSRC#		LCD VFSYNC	Reserved	LCD
GPIO22	RIC#	SPIC_CLK External RXCLK_C	LCD_BIAS_D_EN	Reserved	LCD
GPIO23	DCDC#	SPIC_EN External TXCLK_C	LCD LINE_END	Reserved	LCD
GPIO24	DTRD#		LCDD0	Reserved	LCD
GPIO25	DSRD#		LCDD1	Reserved	LCD
GPIO26	RID#	SPID_CLK External RXCLK_D	LCDD2	Timer 3	LCD

Port name, Function 03 (default at powerup)	Alternate function 00, UART	Alternate function 00, miscellaneous	Alternate function 01	Alternate function 02	On module, default used as
GPIO27	DCDD#	SPID_EN External TXCLK_D	LCDD3	Timer 4	LCD
GPIO28		EIRQ1 (dup)	LCDD4	LCDD8 (dup)	LCD
GPIO29		Timer 5	LCDD5	LCDD9 (dup)	LCD
GPIO30		Timer 6	LCDD6	LCDD10 (dup)	LCD
GPIO31		Timer 7	LCDD7	LCDD11 (dup)	LCD
GPIO32		EIRQ2	1284 D1	LCDD8	LCD
GPIO33		Reserved	1284 D2	LCDD9	LCD
GPIO34		IIC_SCL	1284 D3	LCDD10	LCD
GPIO35		IIC_SDA	1284 D4	LCDD11	LCD
GPIO36		PWM0	1284 D5	LCDD12	LCD
GPIO37		PWM1	1284 D6	LCDD13	LCD
GPIO38		PWM2	1284 D7	LCDD14	LCD
GPIO39		PWM3	1284 D8	LCDD15	LCD
GPIO40	TXDC	SPIC_DO	IRQ3	LCDD16	LCD
GPIO41	RXDC	SPIC_DI	Reserved	LCDD17	LCD
GPIO42	RTSC#		Reserved	USB_PHY_D+	USB_EXTPHY_D+
GPIO43	CTSC#		1284 DORCON	USB_PHY_D-	USB_EXTPHY_D-
GPIO44	TXDD	SPID_DO	1284 SELECT	USB_PHY_TXOUT_EN	USB_EXTPHY_OE#
GPIO45	RXDD	SPID_DI	1284 STRB	USB_PHY_RXD	USB_EXTPHY_RXD
GPIO46	RTSD#		1284 ALFD	USB_PHY_RXD+	GPIO46
GPIO47	CTSD#		1284 INIT	USB_PHY_RXD-	GPIO47 drives DEBUG-LED
GPIO48		USB_PHY_SUSP	1284 P_SEL	DMA1 REQ	USB_EXTPHY_SUSP
GPIO49		USB_PHY_SPEED	1284 P_LOG	DMA1 DONE	R/B# NAND-Flash (GPIO) control on module
GPIO50		MII_MDIO	Reserved	USB_PHY_D+ (dup)	MII_MDIO
GPIO51		MII_RXDV	Reserved	USB_PHY_D- (dup)	MII_RXDV
GPIO52		MII_RXER	Reserved	USB_PHY_TXOUT_EN	MII_RXER
GPIO53		MII_RXD0	Reserved	USB_PHY_RXD (dup)	MII_RXD0
GPIO54		MII_RXD1	Reserved	USB_PHY_SUSP (dup)	MII_RXD1

Port name, Function 03 (default at powerup)	Alternate function 00, UART	Alternate function 00, miscellaneous	Alternate function 01	Alternate function 02	On module, default used as
GPIO55		MII_RXD2	Reserved	USB_PHY_SPEED (dup)	MII_RXD2
GPIO56		MII_RXD3	Reserved	USB_PHY_RXD+ (dup)	MII_RXD3
GPIO57		MII_TXEN	Reserved	USB_PHY_RXD- (dup)	MII_TXEN
GPIO58		MII_TXER	Reserved	Reserved	MII_TXER
GPIO59		MII_TXD0	Reserved	Reserved	MII_TXD0
GPIO60		MII_TXD1	Reserved	Reserved	MII_TXD1
GPIO61		MII_TXD2	Reserved	Reserved	MII_TXD2
GPIO62		MII_TXD3	Reserved	Reserved	MII_TXD3
GPIO63		MII_COL	Reserved	Reserved	MII_COL
GPIO64		MII_CRS	Reserved	Reserved	MII_CRS
GPIO65		MII_PHY_INT	Reserved	Reserved	MII_MDINT#
GPIO66		A22	Reserved	Reserved	A22
GPIO67		A23	Reserved	Reserved	A23
GPIO68		A24	MCKE_0	IRQ0 (dup)	A24
GPIO69		A25	MCKE_1	IRQ1 (dup)	A25
GPIO70		A26	MCKE_2	IIC_SCL (dup)	IIC_SCL
GPIO71		A27	MCKE_3	IIC_SDA (dup)	IIC_SDA
GPIO72		TA_STB	Reserved	Reserved	ext WAIT

External interrupts

Four external interrupts are multiplexed with other functions on the GPIO pins. Every interrupt is multiplexed to two or three different GPIO pins. These duplicate signals are marked as *(dup)* in the table.

External interrupt	1st position	Other functions, 1st position	2nd position (duplicate	Other functions, 2nd position
EIRQ0	GPIO1	RXDB, SPIBoot_DI and SPIB_DI, DMA0_REQ (dup)	GPIO13	DSRA#, PWM2 (dup), used on module for RTC interrupt
EIRQ1	GPIO7	DCDB#, SPIBoot_CE# and SPIB_CE#, DMA0_ACK (dup)	GPIO28	LCD_D4, LCD_D8 (dup)

External interrupt	1st position	Other functions, 1st position	2nd position (duplicate	Other functions, 2nd position
EIRQ2	GPIO32	LCDD8, 1284 D0	GPIO11	CTSA#, Timer 0 (dup)
EIRQ3	GPIO40	TXDC, SPIC_DO, LCDD16	GPIO18	LCD_EN, ETH_CAMREJ

EIRQ0 and EIRQ1 have a third position on the module:

- EIRQ0 (dup): GPIO68 and A24
- EIRQ1 (dup): GPIO69 and A25

Both address lines are routed to the module connectors. If the address lines are not used on the base board or application, access the interrupts by changing the GPIO configuration.

Interfaces

10/100 Mbps Ethernet port

The 10/100 Mbps Ethernet port allows a glueless connection of a 3.3V MII or RMII PHY chip that generates the physical Ethernet signals.

The module has a MII PHY chip LXT971 / LXT972 (depending on temperature) in a LQFP-64 case on board. The module does not have a transformer or Ethernet connector; the base board must provide these parts.

A PHY clock of 25 MHz is generated in the PHY chip with a 25 MHz crystal.

USB 2.0 full and low speed Host and Device controller

The module's USB section provides USB signals for a Host and Device channel. All external configuration for a USB host interface, USB Device interface, or both must be made on the base board.

The internal USB PHY can be used for the USB Host or Device channel (USB_INTPHY_DP, USB_INTPHY_DN). These signals are not 5V tolerant and must be protected on the base board. A second, independent USB Device channel is provided when an external unidirectional or bidirectional PHY is connected to USB Device control signals GPIO42–GPIO45 and GPIO48. In this case, the internal PHY must be used in Host mode.

UART

The module provides up to four UART ports with all handshake signals, used in asynchronous mode:

- Port A = GPIO8 through GPIO15
- Port B = GPIO0 through GPIO7

- Port C = GPIO20 through GPIO23
- Port D = GPIO24 through GPIO27

The module supports baud rates up to 1.8 MHz in asynchronous mode.

SPI

The module provides four SPI ports, which can be used in either master or slave mode. SPI port B (GPIO0, GPIO1, GPIO6, and GPIO7) is connected to the serial 8Kx8 SPI EEPROM that contains the boot program and the initial SDRAM parameters for booting through SPI when RESET# is asserted. Additional hardware allows external use of this port after boot at runtime.

The other SPI ports can be used free in these circumstances:

- If they are not used in UART, USB, or LCD mode
- If they are not blocked by other GPIO use

Serial: UART and SPI use on module

The module has two serial ports, A and B, wired with at least TXD, RXD, RTS#, and CTS# as common port lines.

- If LCD functionality is used, only UART ports A and B and/or SPI function are allowed.
- If all signals for the module's LCD function are used, UART port C and/or SPI function are blocked.
- USB use with external PHY requires GPIOs that provide SPI channel D.

I^2C bus

The I^2C bus (signals IIC_SCL and IIC_SDA) is connected on the module to a serial EEPROM with the I^2C interface on device address 0xA0, 0xA1. Device address 0xD0, 0xD1 connects to an RTC on board. All other addresses can be used externally.

The maximum clock frequency in slow mode is 50 KHz and in fast mode is 200 KHz.

Important: Use only 3.3V devices.

LCD controller (STN and TFT)

The module provides an LCD interface for STN or TFT, with up to 18 data lines (LCDD0 through LCDD17 (GPIO24 through GPIO41)) and 6 control lines (GPIO18 through GPIO23). LCD use disables serial ports C and D and most GPIOs.

This interface allows connection of most TFT and STN monochrome and color LCDs. For more information, see the *NS9360 Hardware Reference* (available in your Jump Start kit).

Serial EEPROM

The module supports nonvolatile storage of parameters such as MAC address with a serial 8Kx8 EEPROM (reference part number 24LC64 or similar with TSSOP8). The serial EEPORM is connected to the I^2C bus at device address 0xA0, 0xA1. Write protect

WP and optional address lines A0, A1, and A2 can be grounded (sometimes these pins are not connected).

RTC

The module provides an RTC (reference part number MAXIM/ DALLAS DS1337 with µSPO8) connected to the I^2C bus at device address 0xD0, 0xD1. The RTC has its own 32.768 KHz clock crystal. Power is taken from +3.3V when provided; otherwise, power is taken from V_{BAT} fed by an external battery. An interrupt line (GPIO13 configured as IRQ1) is connected to the RTC pin AINT# (open drain, default disabled). Depopulate resistor R2 to open the connection.

JTAG, boundary scan

The module supports JTAG and boundary scan with the TCK, TMS, TDI, TDO, and TRST# signals. The RTCK signal is not connected externally.

Use the external signal DEBUG_EN# (HCONF0) to select either normal mode or debug mode. Use the signal OCD_EN# to select either ARM debug mode or boundary scan mode. THis table shows signal and mode use:

DEBUG_EN#	OCD_EN#	Mode	Comments
1	1	Normal	
1	0	Not recommended	**Be aware:** Boundary scan is possible but TRST# is connected with SRST# and the system might hang.
0	1	ARM debug	
0	0	Boundary scan	

Baudrate calculation

The baud rate generators have four different clock sources:

- X1_SYS_OSC/ M
- BCLK
- External receive clock
- External transmit clock

X1_SYS_OSC/M

X1_SYS_OSC/ M is the frequency of the input crystal divided by *M*. The value of M depends on the PLL_ND multiplier setting:

- M = 2 at PLL_ND >= 8 decimal (14.7456 MHz with 29.4912 MHz quartz).
- M = not usable for PLL_ND < 8 (baud clock unstable and or wrong frequency at CPU speeds < 58.9824 MHz).

This clock cannot be used if PLL is bypassed.

BCLK

With 176.9472 MHz, BCLK = AHBCLK/2 = 44.2368 MHz.

This is an internal source when the PLL is bypassed.

External receive clock

The clock source is an external receive clock from pins GPIO6, GPIO14, GPIO22, and GPIO26.

External transmit clock

The clock source is an external transmit clock from pins GPIO7, GPIO15, GPIO23, and GPIO27.

Count values vs baud rate clock

The module uses PLL. Modules with 177 MHz, 155 MHz, and 103 MHz use the values from the first column, which allow baud rates from 75 to 921600Bd.

Baud rate	N, X1_SYS/2 = 14.745600MHz, (Error) [%]	N, BCLK = 44.236800 MHz, (Error) [%]	N, BCLK = 38.707200 MHz, (Error) [%]	N, BCLK = 25.804800 MHz, (Error) [%]
75	12287, (-)	-----	32255, (-)	21503, (-)
150	6143, (-)	18431, (-)	15127, (-)	10751, (-)
300	3071, (-)	9215, (-)	8063, (-)	5375, (-)
600	1535, (-)	4607, (-)	4031, (-)	2687, (-)
1200	767, (-)	2303, (-)	2015, (-)	1343, (-)
2400	383, (-)	1151, (-)	1007, (-)	671, (-)
4800	191, (-)	575, (-)	503, (-)	335, (-)
7200	127, (-)	383, (-)	335, (-)	223, (-)
9600	95, (-)	287, (-)	251, (-)	167, (-)
14400	63, (-)	191, (-)	167, (-)	111, (-)
19200	47, (-)	143, (-)	125, (-)	83, (-)
28800	31, (-)	95, (-)	83, (-)	55, (-)
38400	23, (-)	71, (-)	62, (-)	41, (-)
57600	15, (-)	47, (-)	41, (-)	27, (-)
115200	7, (-)	23, (-)	20, (-)	13, (-)
230400	3, (-)	11, (-)		6, (-)
460800	1, (-)	5, (-)		
921600	0, (-)	2, (-)		
1843200	-----	-----		

Power

Power supply

The module has +3.3V_IN and VLIO supply pins.

Internal voltage

A switching regulator from VLIO converts 1.5V core voltage with up to 400mA to keep losses small.

Powerup/power down behavior

Hardware ensures the recommended powerup and power down behavior (see the *NS9360 Hardware Reference* in your Jump Start kit).

Power sequencing: Important

Every base board has to switch its 3.3V supply according to the module. Otherwise, power sequencing ion the module is influenced by backfeeding the module with 3.3V from the base board. Use the PWREN signal to switch the power supply.

Bootloader (UBOOT)

Every module has a bootloader (UBOOT) pre-installed in NAND flash:

- The bootloader boots the operating system from NAND flash using a serial port or Ethernet.
- The bootloader can pass parameters to the kernel.

Extended module

For use with other modules in the ARM9 family, additional hardware might be required with more signal lines connected between the module and the base board. Digi provides an extended module for this purpose, with two additional 60-pin (each) board-to-board connectors.

About the Development Board

CHAPTER 2

The ConnectCore 9P 9360 development board supports the ConnectCore 9P 9360 module. This chapter describes the components of the development board and explains how to configure the board for your requirements.

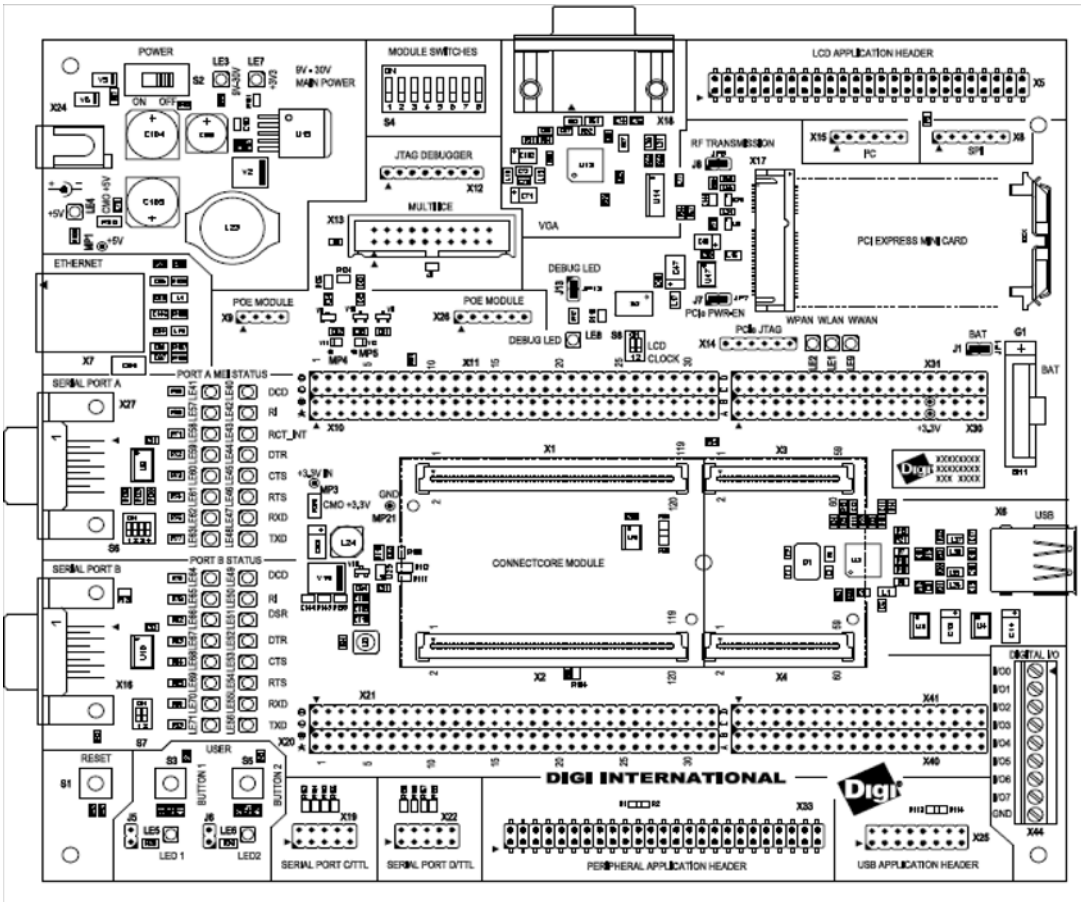
The development board has two 4x32 pin connectors that are 1:1 copies of the module pins. Connectors for an extended module and their signal rails are available should you need them.

What's on the development board?

- Current measurement option on +3.3V and +5V power supplies
- +3.3V, +5V, and GND test points
- +9 / +30 VDC input power supply
- PoE connectors for PoE application board
- Two user LEDs
- Two user keys
- One debug LED
- USB Host port
- PCIe socket
- SPI header
- I^2C digital I/O expansion (8-bit) with 9-pin (standard) header
- Ethernet connector
- 3.3V battery
- VGA interface connector
- Four serial connectors:

  - A: UART MEI (RS232/ RS4xx)
  - B: UART RS232
  - C: UART TTL
  - D: UART TTL
- Eight dip switches: four for hardware configuration and four for software configuration
- Two 2x25 pin connectors for functional expansion:
  - LCD application kit header
  - Peripheral application header

The development board

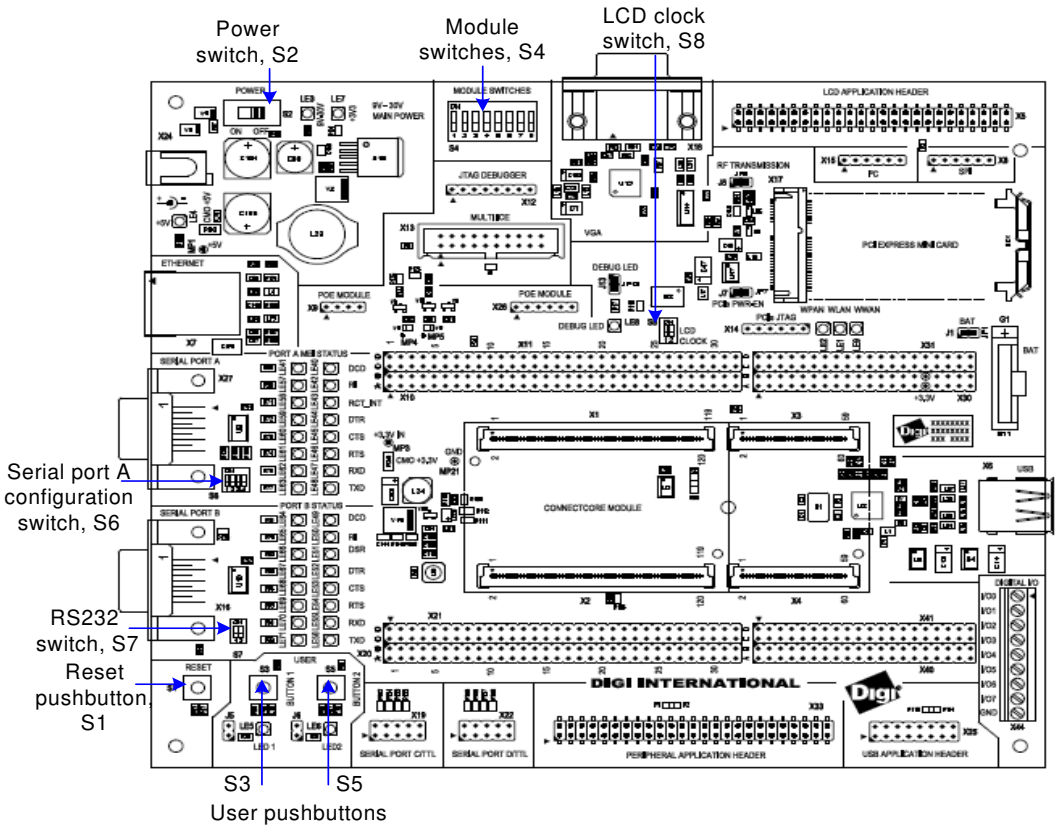


User interface

The development board provides a user interface through software-controlled LEDs, pushbuttons, and two expansion headers (LCD and peripheral application) that allow you to develop an application-specific daughter card for prototyping.

See "Switches and pushbuttons," "LEDs," and "Peripheral (expansion) headers" for more information.

Switches and pushbuttons



Reset control, S1

The reset pushbutton, S1, resets the module. On the module, RSTOUT# and PWRGOOD are produced for peripherals.

Power switch, S2

The development board has an ON/OFF switch, S2. This switch applies only to the +9VDC / +30VDC power supply. If you are using Power-over-Ethernet (PoE), see "PoE module connectors" on page 42.

User pushbuttons, S3 and S5

Use the user pushbuttons to interact with the applications running on the ConnectCore 9P 9360 module. Use these module signals to implement the pushbuttons:

Signal name	Switch (pushbutton)	GPIO used
USER_PUSH_BUTTON_1	S3	GPIO67
USER_PUSH_BUTTON_2	S5	GPIO68

Legend for multi-pin switches

Switches 4–8 are multi-pin switches. In the description tables for these switches, the pin is designated as *S[switch number].[pin number]*. For example, pin 1 in switch 4 is specified as S4.1.

Module configuration switches, S4

Use S4 to configure the module for normal operation or JTAG mode:

Switch pin	Function
S4.1	On = Scan mode for JTAG Off = Normal operation mode
S4.2	On = Flash write protect
S4.3	On = OCD debug mode (if S4.1 is on)
S4.4	Not used
S4.5 – S4.8	Not defined, but can be used by software

Serial port A configuration switches, S6

Use S6 to configure the line interface for serial port A:

Switch pin	Function
S6.1	On = RS232 buffer on Off = RS422/RS485
S6.2	Not used
S6.3	On = 2-wire interface (RS422/RS485) Off = 4-wire interface (RS422)
S6.4	On = Termination on Off = No termination

Serial port B configuration switch, S7

Use S7 to configure the line interface for serial port B:

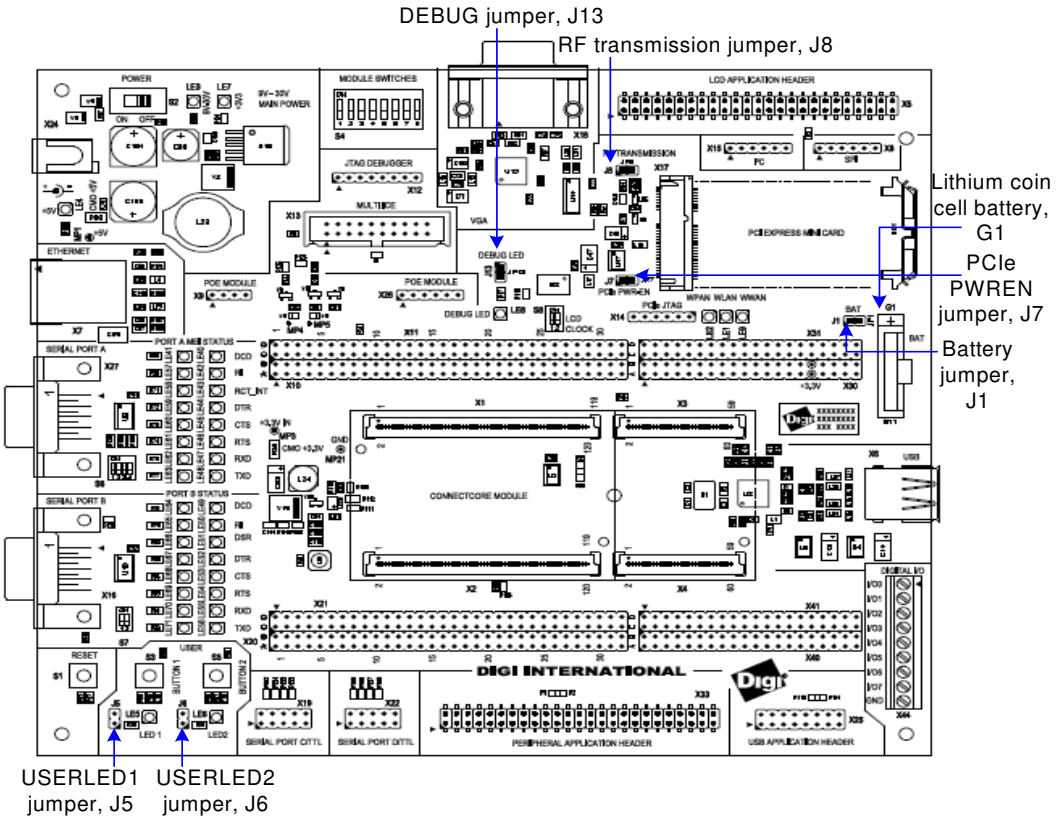
Switch pin	Function
S7.1	On = Enable auto-online mode. Reserved for future use. Off = Normal mode
S7.2	On = DIsable RS232 transceiver (all outputs in high impedance mode) Off = Enable RS232 transceiver

LCD clock configuration switches, S8

Use S8 to configure the LCD clock:

Switch pin	Function
S8.1	On = Supply CPU with 48 MHz for LCD. This switch can be set only if LCD_CLKIN / DCDA# is set to LCD_CLKIN (pin 107 on connector X1).
S8.2	Not connected

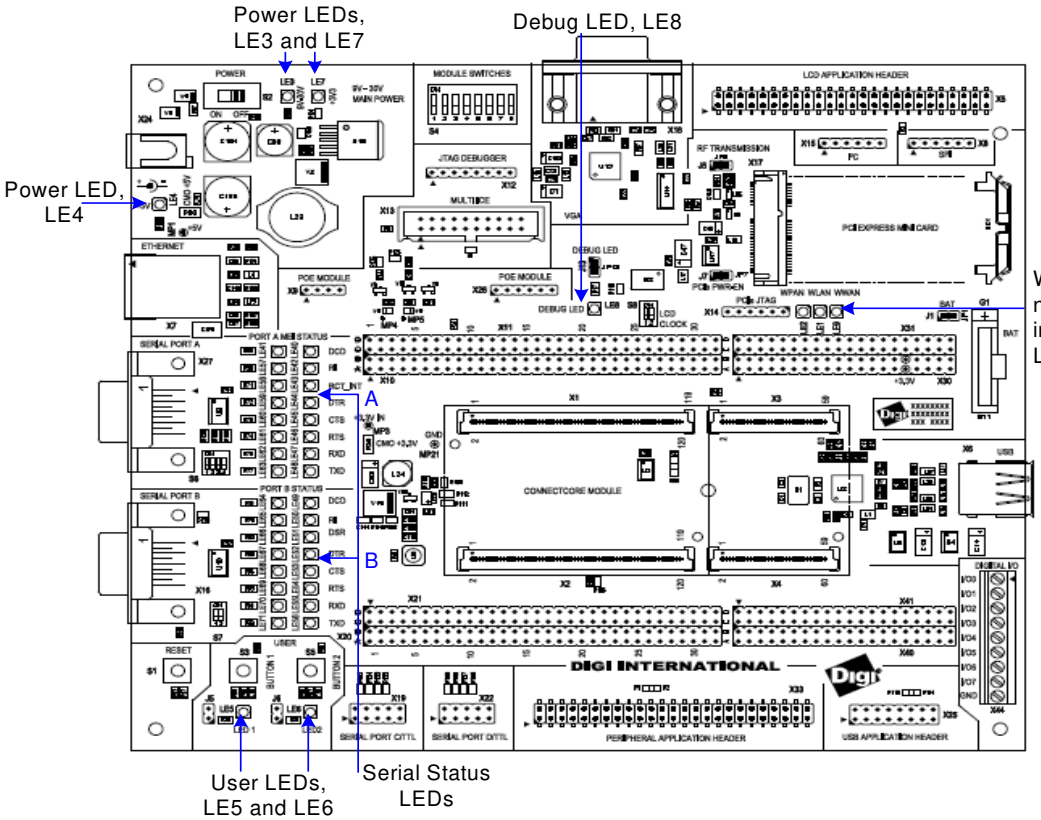
Jumpers



Jumper functions

Jumper	Name	If connection made	Default
1	Battery jumper	Supplies the real time clock with 3V from the battery (lithium coin cell battery, G1) even if the board is switched off. This is for keeping time in the RTC.	Connection made
5	USERLED1	Enables USERLED1 (LE5) to show the status of this signal (lit if low).	Connection not made
6	USERLED2	Enables USERLED2 (LE6) to show the status of this signal (lit if low).	Connection not made
7	PCIe PWREN	Enables the USB port power switch signal PCIe_PWRON# to switch +3.3V PCIe: low=off, high=on. *If no connection is made, 3.3V PCIe is always on.*	Connection made
8	RF transmission	Disables RF transmission on PCIe *If no connection is made, enables RF transmission on PCIe.*	Connection made
13	Debug LED	Enables DEBUGLED (LE8) to show the status of this signal (lit if high).	Connection made

LEDs



Wireless networking indicator LEDs, LE1, LE2, and LE9

The wireless area networking indicator LEDs indicate the type of wireless network being used, in conjunction with the PCIe Mini Card:

- LE1 indicates use of a wireless local area network (WLAN).
- LE2 indicates use of a wireless private area network (WPAN).
- LE9 indicates use of a wireless wide area network (WWAN).

Power LEDs, LE3, LE4, and LE7

The power LEDS are all red LEDs. These power supplies must be present and cannot be switched.

- LE3 ON indicates the +9VDC / +30VDC power supply.
- LE4 ON indicates the +5VDC from the main power supply.
- LE7 ON indicates the +3.3VDC power supply.

User LEDs, LE5 and LE6

The user LEDs are controlled through applications running on the ConnectCore 9P 9360 module, if J5 and J6 are set. Use these module signals to implement the LEDs:

Signal name	LED	GPIO used
USER_LED_1	LE5	GPIO46
USER_LED_2	LE6	GPIO66

Debug LED, LE8

The development board has a debug LED that provides software status information, if J13 is set.

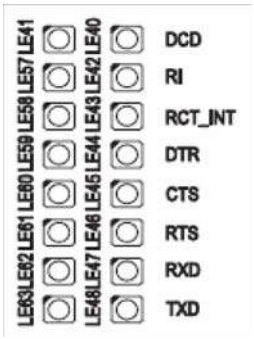
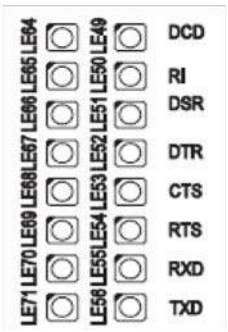
Use this module signal to implement the LED:

Signal name	LED	GPIO used
Debug LED	LE8	GPIO47

Serial status LEDs

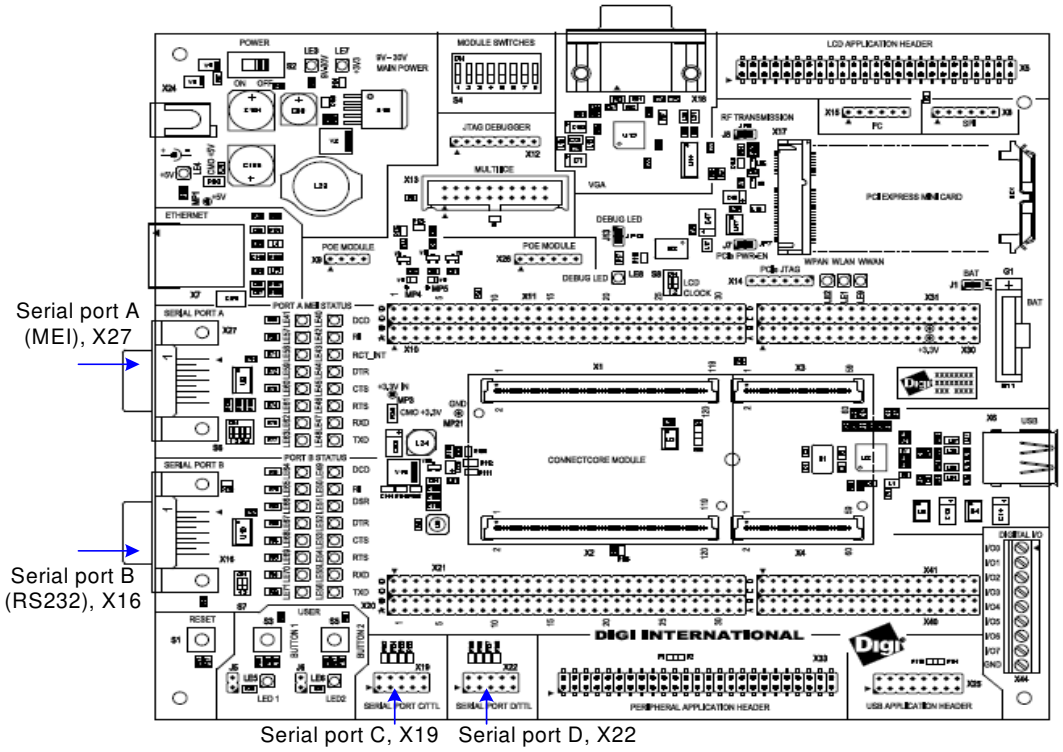
The development board has two sets of serial port LEDs—eight for serial port A and eight for serial port B. The LEDs are connected to the TTL side of the RS232 or RS422/485 transceivers.

- Green represents DB9 high.
- Red represents DB9 low.
- The intensity and color of the LED will change when the voltage is switching.

Serial port A LEDs	Name	Function	Serial Port B LEDs	Name	Function
	LE41 / LE40	DCD		LE64 / LE49	DCD
	LE57 / LE42	RI		LE65 / LE50	RI
	LE58 / LE43	RTC_IN (DSR)		LE66 / LE51	DSR
	LE59 / LE44	DTR		LE67 / LE52	DTR
	LE60 / LE45	CTS		LE68 / LE53	CTS
	LE61 / LE46	RTS		LE69 / LE54	RTS
	LE62 / LE47	RXD		LE70 / LE55	RXD
	LE63 / LE48	TXD		LE71 / LE56	TXD

Serial UART ports

The development board supports the four serial UART ports available on the ConnectCore 9P 9360 module.



Serial port A, MEI console interface

The serial (UART) port A connector, X27, is a DSUB9 male connector. This asynchronous serial port is DTE and requires a null-modem cable to connect to a computer serial port.

The serial port A MEI interface corresponds to NS9360 UART port A. The line driver is configured using switch S6. Note that all pins on S6 contribute to the line driver settings for this port.

Serial port A pins are allocated as shown:

Pin	RS232 function	RS485 function
1	DCD#	CTS-
2	RXD	RX+
3	TXD	TX+
4	DTR#	RTS-
5	GND	GND
6	DSR#	RX-
7	RTS#	RTS+
8	CTS#	CTS+
9	RI#	TX-

Serial port B, RS232 interface

The serial (UART) port B connector, X16, is a DSUB9 male connector. This asynchronous serial port is DTE and requires a null-modem cable to connect to a computer serial port.

The serial port B interface corresponds to NS9360 UART port B. The line driver is enabled or disabled using the switch S7.

Serial port B pins are allocated as shown:

Pin	Function	Comment
1	DCD# (SPIB_EN#)	Can be used if software sets this signal to UART function.
2	RXD (SPIB_DI)	Can be used if software sets this signal to UART function.
3	TXD (SPI_DO)	Can be used if software sets this signal to UART function.
4	DTR#	
5	GND	
6	DSR#	
7	RTS#	
8	CTS#	
9	RIB# (SPIB_CLK)	Can be used if software sets this signal to UART function.

Serial port C TTL interface

The serial (UART) port C interface is a TTL interface connected to a 2x5 pin, 0.1" connector, X19. The connector supports only TTL level.

The serial port C interface corresponds to NS9360 UART port C.

Serial port C pins are allocated as shown:

Pin	Function	Comment
1	No connect	
2	No connect	
3	RXD (LCDD17)	Can be used if software sets this signal to UART function.
4	RTS# (USB_PHY_D+)	Can be used if software sets this signal to UART function.
5	TXD (LCDD16)	Can be used if software sets this signal to UART function.
6	CTS# (USB_PHY_D-)	Can be used if software sets this signal to UART function.
7	No connect	
8	No connect	
9	GND	
10	3.3V	

Serial port D TTL interface

The serial (UART) port D interface is a TTL interface connected to a 2x5 pin, 0.1" connector, X22. The connector supports only TTL level.

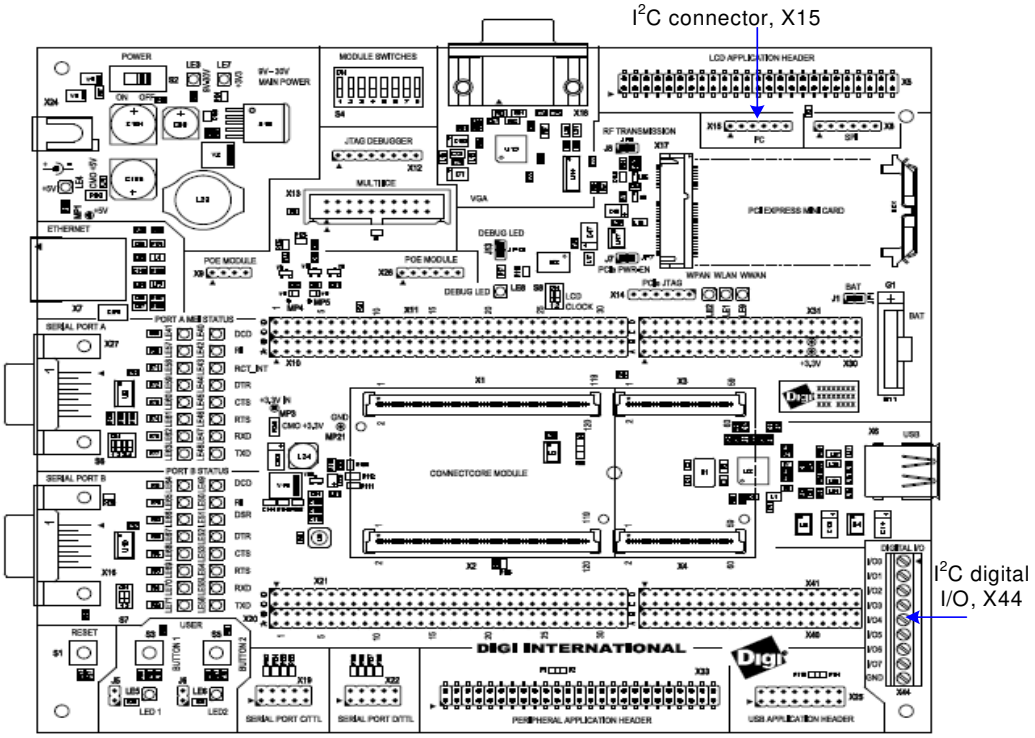
The serial port D interface corresponds to the NS9360 UART port D. The signals are shared with the SPIB interface, which is used for the touch interface if LCDAPKKITJS (purchased separately) is connected.

Serial port D pins are allocated as shown:

Pin	Function	Comment
1	No connect	
2	No connect	
3	RXD (USB_PHY_RCV)	Can be used if software sets this signal to UART function.
4	RTS# (USERLED1)	Can be used if software sets this signal to UART function.
5	TXD (USB_PHY_OE#)	Can be used if software sets this signal to UART function.
6	CTS# (USERLED2)	Can be used if software sets this signal to UART function.

Pin	Function	Comment
7	No connect	
8	No connect	
9	GND	
10	3.3V	

I²C interface



I²C EEPROM

I²C EEPROM is an optional feature. If you use it I²C EEPROM, attach a connector — ST M24C64, 6-pin connector —at X15 on the development board

Software uses I²C EEPROM to identify the hardware on which the module is running. LCDAPKITJS has an EEPROM on the same bus that enables the software to identify the LCD type, if connected.

I²C EEPROM pins are allocated as shown:

Pin	Signal
1	IIC_SDA
2	+3.3V

Pin	Signal
3	IIC_SCL
4	GND
5	No connect
6	No connect

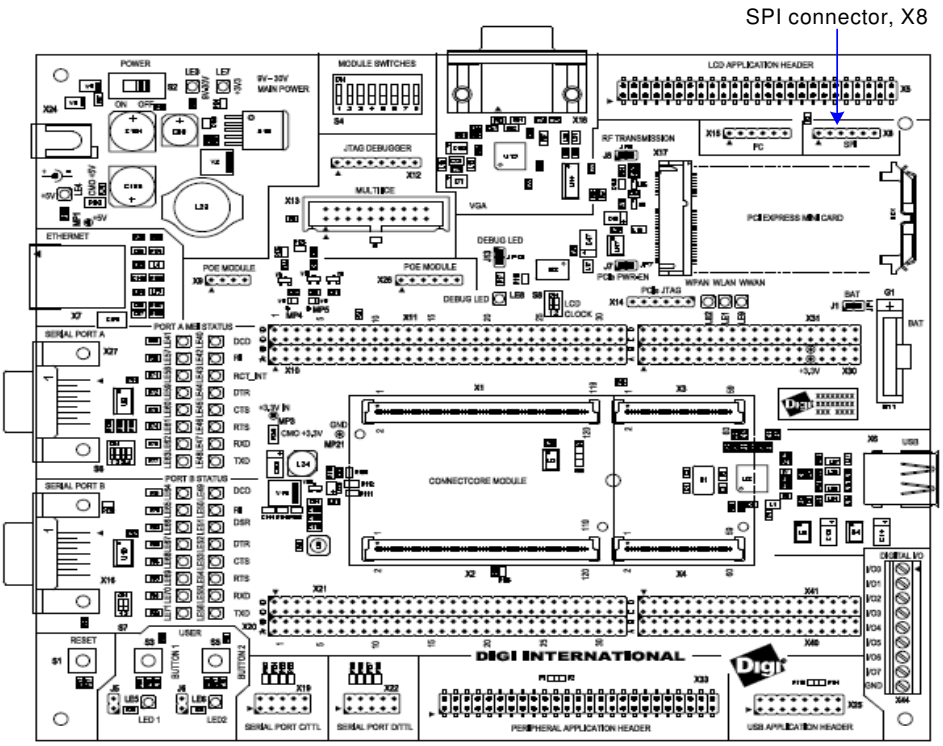
I²C digital I/O expansion

The development board provides a standard 2.54mm (0.10") connector, X44, for additional digital I/Os. The I²C I/O port chip is on-chip ESD-protected, 5V tolerant, and provides an open drain interrupt that is shared with the touch screen interrupt from the optional LCD application board.

The digital I/O connector is a Philips PCA9554D at I²C address 0x20 / 0x21. The pins are allocated as shown:

Pin	Signal
1	IO_0
2	IO_1
3	IO_2
4	IO_3
5	IO_4
6	IO_5
7	IO_6
8	IO_7
9	GND

SPI interface



The development board provides access to the SPI interface on the module using the SPI connector, X8. Because the module's SPI interface is shared with a UART interface, you cannot use both simultaneously. The SPI interface on the development board is shared with UART_B (NS9360 port B).

Note: The primary function of UART port B is to support RS232; SPI support is the secondary function. To move from RS232 to SPI, you need to configure the software. If LCDAPKITJS is connected, this port is reserved for the touch interface.

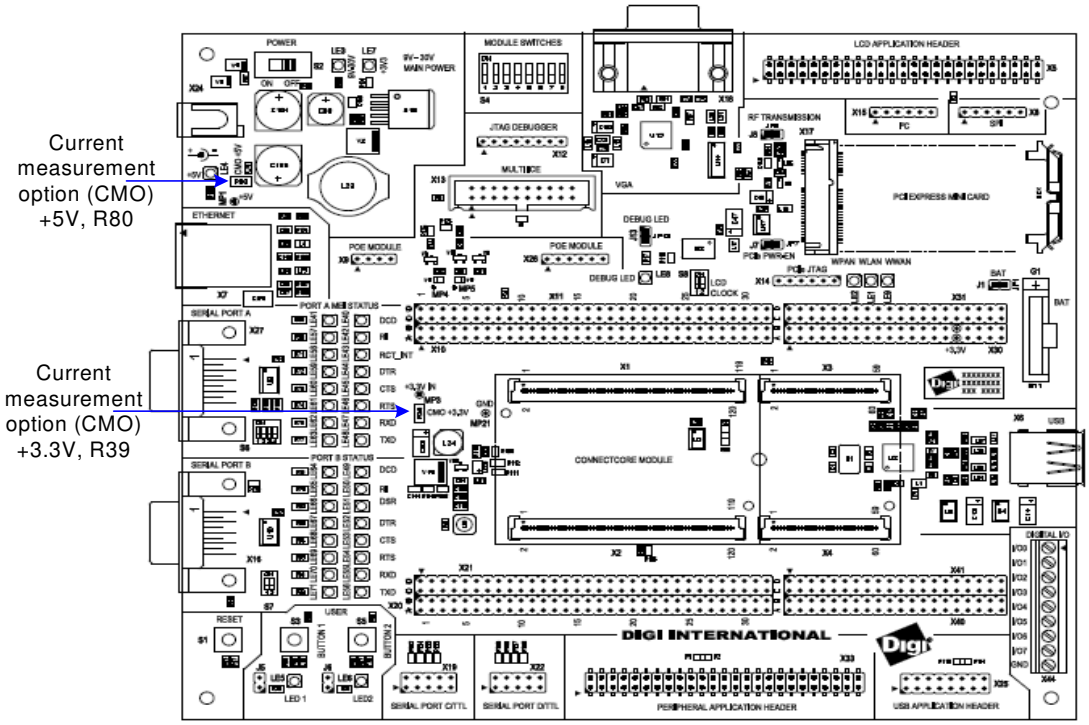
Pin allocation

SPI connector pins are allocated as shown:

Pin	Signal
1	+3.3V
2	TXDB / SPIB_DO
3	RXDB / SPI_DI
4	RIB / SPI_CLK
5	DCDB# / SPIB_EN
6	GND

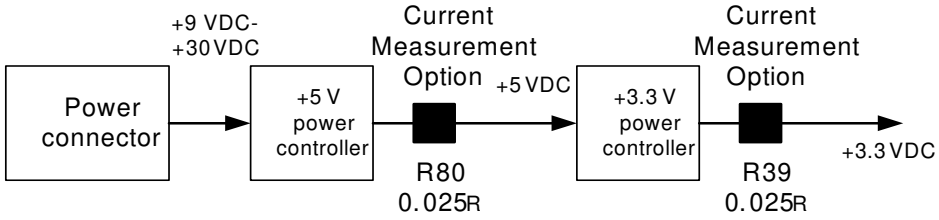
Current Measurement Option

The Current Measurement Option uses 0.025R ohm series resistors to measure the current on the development board's +3.3VDC (R39) and +5VDC (R80) power supplies.



How the CMO works

This drawing shows how the Current Measurement Option works.

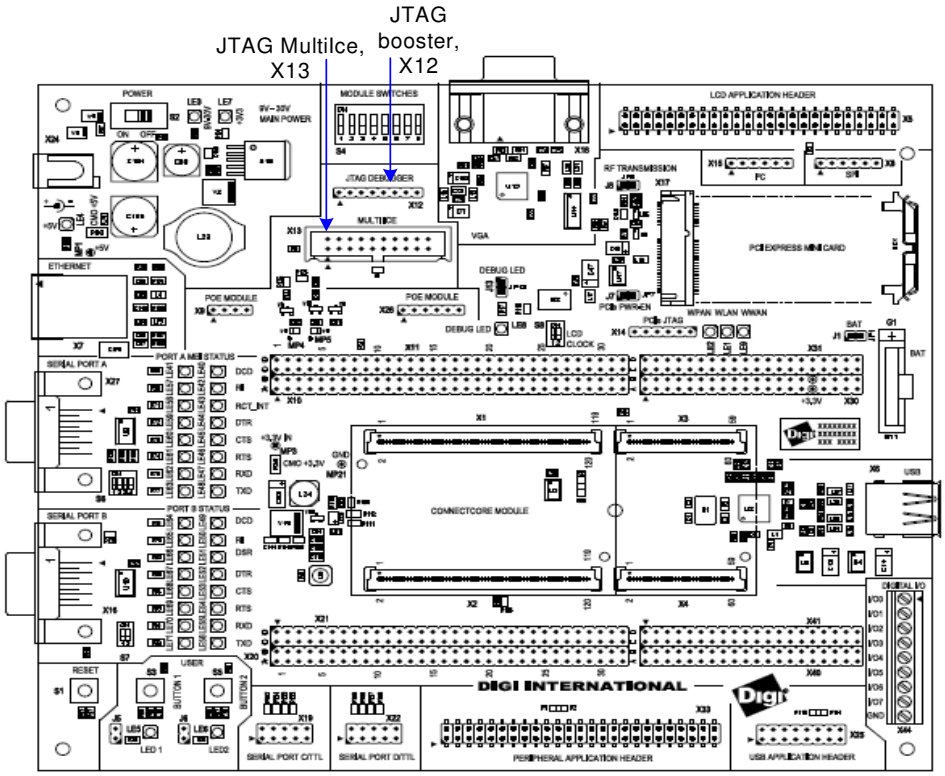


To measure the load current used on different power supplies, measure DC voltage across the sense (CMO) resistor. The value of the resistor is 0.025R ± 1% Calculate the current using this equation: I = U/R

where

- I = current in Amps
- U = measured voltage in Volts
- R = 0.025 Ohms

JTAG interface



Standard JTAG ARM connector, X13

The standatd JTAG ARM connector is a 20-pin header and can be used to connect development tools such as ARM's Multi-ICE, Digi's JTAG Link, Abatron BIDI2000, and others.

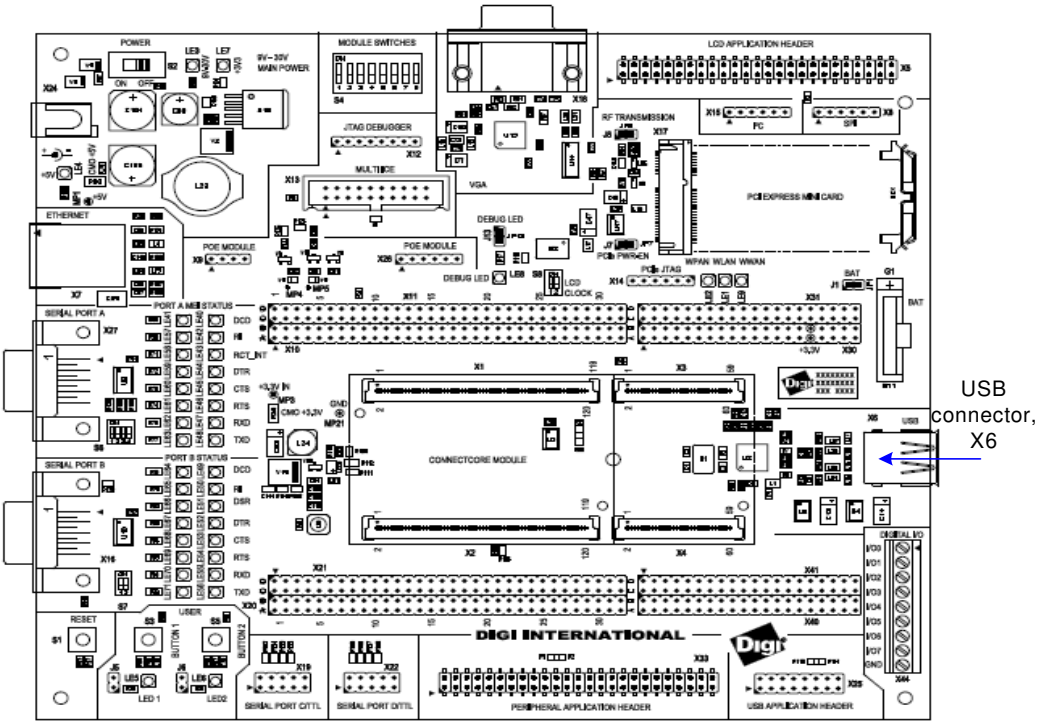
Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	TRST#	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	RTCK (not connected)	12	GND
13	TDO	14	GND
15	PWRGOOD	16	GND
17	No connect	18	GND
19	No connect	20	GND

JTAG Booster, X12

You can use a JTAG booster that allows accelerated programming of the on-board Flash. The development board provides a single row 8-pin header (X12) for connecting the JTAG booster.

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TMS	4	TRST#
5	No connect	6	TDI
7	TDO	8	+3.3V

USB Host and Device functionality



USB Host port

The USB Host is connected to a 4-port USB hub, X6, on the development board.

- USB ports 1 and 2 are connected to X6.
- USB port 3 is the PCIe socket.
- USB port 4 is not used.

USB Device: USB application header, X25

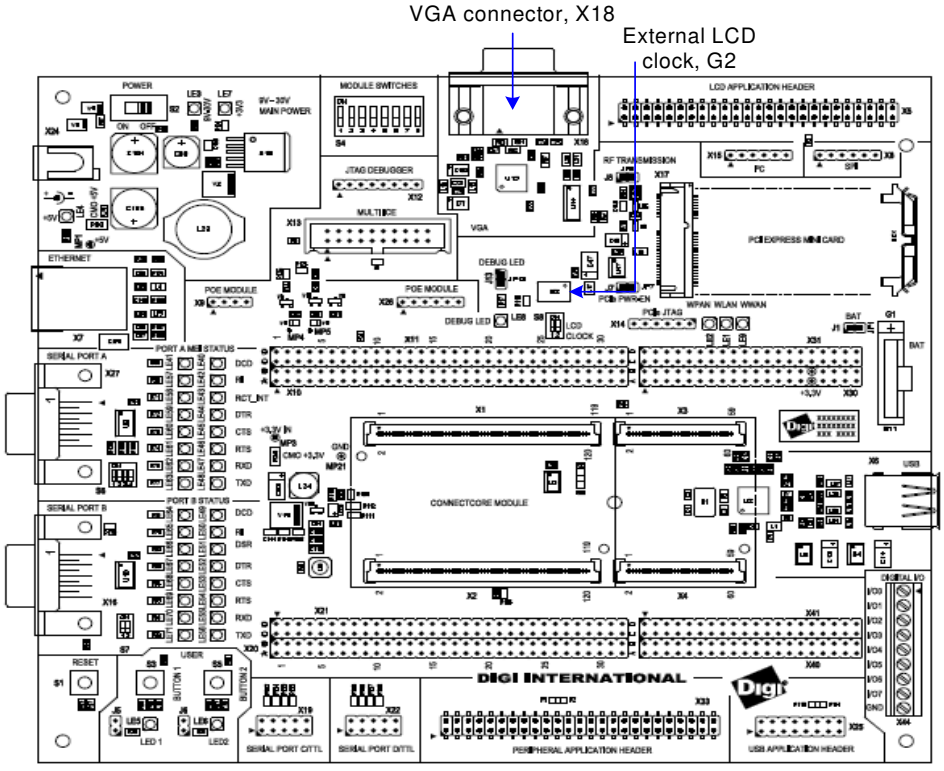
You can add USB Device functionality using the USB application header. This is a 2x8-pin connector, labeled X25 on the development board.

USB header pins are allocated as shown:

Pin	Signal	Pin	Signal
1	+3.3V	2	+5V
3	+5V	4	GND
5	RTSC# / USB_PHY_D+	6	CTSC# / USB_PHY_D-
7	GND	8	GND
9	TXDD / USB_PHY_OE#	10	USB_EXTPHY_SUSP
11	USB_SPEED	12	RXDD / USB_PHY_RCV
13	USB_ENUM	14	GND
15	IIC_SDA	16	IIC_SCL

VGA interface

The development board provides a D-SUB, 15-pin connector, X18, to support the [module's] VGA interface.



Reserved signals

To use the interface, reserve these LCD signals:

- 18 LCD data signals —LCCD0–LCDD17
- LCD_BIAS
- LCD_CLOCK
- LCD_HSYNC
- LCD_VSYNC

VGA pinout

The VGA pins are allocated as shown. Signals marked with an asterisk are analog 0.7V p-p positive signals to 75 ohm load. All other signals are TTL level signals.

Pin	Signal	Pin	Signal
1	Red out*	2	Green out*
3	Blue out*	4	No connect
5	GND	6	Red return
7	Green return	8	Blue return
9	No connect	10	Sync return
11	No connect	12	No connect
13	Horizontal sync out	14	Vertical sync out
15	No connect		

External LCD clock, G2

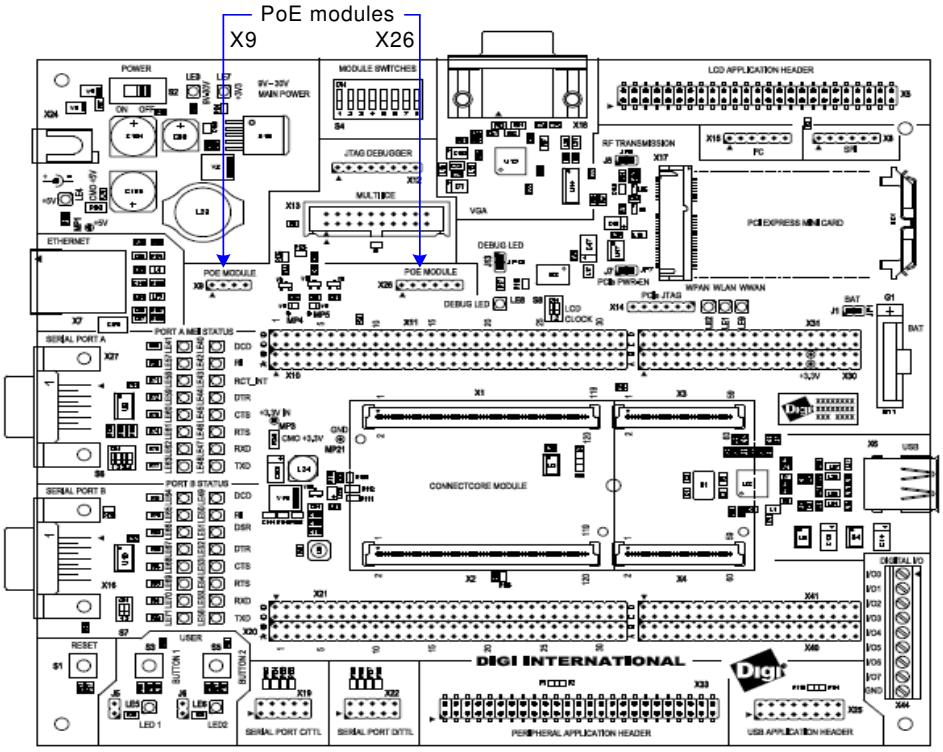
An external LCD controller clock is provided to avoid picture quality deterioration due to the low-emission spread spectrum clock used on the module.

G2 is a 48.000MHz oscillator that must be used for VGA monitors if the module has a spread spectrum oscillator.

PoE module connectors

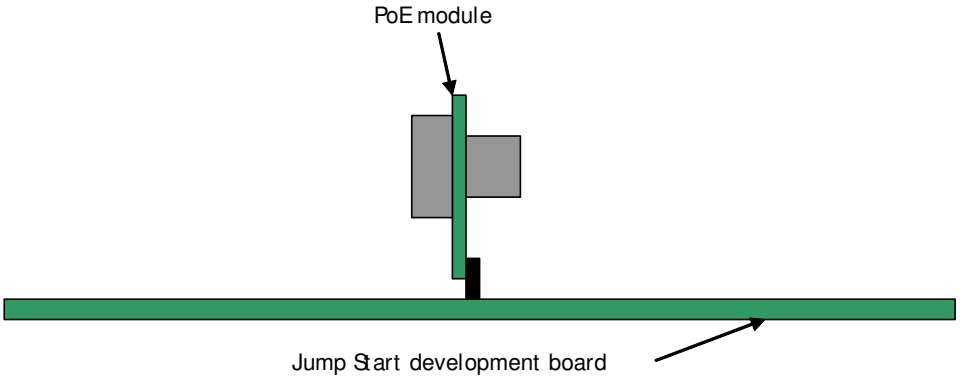
The development board has two PoE module connectors, X9 and X26. The PoE module is an extra-power module that can be plugged on the development board through the two connectors:

- X9, input connector: Provides access to the poE signals coming from the Ethernet interface.
- X26, output connector: Provides the output power supply from the PoE module.



The PoE module

Plug in the PoE module at a right angle to the development board, as shown in this drawing:



X9

This is how the PoE input connector pins are allocated:

Pin	Signal
1	POE_TX_CT
2	POE_RX_CT
3	POE_RJ45_4/5
4	POE_RJ45_7/8

X26

This is how the PoE output connector pins are allocated:

Pin	Signal
1	+12V_PoE
2	+12V_PoE
3	GND
4	GND
5	PoE_GND
6	PoE_GND

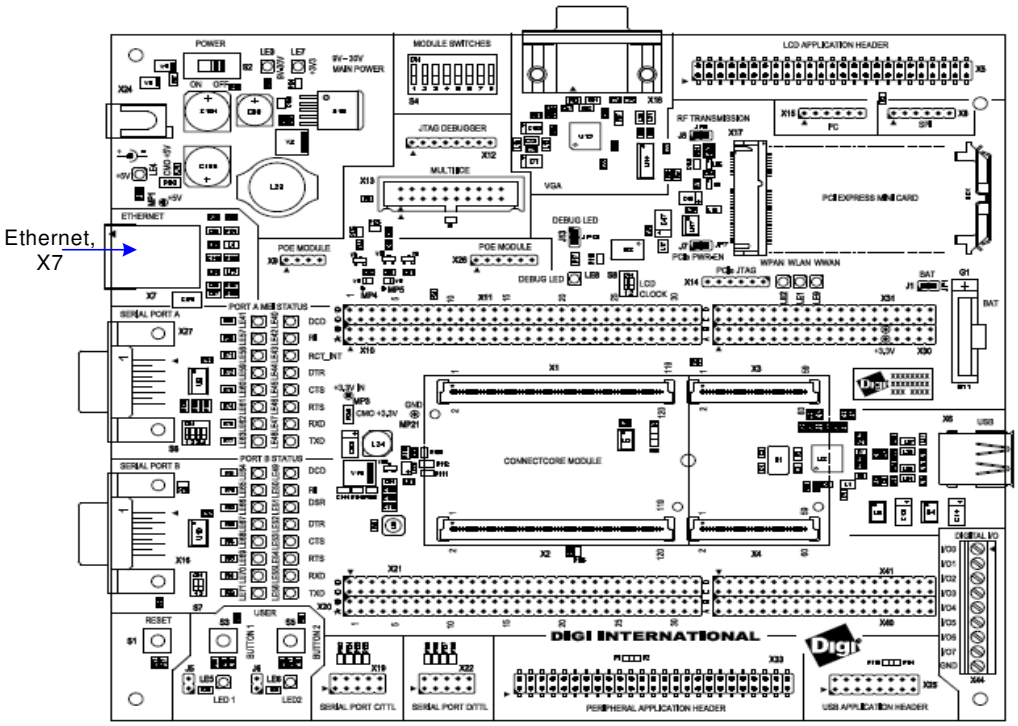
POE_GND

The development board provides access to POE_GND, which allows the PoE module to be switched off once a power cable is plugged on the development board.

Ethernet interface

The module provides the 10/100 Ethernet MII PHY chip. The development board provides the 1:1 transformer and Ethernet connector.

The Ethernet connector is an 8-wire RJ-45 jack, labeled X7, on the development board. The connector has eight interface pins, as well as two integrated LEDS that monitor network information.



RJ-45 pin allocation

RJ45 connector pins are configured as shown:

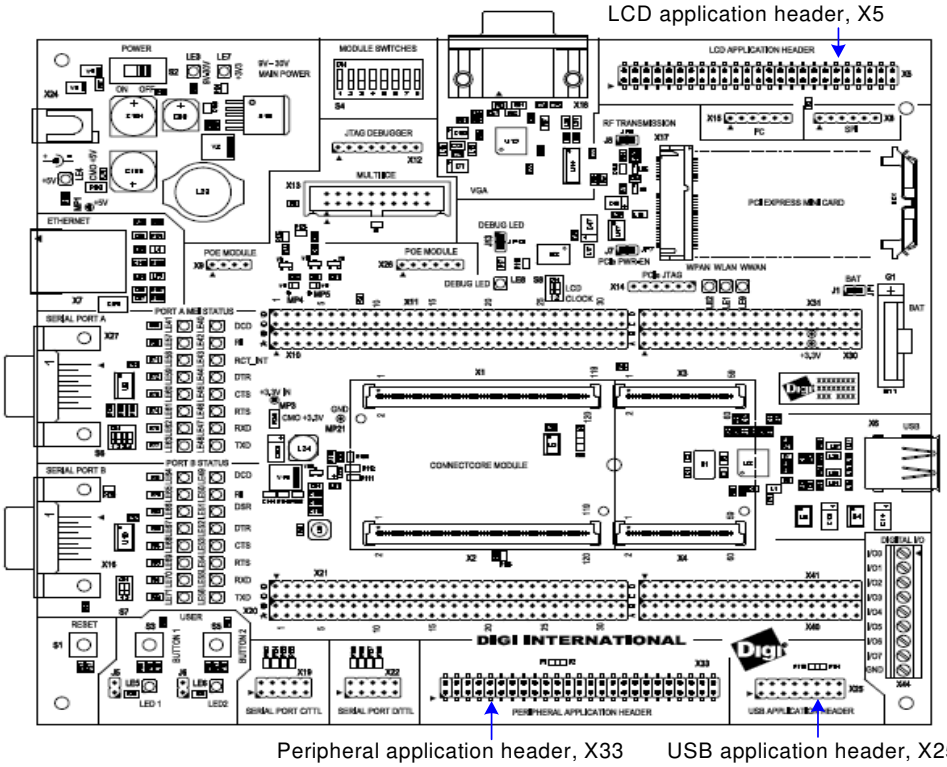
Pin	Signal	Ethernet / PoE / Other
1	TD+	ETH_TPOP
2	TD-	ETH_TPON
3	RD+	ETH_TPIP
4	CT	+3.3V
5	CT	POE_TX_CT
6	RD-	ETH_TPIN
7	CT	+3.3V
8	CT	POE_RX_CT

LEDs

The RJ-45 connector has two LEDs located near the outer lower corners of the connector. These LEDs are not programmable.

LED	Description
Yellow	Network activity (speed): Flashing when network traffic detected; Off when no network traffic detected.
Green	Network link: On indicates an active network link; Off indicates that no network link is present.

Peripheral (expansion) headers



The development board provides two, 2x25-pin, 0.10" (2.54mm) pitch headers for supporting application-specific daughter cards/ expansion boards:

- X5, LCD application header. Provides access to the LCD signals and SPI signals for touch controller purposes. Use with a Digi-provided application kit or attach your own application board.
- X33, Peripheral application header. Provides access to an 8-bit data bus, 8-bit address bus, and control signals (such as CE#, WE#), as well as I^2C and power. Using these signals, you can connect Digi-specific extension modules or your own daughter card to the module's address/ data bus.

The development board also provides a 2x8-pin USB application header, X25. See "USB Device: USB application header, X25" on page 41 for description and pinout information.

LCD application header, X5

LCD application header pins are allocated as shown:

Pin	Signal	Pin	Signal
1	GND	2	LCD_D0 / GPIO24
3	LCD_D1 / GPIO25	4	LCD_D2 / GPIO26

Pin	Signal	Pin	Signal
5	LCD_D3 / GPIO27	6	GND
7	LCD_D4 / GPIO28	8	LCD_D5 / GPIO29
9	LCD_D6 / GPIO30	10	LCD_D7 / GPIO31
11	GND	12	LCD_D8 / GPIO32
13	LCD_D9 / GPIO33	14	LCD_D10 / GPIO34
15	LCD_D11 / GPIO35	16	GND
17	LCD_D12 / GPIO36	18	LCD_D13 / GPIO37
19	LCD_D14 / GPIO38	20	LCD_D15 / GPIO39
21	GND	22	LCD_D16 / TXDC
23	LCD_D17 / RXDC	24	Reserved (LCD_D18)
25	Reserved (LCD_D19)	26	GND
27	Reserved (LCD_D20)	28	Reserved (LCD_D21)
29	IIC_SDA	30	IIC_SCL
31	GND	32	LCD_CLK / GPIO20
33	LCD_BIAS / GPIO22	34	LCD_HSYNC / GPIO19
35	LCD_VSYNC / GPIO21	36	IRQ1 / GPIO69
37	LCD_PWREN / GPIO18	38	+3.3V
39	Reserved (TSPX)	40	Reserved (TSPY)
41	Reserved (TSMX)	42	Reserved (TSMY)
43	+3.3V	44	RIB / SPIB_CLK
45	DCDB# / SPIB_EN#	46	TXDB / SPIB_DO
47	RXDB / SPIB_DI	48	+3.3V
49	GND (TOUCH / SPI#)	50	GND

Peripheral application header, X33

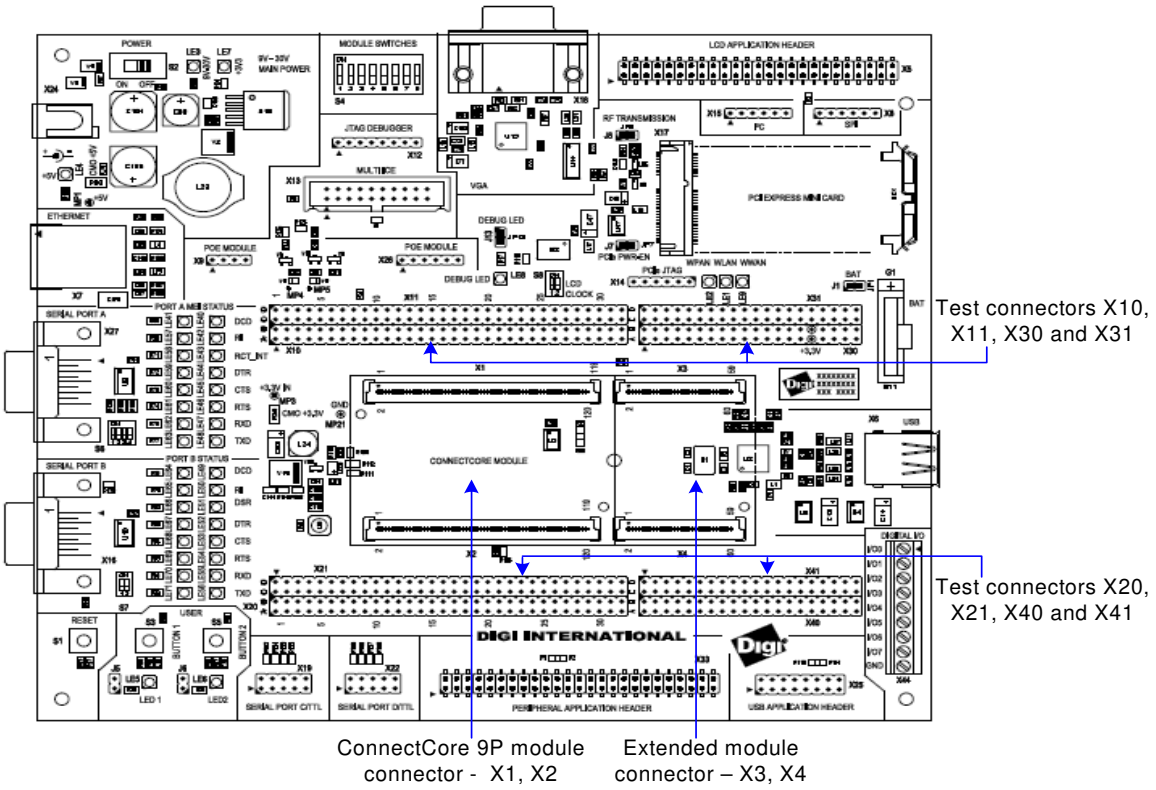
Peripheral application pins are allocated as shown:

Pin	Signal	Pin	Signal
1	GND	2	D0
2	D1	4	D2
5	D3	6	GND
7	D4	8	D5
9	D6	10	D7
11	GND	12	D8
13	D9	14	D10

Pin	Signal	Pin	Signal
15	D11	16	GND
17	D12	18	D13
19	D14	20	D15
21	GND	22	8 bit / 16 bit# 3.3V selects 8-bit data bus
23	GND	24	+3.3V
25	+3.3V	26	A0
27	A1	28	A2
29	A3	30	GND
31	A4	32	A5
33	A6	34	A7
35	GND	36	A8
37	A9	38	GND
39	EXT_CS0#	40	IIC_SDA
41	WE#	42	EXT_OE#
43	IIC_SCL	44	IRQ1_GPIO69
45	+3.3V	46	+3.3V
47	RTSC# / USB_PHY_D+	48	CTSC# / USB_PHY_D-
49	No connect	50	GND

Module and test connectors

The ConnectCore 9P 9360 module plugs into the module connectors X1 and X2 on the development board. The extended module, if used, plugs into connectors X3 and X4.



Module and extended module connectors

See "Module pinout" on page 2 and "Extended module" on page 24 for pinout and related information.

Test connectors

The development board provides two 4x32 pin test connectors, labeled X10/ X11 and X20/ X21. These connectors are 1:1 copies of the module pins and are used for measurement or test purposes.

- X10 and X11 correspond to module connector X1.
- X20 and X21 correspond to module connector X2.

The development board also provides two 4x20 pin test connectors for the extended modules:

- X30 and X31 correspond to extended module connector X3.
- X40 and x41 correspond to extended module connector X4.

X10 pinout

X10 pin	Signal	X10 pin	Signal
A1	GND	B1	RTSIN#
A2	TCK	B2	TMS
A3	TRST#	B3	DEBUG_EN# (CONF0)
A4	X1_X13 (CONF3)	B4	CONF4 / GPIO38 (CONF4)
A5	CONF7 / GPIO41 (CONF7)	B5	TXDA
A6	CTSA#	B6	DTRA#
A7	RXDB / SPIB_DI	B7	RTSB#
A8	DSRB#	B8	RIB_ / SPIB_CLK
A9	USER_KEY_2 / GPIO68	B9	IRQ1 / GPIO69
A10	LCD_D0 / GPIO24	B10	LCD_D1 / GPIO25
A11	LCD_D3 / GPIO27	B11	LCD_D4 / GPIO28
A12	LCD_D7 / GPIO31	B12	LCD_D8 / GPIO32
A13	LCD_D11 / GPIO35	B13	LCD_D12 / GPIO36
A14	LCD_D15 / GPIO39	B14	LCD_D16 / TXDC
A15	CTSC# / USB_PHY_D-	B15	TXDD / USB_PHY_OE#
A16	DEBUGLED / GPIO47	B16	LCD_PWREN# / GPIO18
A17	LCD_HSYNC / GPIO19	B17	LCD_CLK / GPIO20
A18	A1	B18	A2
A19	A5	B19	A6
A20	A9	B20	A10
A21	A12	B21	A13
A22	A16	B22	A17
A23	A20	B23	A21
A24	WE#	B24	USER_KEY_1 / GPIO67
A25	EXT_CS3#	B25	X1_98
A26	USB_EXTPHY_SUSP	B26	USB_OVRCURR
A27	EXT_BE2#	B27	EXT_BE3#
A28	X1_109	B28	RIA#
A29	USB_ENUM	B29	USB_INTPHY_P
A30	GND	B30	GND
A31	No connect	B31	No connect
A32	3.3V_IN	B32	3.3V_IN

X11 pinout

X11 pin	Signal	X11 pin	Signal
C1	PWRGOOD	D1	RSTOUT#
C2	TDI	D2	TDO
C3	CONF1 (CONF1)	D3	OCD_EN# (CONF2)
C4	CONF5 / GPIO39 (CONF5)	D4	CONF6 / GPIO40 (CONF6)
C5	RXDA	D5	RTSA#
C6	RTC_INT#	D6	TXDB / SPIB_DO
C7	CTSB#	D7	DTRB#
C8	DCDB# / SPIB_EN#	D8	WAIT#
C9	X1_35	D9	X1_36
C10	GND	D10	LCD_D2 / GPIO25
C11	LCD_D5 / GPIO29	D11	LCD_D6 / GPIO30
C12	LCD_D9 / GPIO33	D12	LCD_D10 / GPIO34
C13	LCD_D13 / GPIO37	D13	LCD_D14 / GPIO38
C14	LCD_D17 / RXDC	D14	RTSC# / USB_PHY_D+
C15	RXDD / USB_PHY_RCV	D15	USERLED1 / GPIO45
C16	LCD_BIAS / GPIO22	D16	LCD_VSYNC / GPIO21
C17	GPIO23	D17	A0
C18	A3	D18	A4
C19	A7	D19	A8
C20	GND	D20	A11
C21	A14	D21	A15
C22	A18	D22	A19
C23	USERLED2 / GPIO66	D23	EXT_OE#
C24	EXT_CS0#	D24	EXT_CS2#
C25	PWREN	D25	X1_100
C26	EXT_BE0#	D26	EXT_BE1#
C27	LCD_CLKIN / DCDA#	D27	X1_108
C28	IIC_SCL	D28	IIC_SDA
C29	USB_INTPHY_N	D29	VRTC
C30	VLIO	D30	VLIO
C31	No connect	D31	No connect
C32	3.3V_IN	D32	3.3V_IN

X20 pinout

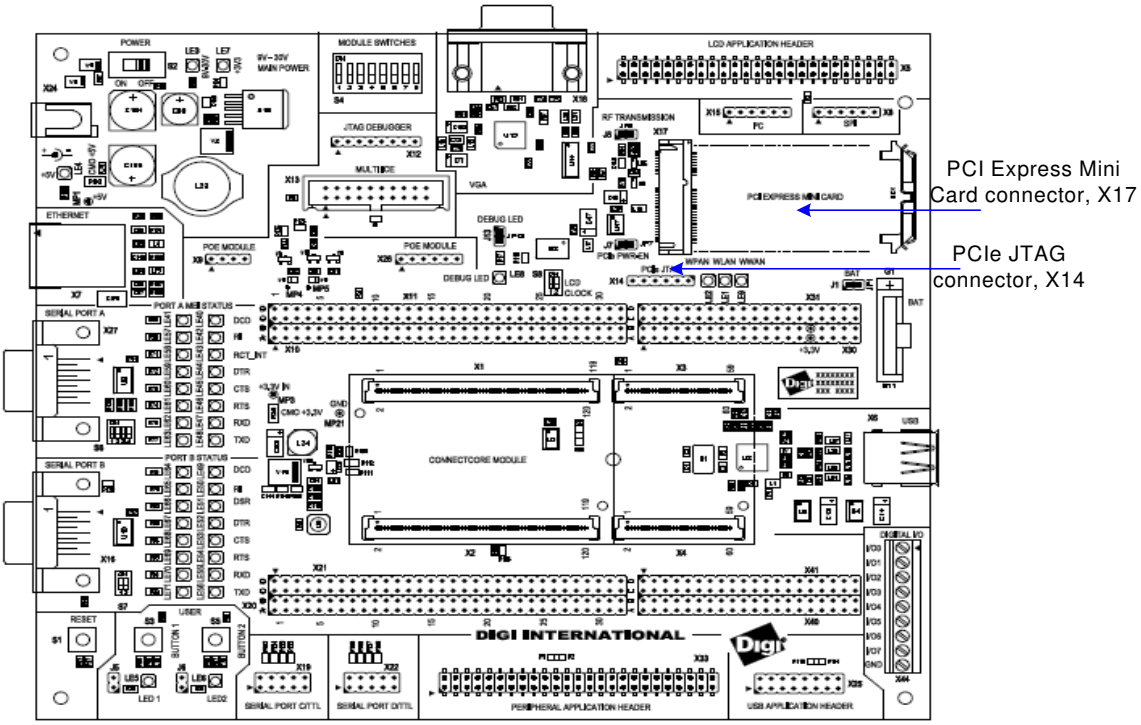
X20 pin	Signal	X20 pin	Signal
A1	X2_1	B1	GND
A2	X2_5	B2	X2_6
A3	X2_9	B3	X2_10
A4	X2_13	B4	GND
A5	X2_17	B5	X2_18
A6	X2_21	B6	X2_22
A7	X2_25	B7	X2_26
A8	X2_29	B8	X2_30
A9	X2_33	B9	X2_34
A10	X2_37	B10	X2_38
A11	X2_41	B11	X2_42
A12	X2_45	B12	X2_46
A13	X2_49	B13	X2_50
A14	X2_53	B14	X2_54
A15	X2_57	B15	X2_58
A16	X2_61	B16	X2_62
A17	X2_65	B17	ETH_TPIN
A18	ETH_LEDH	B18	ETH_TPON
A19	X2_73	B19	X2_74
A20	X2_77	B20	X2_78
A21	D0	B21	D1
A22	D4	B22	D5
A23	D8	B23	D9
A24	D12	B24	D13
A25	D16	B25	D17
A26	D20	B26	D21
A27	D24	B27	D25
A28	D28	B28	D29
A29	X2_113	B29	X2_114
A30	Reserved	B30	Reserved
A31	VLIO	B31	VRTC
A32	+3.3V	B32	+3.3V

X21 pinout

X21 pin	Signal	X21 pin	Signal
C1	X2_3	D1	X2_4
C2	X2_7	D2	GND
C3	X2_11	D3	X2_12
C4	X2_15	D4	X2_16
C5	X2_19	D5	X2_20
C6	X2_23	D6	X2_24
C7	X2_27	D7	X2_28
C8	X2_31	D8	X2_32
C9	X2_35	D9	X2_36
C10	X2_39	D10	GND
C11	X2_43	D11	X2_44
C12	X2_47	D12	X2_48
C13	X2_51	D13	X2_52
C14	X2_55	D14	X2_56
C15	X2_59	D15	X2_60
C16	X2_63	D16	X2_64
C17	ETH_LEDLNK	D17	ETH_TPIP
C18	ETH_ESD0	D18	ETH_TPOP
C19	X2_75	D19	X2_76
C20	X2_79	D20	GND
C21	D2	D21	D3
C22	D6	D22	D7
C23	D10	D23	D11
C24	D14	D24	D15
C25	D18	D25	D19
C26	D22	D26	D23
C27	D26	D27	D27
C28	D30	D28	D31
C29	X2_115	D29	X2_116
C30	BCLKOUT	D30	GND
C31	GND	D31	GND
C32	RSTIN#	D32	PWRGOOD

PCIe Mini Card

The development board supports a PCI Express (PCIe) Mini Card. The card attaches to the development board at X17. The board also provides a PCIe-specific JTAG connector, labeled X14.



PCIe Mini Card pin allocation

The PCIe Mini Card connector pins are allocated as shown:

Pins	Signal	Pins	Signal
1	No connect	2	3
3	No connect	4	GND
5	No connect	6	No connect
7	No connect	8	No connect
9	GND	10	No connect
11	No connect	12	No connect
13	No connect	14	No connect
15	GND	16	No connect
17	No connect	18	GND
19	No connect	20	W_DISABLE#
21	GND	22	PERST#

Pins	Signal	Pins	Signal
23	No connect	24	No connect
25	No connect	26	GND
27	GND	28	No connect
29	GND	30	No connect
31	No connect	32	No connect
33	No connect	34	GND
35	GND	36	PCIe_USB_N
37	GND	38	PCIe_USB_P
39	+3.3V_PCIe	40	GND
41	+3.3V_PCIe	42	+3.3V_PCIe (LED WWAN)
43	GND	44	+3.3V_PCIe (LED WLAN)
45	PCIe_TCK	46	+3.3V_PCIe (LED WPAN)
47	PCIe_TMS	48	No connect
49	PCIe_TDO	50	GND
51	PCIe_TDI	52	+3.3V_PCIe

PCIe JTAG pin allocation

The PCIe JTAG header pins are allocated as shown:

Pin	Signal
1	+3.3V_PCIe
2	GND
3	PCIe_TCK
4	PCIe_TDO
5	PCIe_TDI
6	PCI_TMS

Power

The development board is powered by the main power supply, +9VDC / +30VDC.

Power supplies

The development board power supply input supports an external supply voltage between 9VDC and 30VDC. The development board power supply section splits and regulates the input supply into two stable onboard voltage levels:

- +5VDC, which is used on the development board

- +3.3VDC, which powers the ConnectCore 9P 9360 module

At powerup, the module is powered by 3.3V_IN. After 3.3V_IN is stable, the module hardware switches on the peripheral 3.3V power supply.

Module and Development Board Specifications

APPENDIX A

This appendix provides ConnectCore 9P 9360 module and electrical specifications, as well as module and development board mechanical specifications.

Temperature ranges

The module temperature range depends on which clock speed you are using:

- 0° C–70° C with 177 MHz clock
- -40° C–+85° C with 155 MHz clock

Mechanical specifications

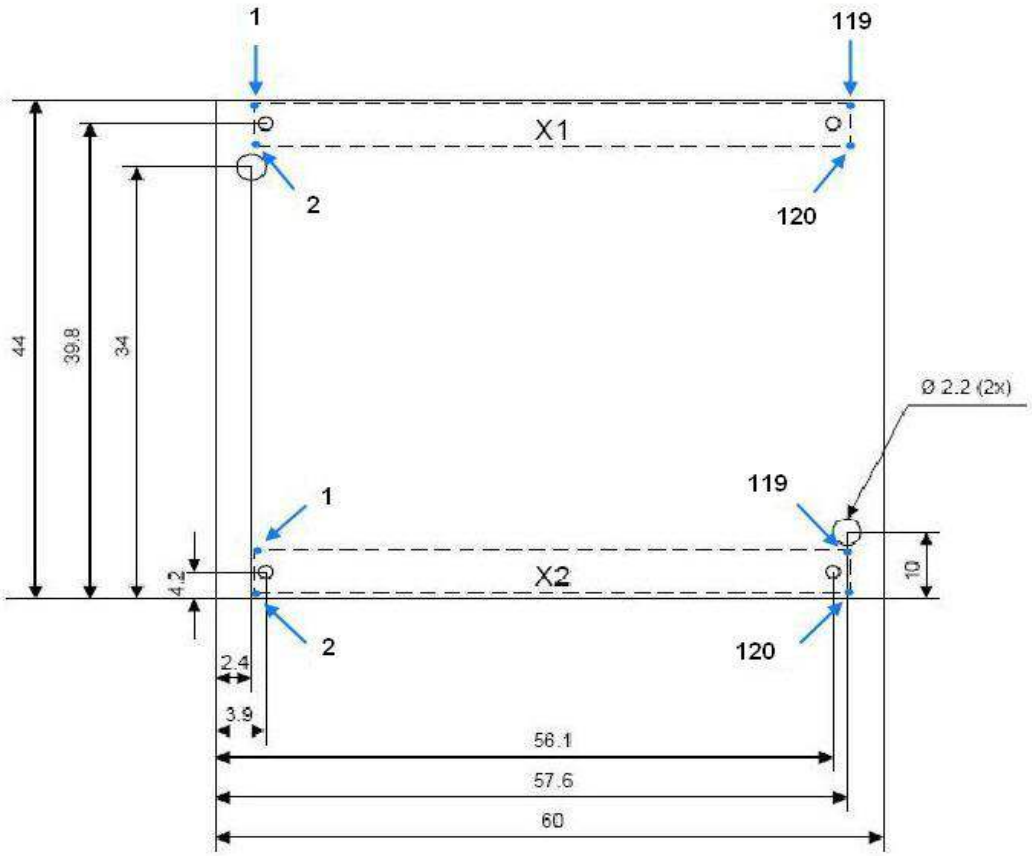
The module size is 60 x 44mm.

Two board-to-board connectors are used on the module. The distance between the module and the base board depends on the counterpart on the base board. The minimum distance is 5mm.

The height of the parts mounted on the bottom side of the module should not exceed 2.5mm. The height of the parts mounted on the top side of the module should not exceed 4.1mm.

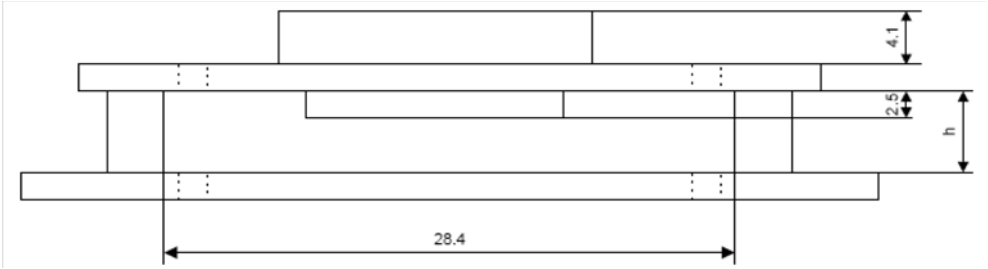
Module, top view

Note: Measurements are in millimeters.



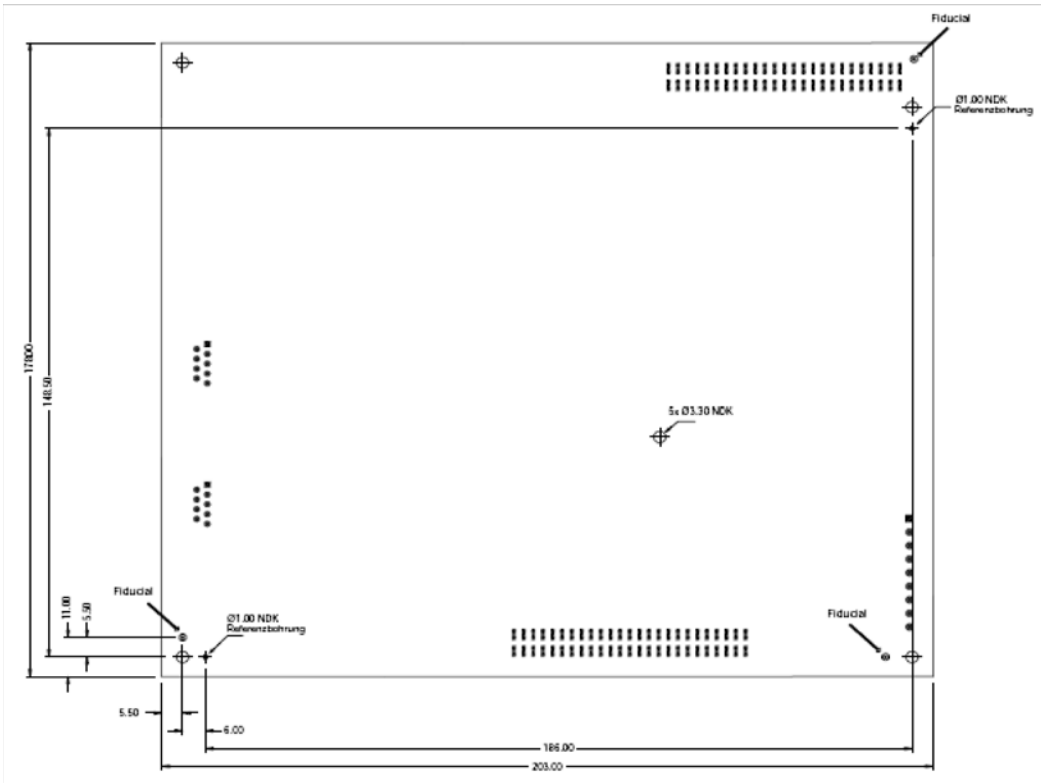
Module, side view

Note: Measurements are in millimeters.



Development board, top view

Note: Measurements are in millimeters.



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