- **Cancels the Acoustic Echo Common in Hands-Free Use of Cellular Phones in Automobiles**
  - **Eliminates Echo Created by Speaker Output Feeding Back Into the Microphone**
- **Suppresses Wind, Engine, and Tire Noise**
- **Line Echo Canceler**
- **Standard Independent**
  - **IS-54B, IS-136, GSM, AMPS, IS-95**
- **Continuous, Automatic Adaptation to Changing Acoustic Environment**
  - **Initial System Training Not Required**
- **Based on TMS320C5x Platforms**
- **Support for Industry Standard Microcontrollers**
- **Interfaces Easily with TI's Voice Codec, the TCM320AC36**
- **Acoustic Echo Canceler Performance**
  - **Length of Echo Path up to 44 ms**
  - **Initial Adaptation Rate $>$20 dB/s for Speech Signals**
  - **Zero Speech Delay**
  - **Echo Return Loss up to 30 dB for Speech Echo in Automobiles and 41 dB for Sine Wave Input**
- **Noise Suppressor Performance**
  - **Up to 10 dB Noise Suppression for Hands-Free Use of Cellular Phones in Automobiles Without Distorting Speech Signals**
  - **16 ms Processing Delay**
  - **Continuous Adaptation**
- **Demonstration Platform**
  - **Allows Evaluation of Software Algorithm Performance in Lab and Automobile**
  - **Ability to Enable/Disable AEC, ANS, and LEC**

description

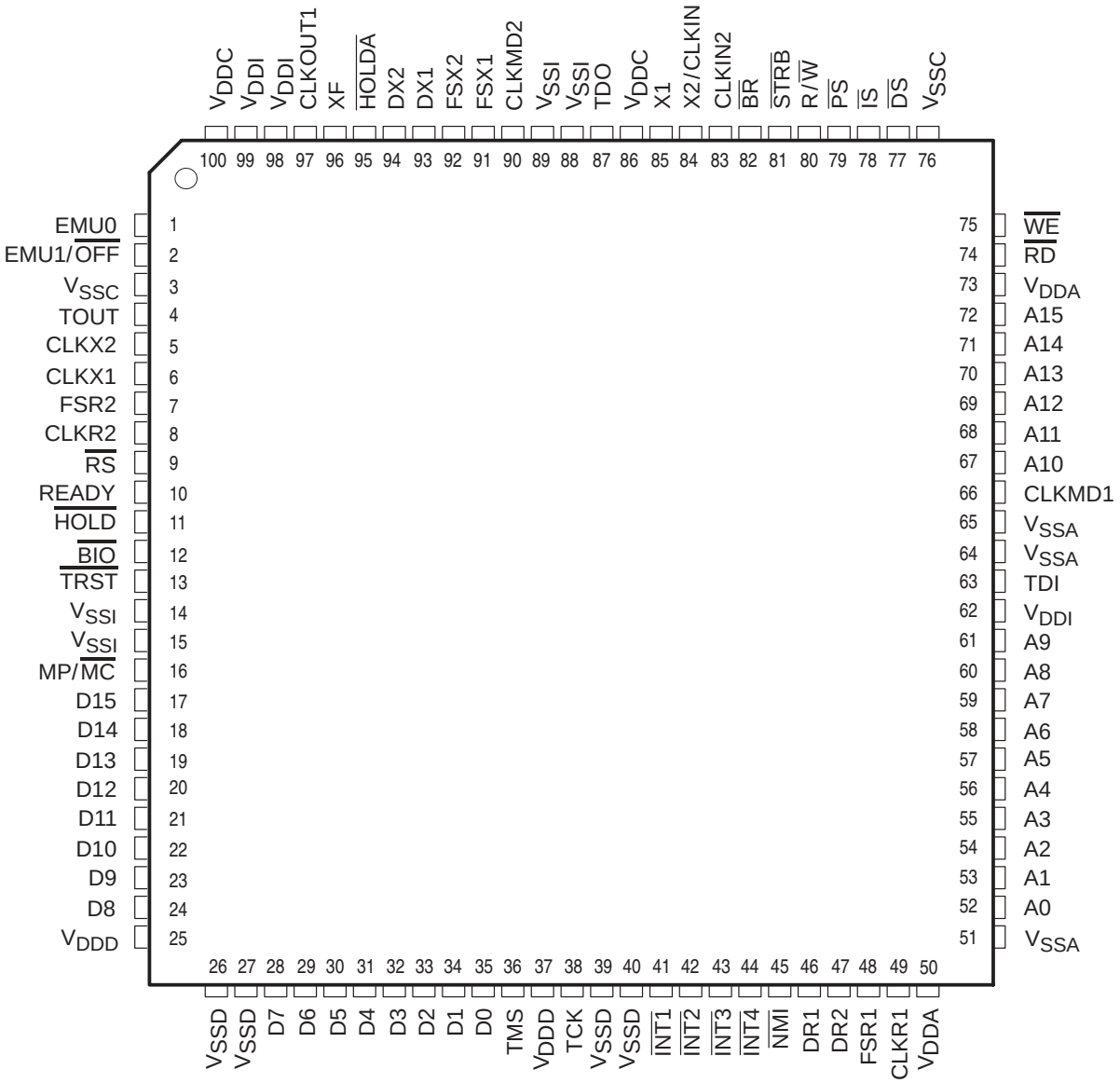
For the cellular phone cradle market, the TMS320WP010 provides enhanced quality, full-duplex, hands-free communications. The 'WP010 is a ROM-coded DSP that provides all the adaptive filtering and processing necessary for acoustic echo cancellation (AEC), line echo cancellation (LEC), and adaptive noise suppression (ANS).

The 'WP010's acoustic echo cancellation function is based on a Finite Impulse Response (FIR) filter with an adaptive coefficient updating algorithm. The adaptive algorithm updates continuously so that it can constantly track acoustic path changes from the speaker to the microphone. Based upon FIR filter coefficients, the echo signal can be estimated and subtracted from the observed signal at the microphone. The acoustic echo cancellation function provides continuous adaptation and needs no initial system training. It is capable of canceling an echo path of up to 44 milliseconds and provides up to 30 dB cancellation for speech signals. In addition, the initial convergence rate is faster than 20 dB per second.

The line echo cancellation function cancels the near-end speech that has been reflected at the network switch and transmitted back to the cellular phone. The principle of the line echo cancellation function is very similar to that of the acoustic echo cancellation function. The difference is that the line echo cancellation function is designed to cancel the echo signal caused by network feedback due to impedance mismatch in the network circuit. The line echo cancellation function is capable of canceling a line echo path of up to 16 milliseconds.

The received signal at the microphone consists of the near-end speech signal, acoustic feedback echo, and ambient noise from the environment. The purpose of the adaptive noise suppression function is to suppress ambient noise components without distorting near-end speech. The initial adaptation rate is about 3 dB per second without initial system training. It tracks the changes of the noise characteristics and suppresses noise accordingly. The adaptive noise suppression provides up to 10 dB of noise cancellation without degrading near-end speech.

TMS320WP010
PZ PACKAGE
(TOP VIEW)



Pin Functions for Devices in the PZ Package

SIGNAL	TYPE	DESCRIPTION
PARALLEL INTERFACE BUS		
A0–A15	I/O/Z	16-bit external address bus (MSB: A15, LSB: A0)
D0–D15	I/O/Z	16-bit external data bus (MSB: D15, LSB: D0)
$\overline{PS}$, $\overline{DS}$, $\overline{IS}$	O/Z	Program, data, and I/O space select outputs, respectively
$\overline{STRB}$	I/O/Z	Timing strobe for external cycles and external DMA
R/$\overline{W}$	I/O/Z	Read/write select for external cycles and external DMA
$\overline{RD}$, $\overline{WE}$	O/Z	Read and write strobes, respectively, for external cycles
READY	I	External bus ready/wait-state control input
$\overline{BR}$	I/O/Z	Bus request. Arbitrates global memory and external DMA
SYSTEM INTERFACE/CONTROL SIGNALS		
$\overline{RS}$	I	Reset. Initializes device and sets PC to zero
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. Enables internal ROM
$\overline{HOLD}$	I	Puts parallel I/F bus in high-impedance state after current cycle
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates external bus in hold state
XF	O/Z	External flag output. Set/cleared through software
$\overline{BIO}$	I	I/O branch input. Implements conditional branches
TOUT	O/Z	Timer output signal. Indicates output of internal timer
$\overline{INT1}$–$\overline{INT4}$	I	External interrupt inputs
$\overline{NMI}$	I	Nonmaskable external interrupt
SERIAL PORT INTERFACE		
DR1, DR2	I	Serial receive-data input
DX1, DX2	O/Z	Serial transmit-data output. In high-impedance state when not transmitting
CLKR1, CLKR2	I	Serial receive-data clock input
CLKX1, CLKX2	I/O/Z	Serial transmit-data clock. Internal or external source
FSR1, FSR2	I	Serial receive-frame-synchronization input
FSX1, FSX2	I/O/Z	Serial transmit-frame-synchronization signal. Internal or external source

LEGEND:
I = Input
O = Output
Z = High impedance

Pin Functions for Devices in the PZ Package (Continued)

SIGNAL	TYPE	DESCRIPTION
EMULATION/JTAG INTERFACE		
TDI	I	JTAG-test-port scan data input
TDO	O/Z	JTAG-test-port scan data output
TMS	I	JTAG-test-port mode select input
TCK	I	JTAG-port clock input
$\overline{\text{TRST}}$	I	JTAG-port reset (with pull-down resistor). Disables JTAG when low
EMU0	I/O/Z	Emulation control 0. Reserved for emulation use
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulation control 1. Puts outputs in high-impedance state when low
CLOCK GENERATION AND CONTROL		
X1	O	Oscillator output
X2/CLKIN	I	Clock/oscillator input
CLKIN2	I	Clock input
CLKMD1, CLKMD2	I	Clock-mode select inputs
CLKOUT1	I/O/Z	Device system-clock output
POWER SUPPLY CONNECTIONS		
V_{DDA}	S	Supply connection, address-bus output
V_{DDD}	S	Supply connection, data-bus output
V_{DDC}	S	Supply connection, control output
V_{DDI}	S	Supply connection, internal logic
V_{SSA}	S	Supply connection, address-bus output
V_{SSD}	S	Supply connection, data-bus output
V_{SSC}	S	Supply connection, control output
V_{SSI}	S	Supply connection, internal logic

LEGEND:
I = Input
O = Output
S = Supply
Z = High impedance

architecture

The 'WP010 architecture is based on the TMS320C5x Digital Signal Processor as shown in Figure 1. The 'WP010 sends/receives data through two serial ports available in the device. The first serial port (both RX1 and TX1) should be connected to the audio codec to interface with the phone line (in the cradle). The other serial port (RX2 and TX2) should be connected to the audio codec for the microphone and the speaker interfaces. The necessary software for the 'WP010 is ROM-coded and contained in ROM space. The 'WP010 also provides an MCU control interface to receive control commands from an MCU. The MCU control commands include the ability to reset the 'WP010 and to enable/disable some functions of the 'WP010.

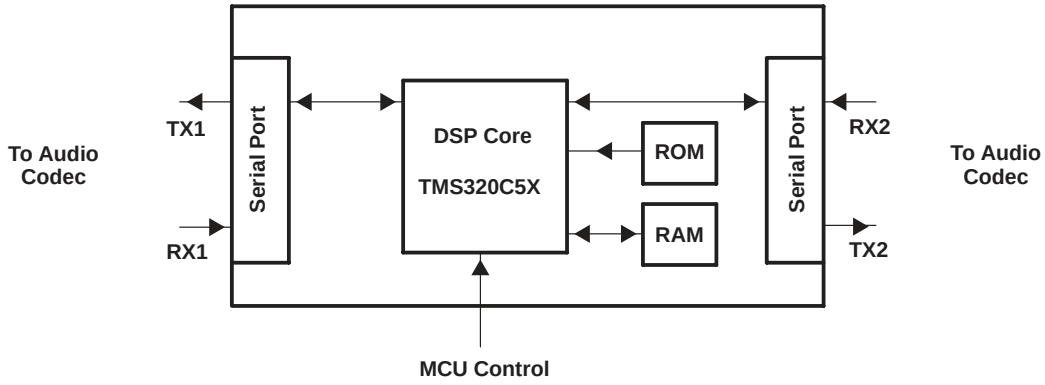


Figure 1. TMS320WP010 Architecture

functional description

The 'WP010 contains three main functional blocks: the adaptive line echo canceler, the adaptive acoustic echo canceler, and the adaptive noise suppressor. All three functions can be enabled or disabled by MCU control commands.

line echo canceler

The line echo canceler is to cancel the feedback line echo between two ports: RX1 and TX1. This function is performed by estimating the line echo path adaptively and subtracting it from the input signal. The line echo canceler cancels up to 16 milliseconds of line echo.

acoustic echo canceler

The purpose of the acoustic echo canceler (AEC) is to cancel the feedback acoustic echo from TX2 (interfaced with the speaker) to RX2 (interfaced with the microphone). The signal from the microphone (via RX2) is subtracted from the estimate of the acoustic echo path. The acoustic echo canceler is capable of canceling an echo up to 44 milliseconds long.

adaptive noise suppressor

The purpose of the adaptive noise suppressor (ANS) is to selectively suppress noise from the signal coming from the microphone (via RX2) without distorting near-end speech. Near-end speech is the desired speech signal of the user of the hands-free phone in a car. The adaptive noise suppressor tracks noise characteristics and suppresses accordingly. The ANS can suppress noise up to 10 dB.

development support

Texas Instruments offers a demonstration platform for the 'WP010. This platform contains all software modules including AEC, LEC, and ANS. There are switches that allow the algorithms to be turned on and off. The demonstration platform can be used in a lab or an automobile to fully evaluate the performance of the 'WP010.

device nomenclature

To designate the stages in the product development cycle, Texas Instruments assigns prefixes to the part numbers of all TMS320 devices. Each TMS320 member has one of three prefixes: TMX, TMP, or TMS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX) through fully qualified production devices/tools (TMS). This development flow is defined below.

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device

Predictions show that prototype devices (TMX or TMP) will have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate is still undefined. Only qualified production devices should be used.

TI™ device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, N, FN, or GB) and temperature range (for example, L). Figure 2 provides a legend for reading the complete device name for any TMS320WP family member.

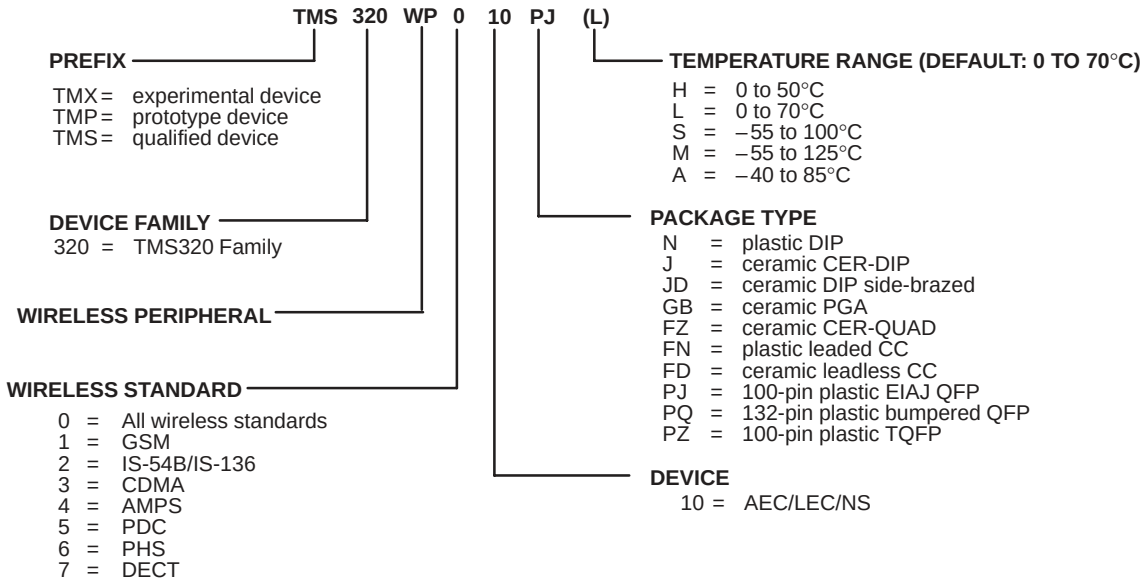


Figure 2. TMS320WP Device Nomenclature

documentation support

In addition to this data sheet, a product bulletin and demonstration platform user's guide are available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . – 0.3 V to 7 V
Input voltage range, V_I . . . . . – 0.3 V to 7 V
Output voltage range, V_O . . . . . – 0.3 V to 7 V
Operating ambient temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	X2/CLKIN, CLKIN2	3		V_{DD}+0.3	V
		CLKX1, CLKX2, CLKR1, CLKR2	2.5		V_{DD}+0.3	
		All others	2		V_{DD}+0.3	
V_{IL}	Low-level input voltage	X2/CLKIN, CLKIN2, CLKX1, CLKX2, CLKR1, CLKR2	– 0.3		0.7	V
		All others	– 0.3		0.8	
I_{OH}	High-level output current (see Note 2)				– 300	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		85	°C
T_A	Operating ambient temperature (industrial)		–40		85	°C

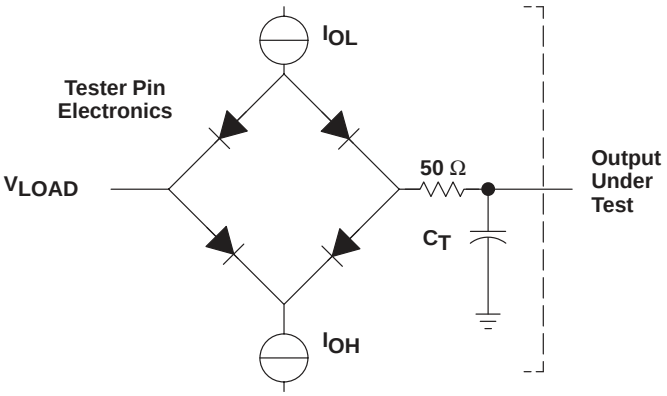
NOTE 2: Figure 3 shows the test load circuit and Figures 4 and 5 show the voltage reference levels.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage (see Note 2)	I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage (see Note 2)	I_{OL} = MAX		0.3	0.6	V
I_{OZ}	High-impedance output current (V_{DD} = MAX)	$\overline{BR}$ (with internal pull-up)	– 500		20	µA
		All others	– 20		20	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$ (with internal pull-down)	– 10		800	µA
		TMS, TCK, TDI (with internal pull-ups)	– 500		10	
		X2/CLKIN	– 50		50	
		All other inputs	– 10		10	
$I_{DD(core)}$	Supply current, core CPU	V_{DD} = 5.25 V		94		mA
$I_{DD(pins)}$	Supply current, pins	V_{DD} = 5.25 V		63		mA
$I_{DD(standby)}$	Supply current, standby	IDLE2, Clocks shut off		5		µA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† For conditions shown as MIN/MAX, use the appropriate value specified under “recommended operating conditions”.
‡ Typical values are at V_{DD} = 5 V, T_A = 25°C, unless otherwise specified.
NOTE 2: Figure 3 shows the test load circuit and Figures 4 and 5 show the voltage reference levels.

PARAMETER MEASUREMENT INFORMATION



Where:

I_{OL}	=	2 mA (all outputs) minimum
I_{OH}	=	300 μA (all outputs) minimum
V_{LOAD}	=	1.5 V
C_T	=	80-pF typical load circuit capacitance

Figure 3. Test Load Circuit

signal transition levels

TTL-output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Figure 4 shows the TTL-level outputs.

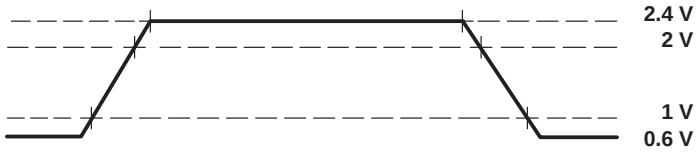


Figure 4. TTL-Level Outputs

TTL-output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is 2 V, and the level at which the output is said to be low is 1 V.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 1 V, and the level at which the output is said to be high is 2 V.

Figure 5 shows the TTL-level inputs.

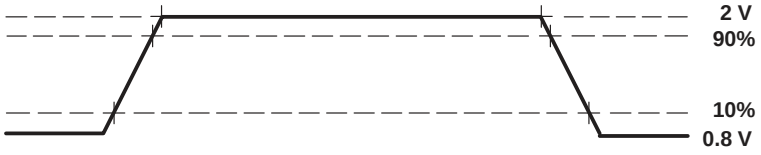


Figure 5. TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 2 V, and the level at which the input is said to be low is 0.8 V.
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 0.8 V, and the level at which the input is said to be high is 2 V.

CLOCK CHARACTERISTICS AND TIMING

The ’WP010 can use either its internal oscillator or an external frequency source for a clock. The clock mode is determined by the clock mode pins (CLKMD1 and CLKMD2). Table 1 shows the standard clock options available on the ’WP010.

Table 1. Standard Clock Options

CLKMD1	CLKMD2	CLOCK SOURCE
1	0	PLL clock generator option
0	1	Reserved for test purposes
1	1	External divide-by-two option or internal divide-by-two clock option with an external crystal
0	0	External divide-by-two option with the internal oscillator disabled

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT1 is one-half the crystal’s oscillating frequency. The crystal should be in either fundamental or overtone operation and parallel resonant, with an effective series resistance of 30 ohms and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF. Note that overtone crystals require an additional tuned-LC circuit. Figure 6 shows an external crystal (fundamental frequency) connected to the on-chip oscillator.

recommended operating conditions for internal divide-by-two clock option

		MIN	NOM	MAX	UNIT
f_{clk}	Input clock frequency	0†		80	MHz
C1, C2	Load capacitance		10		pF

† This device utilizes a fully static design and, therefore, can operate with input clock cycle time ($t_{c(CI)}$) approaching infinity. The device is characterized at frequencies approaching 0 Hz, but is tested at f_{clk} = 6.7 MHz to meet device test time requirements.

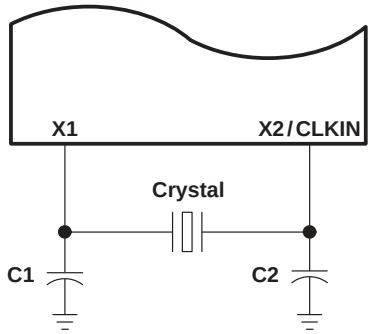


Figure 6. Internal Clock Option

external divide-by-two clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected, CLKMD1 set low, and CLKMD2 set low. This external frequency is divided by two to generate the internal machine cycle. The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] (see Figure 7)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	25	$2t_{c(CI)}$	†	ns
$t_{d(CIH-COH/L)}$	Delay time, X2/CLKIN high to CLKOUT1 high/low	1	9	18	ns
$t_{f(CO)}$	Fall time, CLKOUT1		4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3	H	H + 2	ns

† This device utilizes a fully static design and, therefore, can operate with $t_{c(CO)}$ approaching infinity. The device is characterized at frequencies approaching 0 Hz but is tested at $t_{c(CO)}$ = 300 ns to meet device test time requirements

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 7)

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, X2/CLKIN	12.5	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN‡		4	ns
$t_{r(CI)}$	Rise time, X2/CLKIN‡		4	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	5	†	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	5	†	ns

† This device utilizes a fully static design and, therefore, can operate with $t_{c(CI)}$ approaching infinity. The device is characterized at frequencies approaching 0 Hz, but is tested at a minimum of $t_{c(CI)}$ = 150 ns to meet device test time requirements.
‡ Values derived from characterization data and not tested

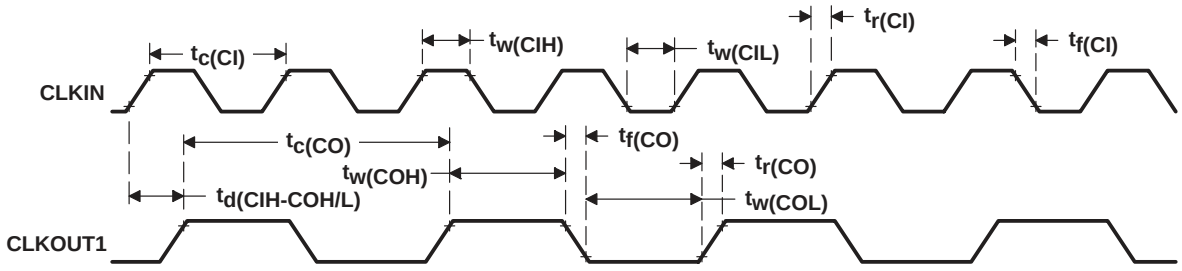


Figure 7. External Divide-by-Two Clock Timing

PLL clock generator option

An external frequency source can be used by injecting the frequency directly into CLKIN2 with X1 left unconnected and X2 connected to V_{DD}. This external frequency is multiplied by one or by two to generate the internal machine cycle. The multiply-by-one option is available on the 'WP010. The PLL clock generator option is used when CLKMD1 is strapped high and CLKMD2 is strapped low. The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$] (see Figure 8)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	25		55	ns
$t_{f(CO)}$	Fall time, CLKOUT1		4		ns
$t_{r(CO)}$	Rise time, CLKOUT1		4		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low	H – 3†	H	H + 2†	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high	H – 3†	H	H + 2†	ns
$t_{d(C2H-COH)}$	Delay time, CLKIN2 high to CLKOUT1 high	1	8	15	ns
$t_{d(TP)}$	Delay time, transitory phase—PLL synchronized after CLKIN2 supplied†			$1000t_{c(C2)}$	ns

† Values assured by design and not tested

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 8)

			MIN	MAX	UNIT
$t_{c(C2)}$	Cycle time, CLKIN2	Multiply by one	25	75†	ns
		Multiply by two	50	150†	ns
$t_{f(C2)}$	Fall time, CLKIN2‡			4	ns
$t_{r(C2)}$	Rise time, CLKIN2‡			4	ns
$t_{w(C2L)}$	Pulse duration, CLKIN2 low		8	$t_{c(C2)}-8$	ns
$t_{w(C2H)}$	Pulse duration, CLKIN2 high		8	$t_{c(C2)}-8$	ns

† Clocks may only be stopped while executing IDLE2 when using the PLL clock generator option. Note that $t_{d(TP)}$ (the transitory phase) will occur when restarting clock from IDLE2 in this mode.

‡ Values derived from characterization data and not tested

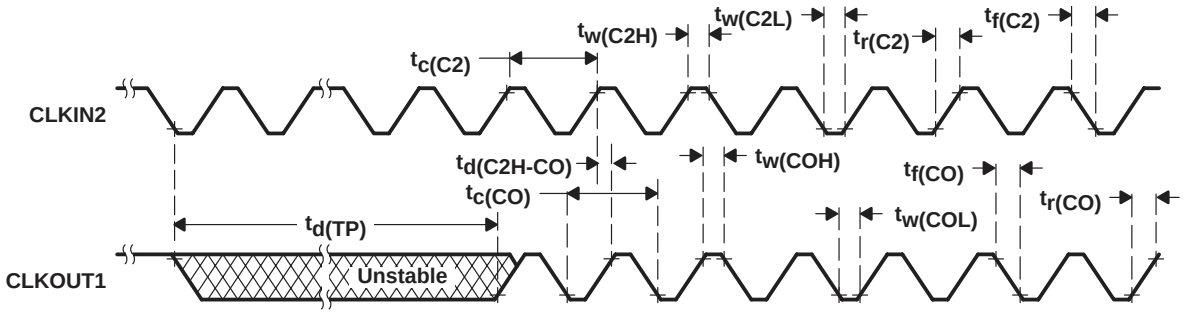


Figure 8. PLL Clock Generator Timing

RESET AND INTERRUPT

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 9)

		MIN	MAX	UNIT
$t_{su(IN-COL)}$	Setup time, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ before CLKOUT1 low †	10		ns
$t_{su(RS-COL)}$	Setup time, $\overline{RS}$ before CLKOUT1 low	10	2H – 5‡	ns
$t_{su(RS-X2L)}$	Setup time, $\overline{RS}$ before X2/CLKIN low	7		ns
$t_{h(COL-IN)}$	Hold time, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ after CLKOUT1 low †	0		ns
$t_{w(INL)SYN}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ low, synchronous	4H + 10§		ns
$t_{w(INH)SYN}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ high, synchronous	2H + 10§		ns
$t_{w(INL)ASY}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ low, asynchronous ‡	6H + 10§		ns
$t_{w(INH)ASY}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ high, asynchronous ‡	4H + 10§		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low	12H		ns
$t_{d(RSH)}$	Delay time, $\overline{RS}$ high to reset vector fetch	34H		ns

† These parameters must be met to use the synchronous timings. Both reset and the interrupts can operate asynchronously. The pulse durations require an extra half-cycle to ensure internal synchronization.
‡ Values derived from characterization data and not tested
§ If in IDLE2, add 4H to these timings.

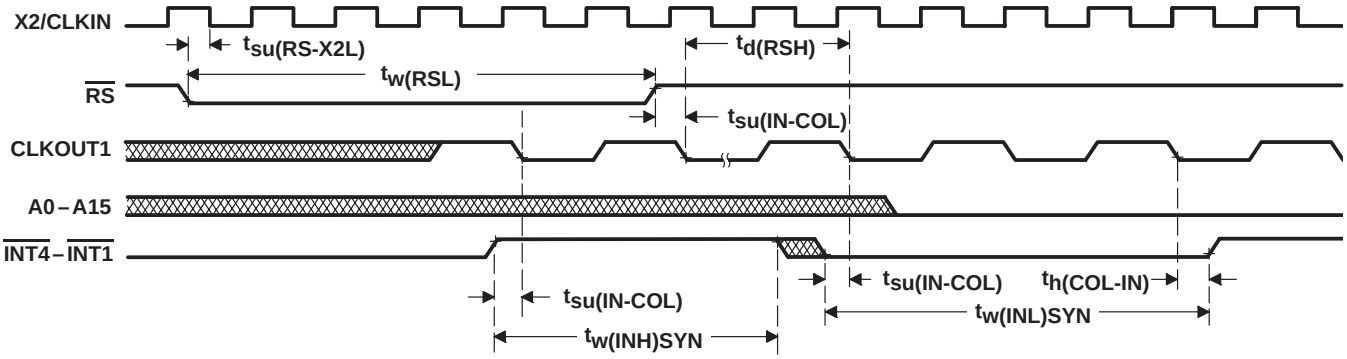


Figure 9. Reset and Interrupt Timing

SERIAL-PORT RECEIVE

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Figure 10)

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H†	‡	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6§	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6§	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H†		ns
$t_{su(FS-CK)}$	Setup time, FSR1 (FSR2) before CLKR1 (CLKR2) falling edge	7		ns
$t_{su(DR-CK)}$	Setup time, DR1 (DR2) before CLKR1 (CLKR2) falling edge	7		ns
$t_{h(CK-FS)}$	Hold time, FSR1 (FSR2) after CLKR1 (CLKR2) falling edge	7		ns
$t_{h(CK-DR)}$	Hold time, DR1 (DR2) after CLKR1 (CLKR2) falling edge	7		ns

† Values ensured by design but not tested
‡ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
§ Values derived from characterization data and not tested

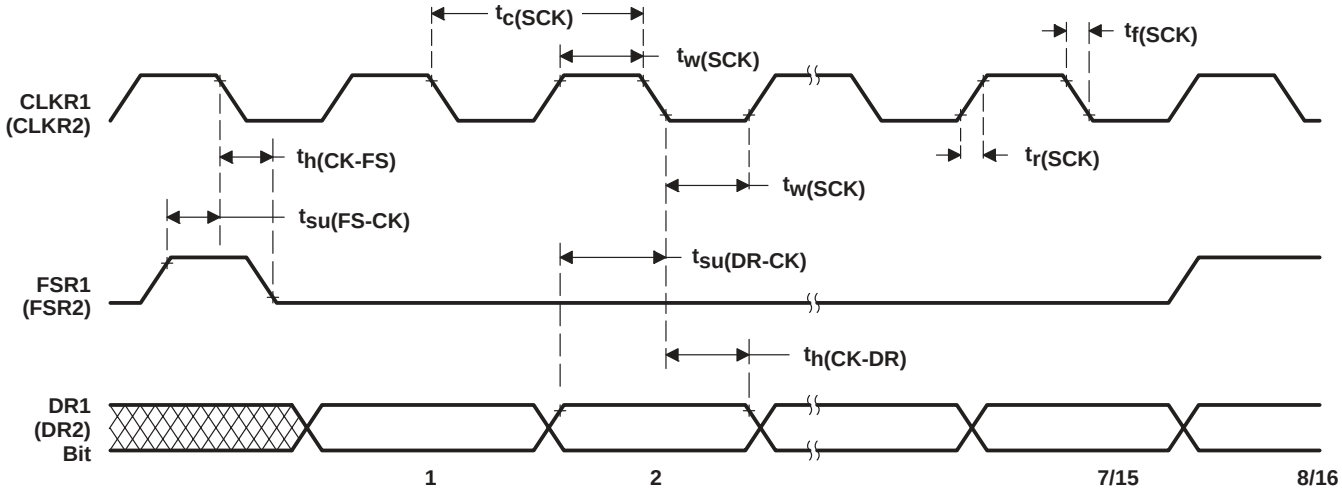


Figure 10. Serial-Port Receive Timing

SERIAL-PORT TRANSMIT, EXTERNAL CLOCKS, AND EXTERNAL FRAMES

switching characteristics over recommended operating conditions (see Note 3) (see Figure 11)

PARAMETER		MIN	MAX	UNIT
$t_{d(CXH-DXV)}$	Delay time, DX1 (DX2) valid after CLKX1 (CLKX2) high		25	ns
$t_{dis(CXH-DX)}$	Disable time, DX1 (DX2) invalid after CLKX1 (CLKX2) high		40†	ns
$t_{h(CXH-DXV)}$	Hold time, DX1 (DX2) valid after CLKX1 (CLKX2) high	– 5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$] (see Note 3) (see Figure 11)

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H‡	§	ns
$t_{f(SCK)}$	Fall time, serial-port clock		6†	ns
$t_{r(SCK)}$	Rise time, serial-port clock		6†	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H‡		ns
$t_{d(CXH-FXH)}$	Delay time, FSX1 (FSX2) high after CLKX1 (CLKX2) high		2H – 8	ns
$t_{h(CXL-FXL)}$	Hold time, FSX1 (FSX2) low after CLKX1 (CLKX2) low	7		ns
$t_{h(CXH-FXL)}$	Hold time, FSX1 (FSX2) low after CLKX1 (CLKX2) high		2H – 8¶	ns

† Values derived from characterization data and not tested
‡ Values ensured by design but not tested
§ The serial-port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching infinity. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
¶ If the FSX1 (FSX2) pulse does not meet this specification, the first bit of serial data will be driven on the DX1 (DX2) pin until the falling edge of FSX1 (FSX2). After the falling edge of FSX1 (FSX2), data will be shifted out on the DX1 (DX2) pin. The transmit buffer empty interrupt will be generated when the $t_{h(CXL-FXL)}$ and $t_{h(CXH-FXL)}$ specification is met.

NOTE 3: Internal clock with external FSX1 (FSX2) and vice versa are also allowable. However, FSX1 (FSX2) timings to CLKX1 (CLKX2) are always defined depending on the source of FSX1 (FSX2), and CLKX1 (CLKX2) timings are always dependent upon the source of CLKX1 (CLKX2). Specifically, the relationship of FSX1 (FSX2) to CLKX1 (CLKX2) is independent of the source of CLKX1 (CLKX2).

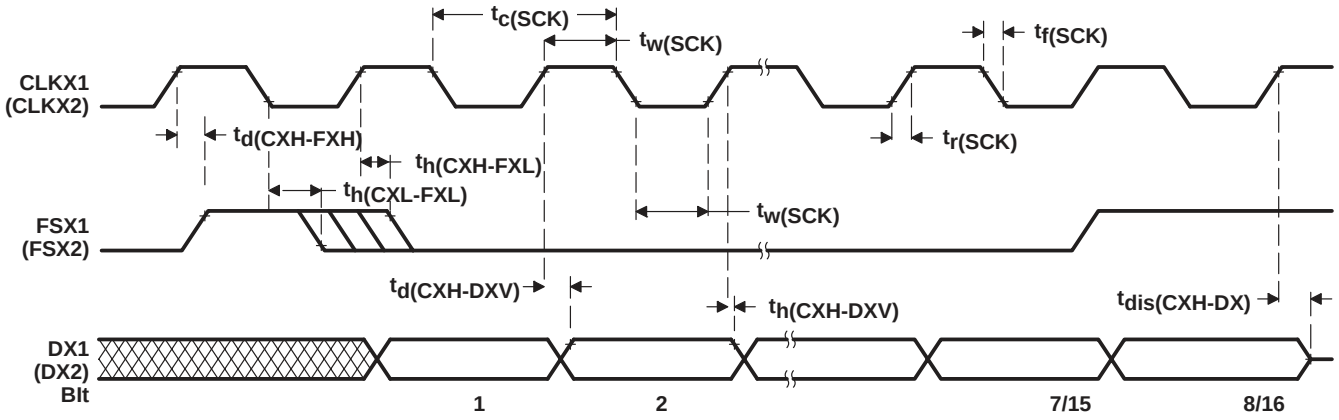


Figure 11. Serial-Port Transmit Timing of External Clocks and External Frames

SERIAL-PORT TRANSMIT, INTERNAL CLOCKS, AND INTERNAL FRAMES (SEE NOTE 3)

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Figure 12)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CX-FX)}$	Delay time, CLKX1 (CLKX2) rising edge to FSX1 (FSX2)	– 4		18	ns
$t_{d(CX-DX)}$	Delay time, CLKX1 (CLKX2) rising edge to DX1 (DX2)			18	ns
$t_{dis(CX-DX)}$	Disable time, CLKX1 (CLKX2) rising edge to DX1 (DX2)			29†	ns
$t_{c(SCK)}$	Cycle time, serial-port clock		8H		ns
$t_{f(SCK)}$	Fall time, serial-port clock		4		ns
$t_{r(SCK)}$	Rise time, serial-port clock		4		ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	4H – 14			ns
$t_{h(CXH-DXV)}$	Hold time, DX1 (DX2) valid after CLKX1 (CLKX2) high	– 4			ns

† Values derived from characterization data and not tested

NOTE 3: Internal clock with external FSX1 (FSX2) and vice versa are also allowable. However, FSX1 (FSX2) timings to CLKX1 (CLKX2) are always defined depending on the source of FSX1 (FSX2), and CLKX1 (CLKX2) timings are always dependent upon the source of CLKX1 (CLKX2). Specifically, the relationship of FSX1 (FSK2) to CLKX1 (CLKX2) is independent of the source of CLKX1 (CLKX2).

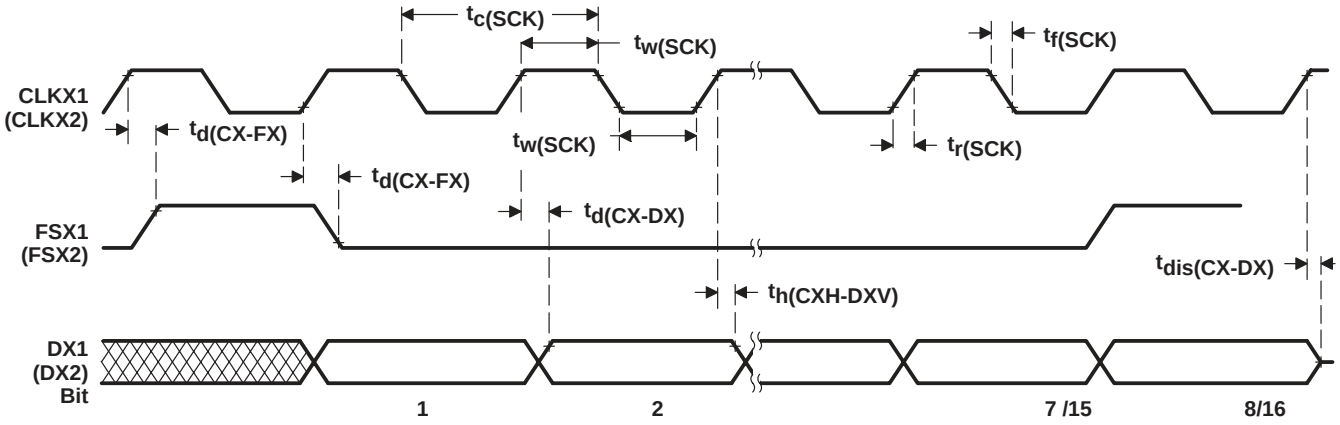
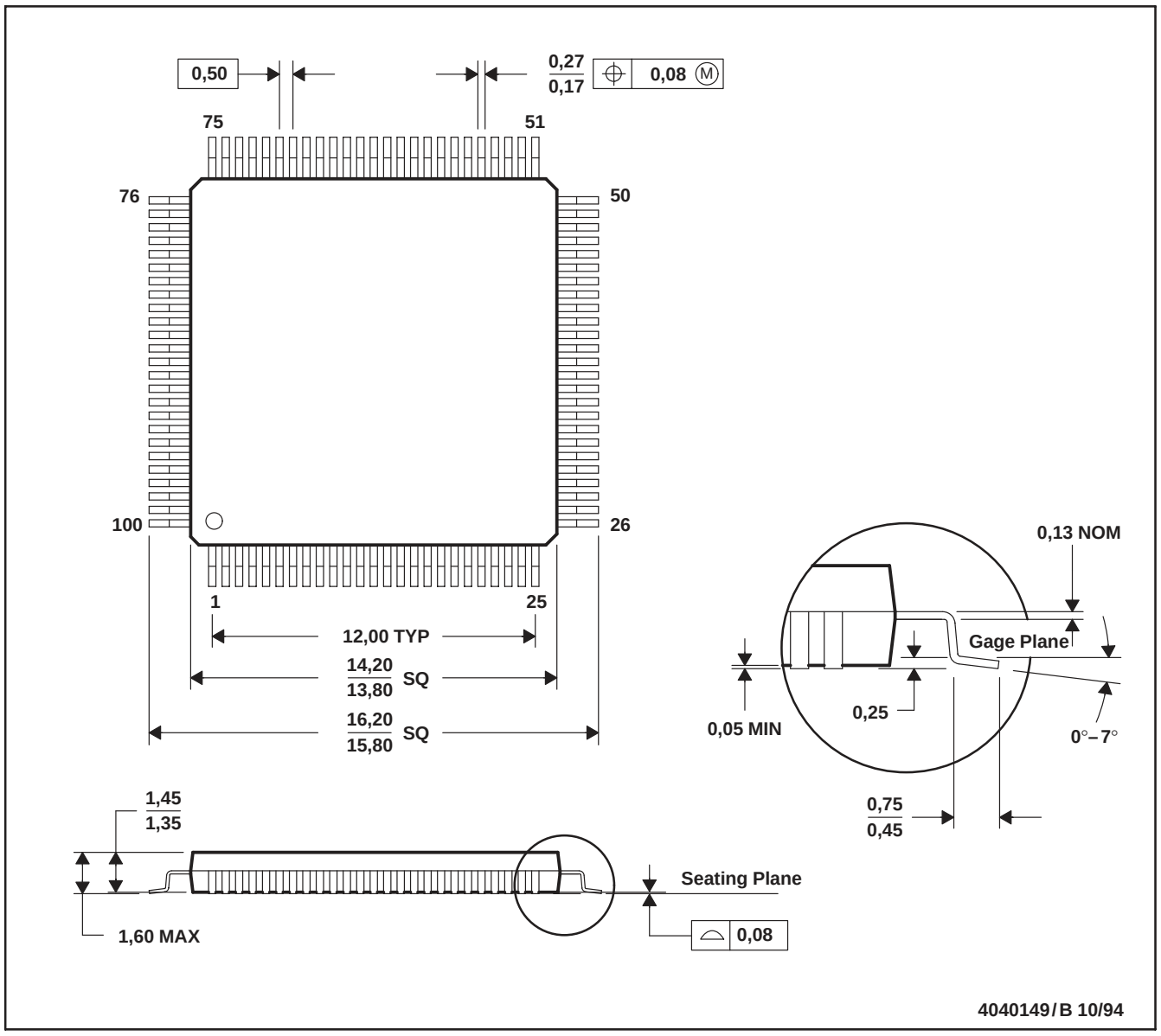


Figure 12. Serial-Port Transmit Timing of Internal Clocks and Internal Frames

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMS320WP010PZ	OBSOLETE	LQFP	PZ	100		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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