PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017 (83940DKILF)

General Description

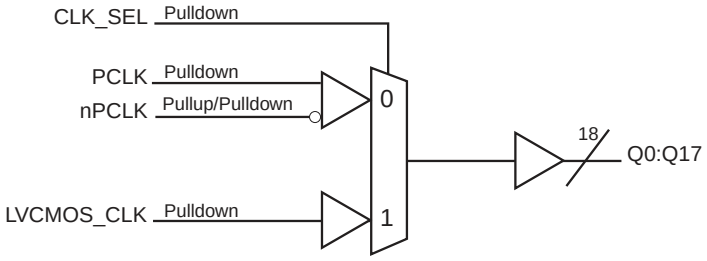
The ICS83940DI is a low skew, 1 to 18 LVPECL to LVCMOS/LVTTL fanout buffer. The ICS83940DI has two selectable clock inputs. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The LVCMOS_CLK can accept LVCMOS or LVTTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

The ICS83940DI is characterized at full 3.3V and 2.5V or mixed 3.3V core, 2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS83940DI ideal for those clock distribution applications demanding well defined performance and repeatability.

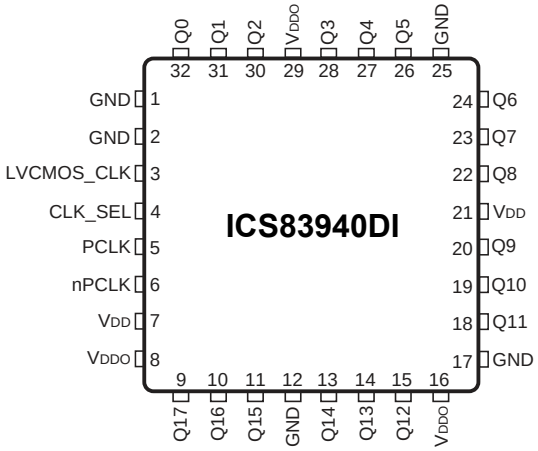
Features

- Eighteen LVCMOS/LVTTL outputs
- Selectable LVCMOS_CLK or LVPECL clock inputs
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- LVCMOS_CLK supports the following input types: LVCMOS or LVTTL
- Maximum output frequency: 250MHz
- Output skew: 150ps (maximum)
- Part-to-part skew: 750ps (maximum)
- Operating supply modes:
- Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging
- For functional replacement part for 83940DKILF, use 87016i

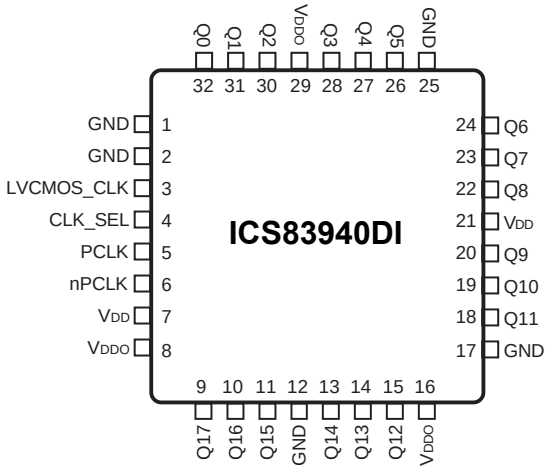
Block Diagram



Pin Assignments



32 Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 12, 17, 25	GND	Power		Power supply ground.
3	LVCMOS_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
4	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects LVCMOS_CLK input. When LOW, selects PCLK, nPCLK inputs. LVCMOS / LVTTL interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{DD}/2$ default when left floating.
7, 21	V_{DD}	Power		Power supply pin.
8, 16, 29	V_{DDO}	Power		Output supply pins.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q17, Q16, Q15, Q14, Q13, Q12, Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			6		pF
R_{OUT}	Output Impedance		18		28	Ω

Function Tables

Table 3A. Clock Select Function Table

Control Input	Clock	
CLK_SEL	**PCLK, nPCLK**	**LVCMOS_CLK**
0	Selected	De-selected
1	De-selected	Selected

Table 3B. Clock Input Function Table

Inputs				Outputs		
CLK_SEL	**LVCMOS_CLK**	**PCLK**	**nPCLK**	**Q[0:17]**	**Input to Output Mode**	**Polarity**
0	–	0	1	LOW	Differential to Single-Ended	Non-Inverting
0	–	1	0	HIGH	Differential to Single-Ended	Non-Inverting
0	–	0	Biased; NOTE 1	LOW	Single-Ended to Single-Ended	Non-Inverting
0	–	1	Biased; NOTE 1	HIGH	Single-Ended to Single-Ended	Non-Inverting
0	–	Biased; NOTE 1	0	HIGH	Single-Ended to Single-Ended	Inverting
0	–	Biased; NOTE 1	1	LOW	Single-Ended to Single-Ended	Inverting
1	0	–	–	LOW	Single-Ended to Single-Ended	Non-Inverting
1	1	–	–	HIGH	Single-Ended to Single-Ended	Non-Inverting

NOTE 1: Please refer to the Application Information Section, *Wiring the Differential Input to Accept Single-ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I	-0.3V to V_{DD} + 0.3V
Outputs, V_O	-0.3V to V_{DDO} + 0.3V
Input Current, I_{IN}	±20mA
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. DC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2.4		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.5	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1	PCLK, nPCLK		500		1000	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	PCLK, nPCLK		V_{DD} – 1.45		V_{DD} – 0.6	V
I_{DD}	Power Supply Current					25	mA

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 4B. DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2.4		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	1.8			V
V_{OL}	Output Low Voltage		I_{OL} = 20mA			0.5	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1	PCLK, nPCLK		300		1000	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	PCLK, nPCLK		V_{DD} – 1.4		V_{DD} – 0.6	V
I_{DD}	Power Supply Current					25	mA

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 4C. DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	LVCMOS_CLK		2		V_{DD}	V
V_{IL}	Input Low Voltage	LVCMOS_CLK				0.8	V
I_{IN}	Input Current					±200	µA
V_{OH}	Output High Voltage		I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage		I_{OL} = 12mA			0.5	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1	PCLK, nPCLK		300		1000	mV
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2	PCLK, nPCLK		V_{DD} – 1.4		V_{DD} – 0.6	V
I_{DD}	Power Supply Current					25	mA

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150$MHz	1.6		3.0	ns
		LVCMOS_CLK; NOTE 2, 5	$f \leq 150$MHz	1.8		3.0	ns
	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150$MHz	1.6		3.3	ns
		LVCMOS_CLK; NOTE 2, 5	$f > 150$MHz	1.8		3.2	ns
*t*sk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on the Rising Edge at $V_{DDO}/2$			150	ps
		LVCMOS_CLK				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150$MHz			1.4	ns
		LVCMOS_CLK	$f \leq 150$MHz			1.2	ns
	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150$MHz			1.7	ns
		LVCMOS_CLK	$f > 150$MHz			1.4	ns
	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on the Rising Edge at $V_{DDO}/2$			850	ps
		LVCMOS_CLK				750	ps
t_R / t_F	Output Rise/Fall Time		0.5V to 2.4V	0.3		1.1	ns
odc	Output Duty Cycle		$f < 134$MHz	45	50	55	%
			$134\text{MHz} \leq f \leq 250\text{MHz}$	40	50	60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output $V_{DDO}/2$.
NOTE 2: Measured from $V_{DD}/2$ to $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

Table 5B. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq$ 150MHz	1.7		3.2	ns
		LVCMOS_CLK; NOTE 2, 5	$f \leq$ 150MHz	1.7		3.0	ns
	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f >$ 150MHz	1.6		3.4	ns
		LVCMOS_CLK; NOTE 2, 5	$f >$ 150MHz	1.8		3.3	ns
*t*sk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on the Rising Edge at V_{DDO}/2			150	ps
		LVCMOS_CLK				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq$ 150MHz			1.5	ns
		LVCMOS_CLK	$f \leq$ 150MHz			1.3	ns
	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f >$ 150MHz			1.8	ns
		LVCMOS_CLK	$f >$ 150MHz			1.5	ns
	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on the Rising Edge at V_{DDO}/2			850	ps
		LVCMOS_CLK				750	ps
t_R / t_F	Output Rise/Fall Time		0.5V to 1.8V	0.3		1.2	ns

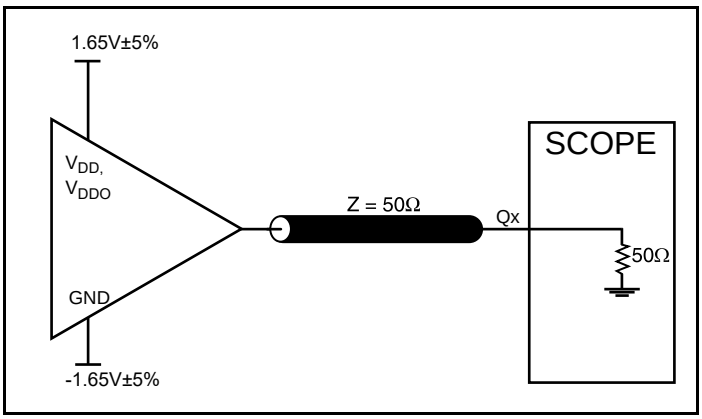
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output V_{DDO}/2.
NOTE 2: Measured from V_{DD}/2 to V_{DDO}/2.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.

Table 5C. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

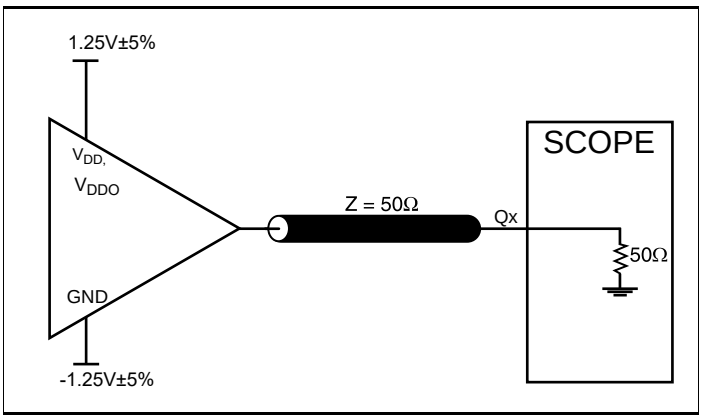
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					200	MHz
t_{PLH}	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f \leq 150$MHz	1.2		3.8	ns
		LVCMOS_CLK; NOTE 2, 5	$f \leq 150$MHz	1.5		3.2	ns
	Propagation Delay	PCLK, nPCLK; NOTE 1, 5	$f > 150$MHz	1.5		3.7	ns
		LVCMOS_CLK; NOTE 2, 5	$f > 150$MHz	2.0		3.6	ns
*t*sk(o)	Output Skew; NOTE 3, 5	PCLK, nPCLK	Measured on the Rising Edge at $V_{DDO}/2$			200	ps
		LVCMOS_CLK				200	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f \leq 150$MHz			2.6	ns
		LVCMOS_CLK	$f \leq 150$MHz			1.7	ns
	Part-to-Part Skew; NOTE 6	PCLK, nPCLK	$f > 150$MHz			2.2	ns
		LVCMOS_CLK	$f > 150$MHz			1.7	ns
	Part-to-Part Skew; NOTE 4, 5	PCLK, nPCLK	Measured on the Rising Edge at $V_{DDO}/2$			1.2	ns
		LVCMOS_CLK				1.0	ns
t_R / t_F	Output Rise/Fall Time		0.5V to 1.8V	0.3		1.2	ns
odc	Output Duty Cycle		$f < 166$MHz	40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 200MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output $V_{DDO}/2$.
NOTE 2: Measured from $V_{DD}/2$ to $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Defined as skew between outputs on different devices, across temperature and voltage ranges, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

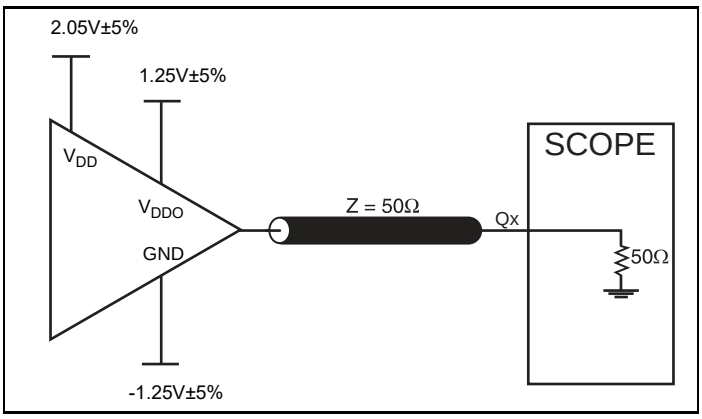
Parameter Measurement Information



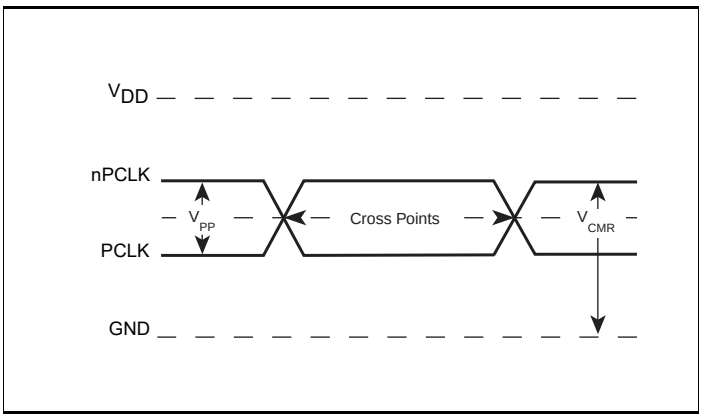
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



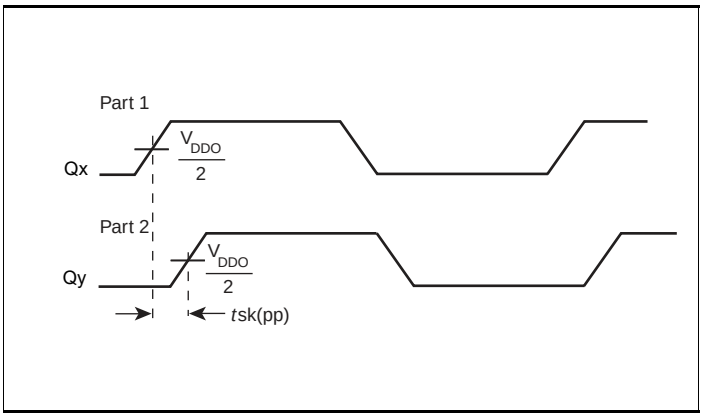
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



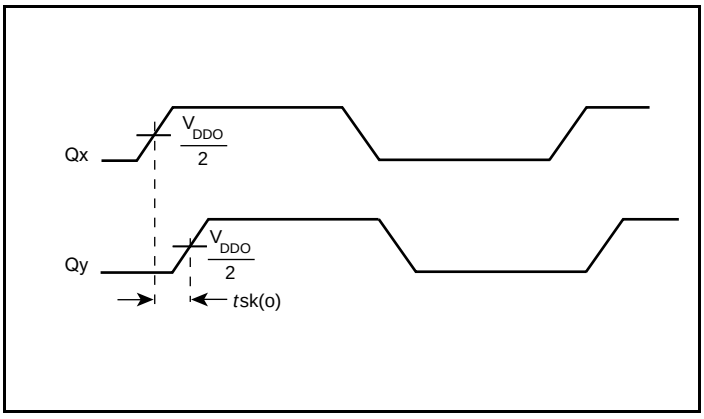
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



Differential Input Level

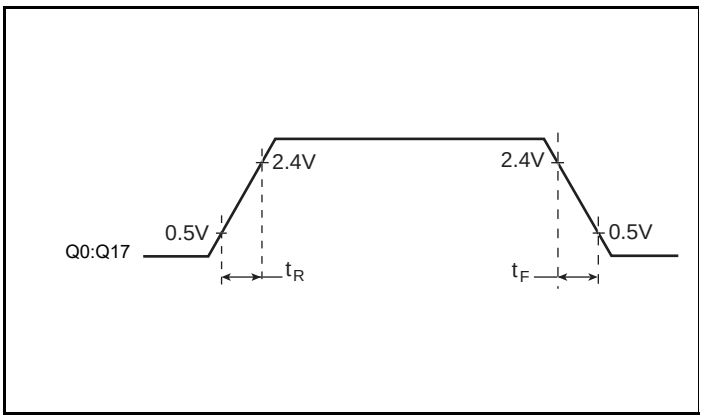


Part-to-Part Skew

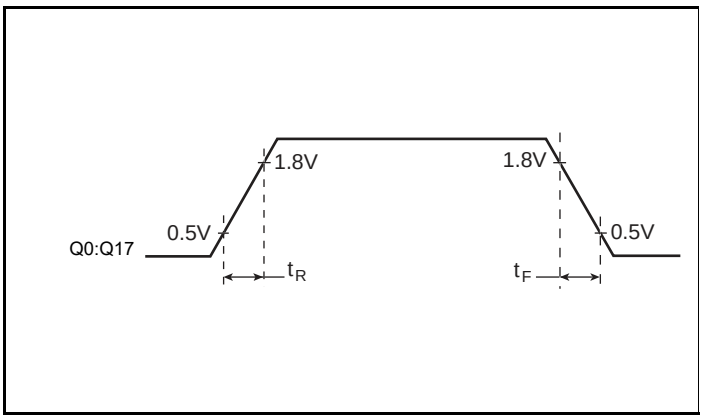


Output Skew

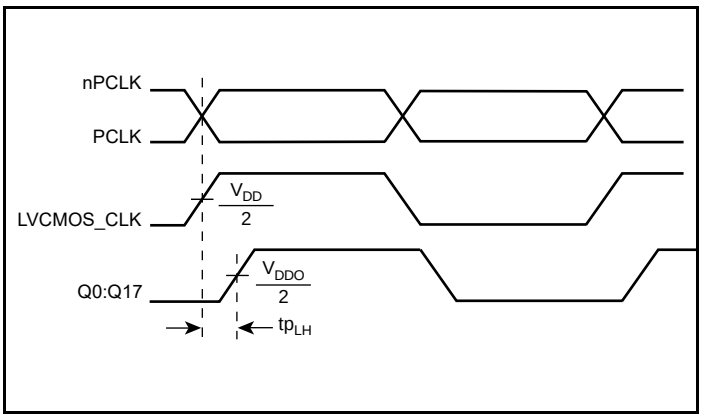
Parameter Measurement Information, continued



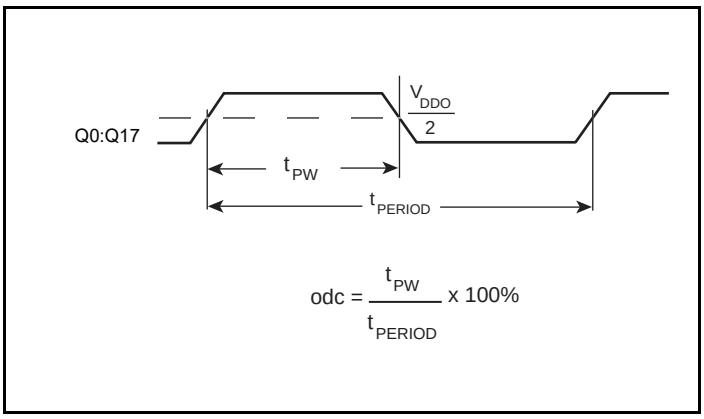
3.3V Output Rise/Fall Time



2.5V Output Rise/Fall Time



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

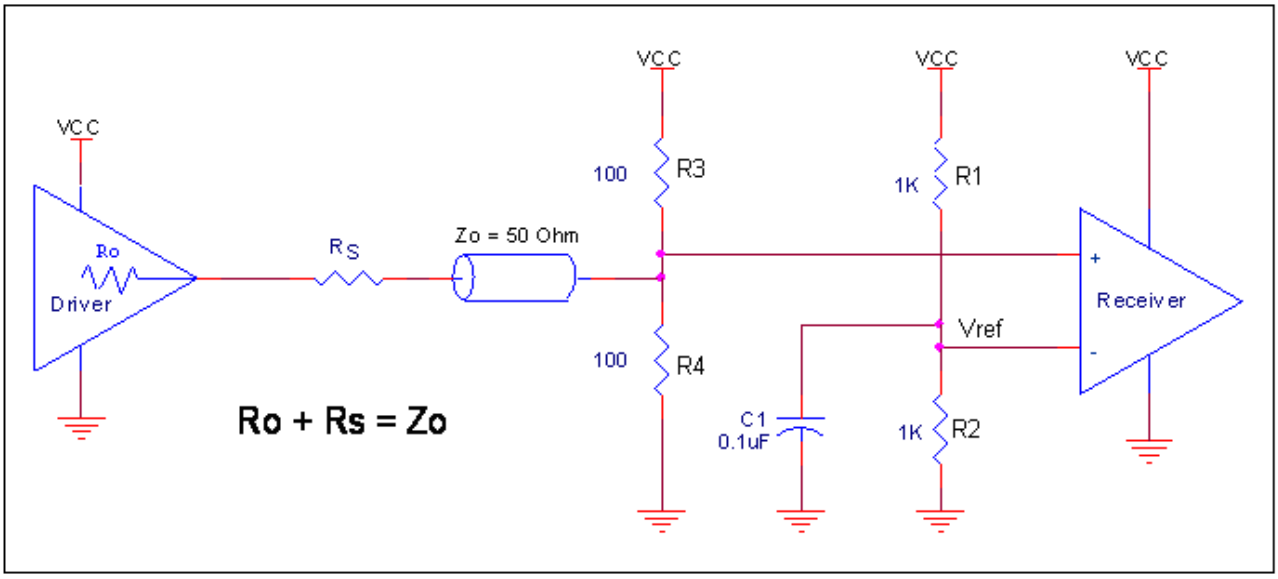


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

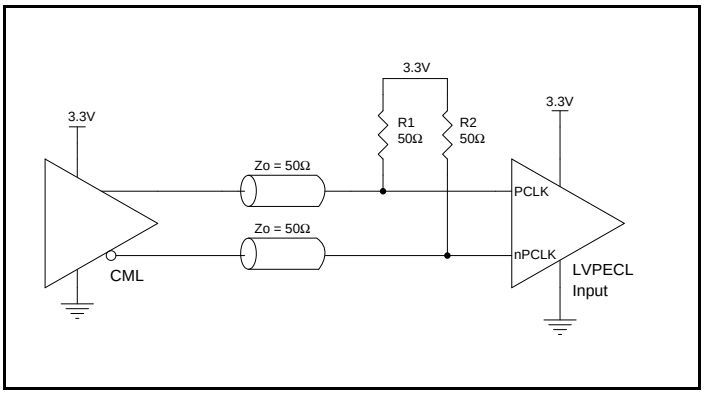


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

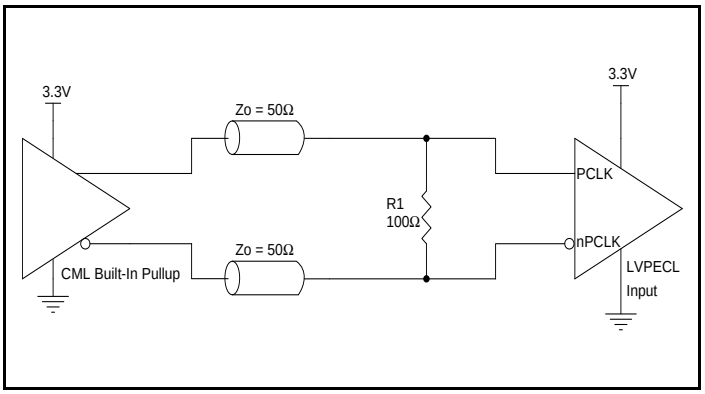


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

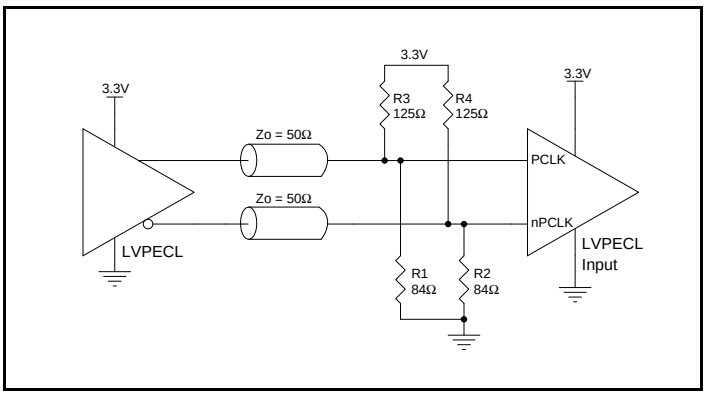


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

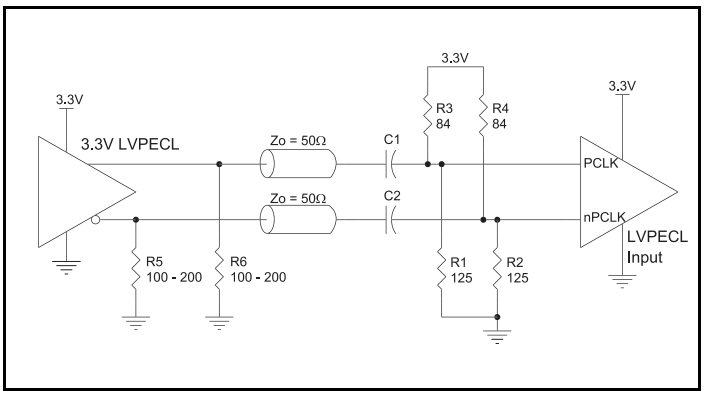


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

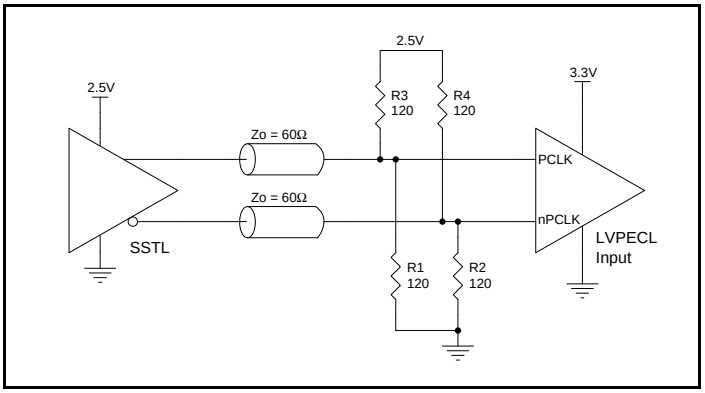


Figure 2E. PCLK/nPCLK Input Driven by an SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

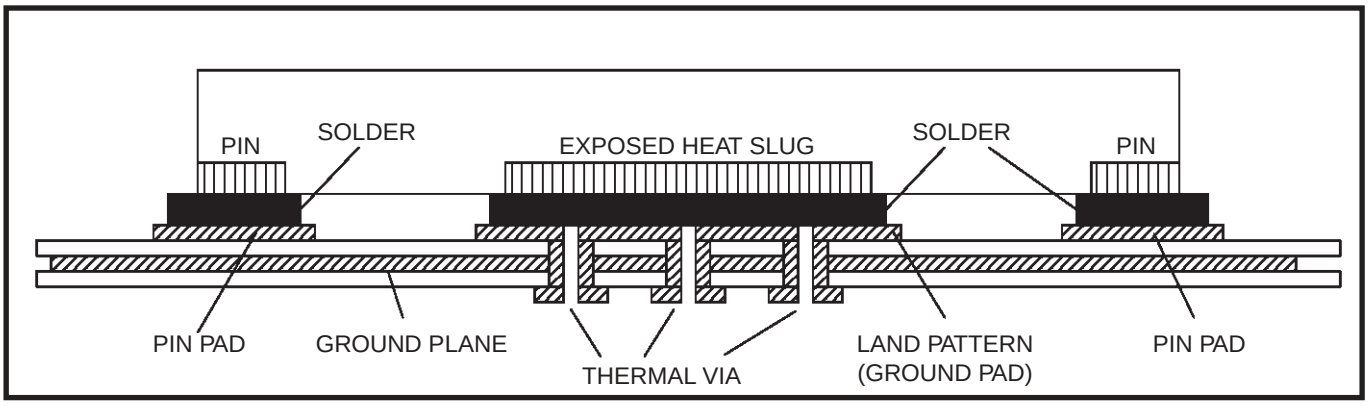


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVCMOS_CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the LVCMOS_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6A. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

Table 6B. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	40.2°C/W	35.1°C/W	31.5°C/W

Transistor Count

The transistor count for ICS83940DI is: 820

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/prg32-package-outline-70-x-70-mm-lqfp

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83940DYILF	ICS83940DYIL	“Lead-Free” 32 Lead LQFP	Tray	-40°C to 85°C
83940DYILFT	ICS83940DYIL	“Lead-Free” 32 Lead LQFP	Tape & Reel	-40°C to 85°C

Revision History

Date	Description
January 7, 2020	▪ Removed Output Duty Cycle specification from table 5B. ▪ Updated Output Duty Cycle specifications in table 5C. ▪ Removed 83940DKILF/T devices from Ordering Information table. ▪ Updated Package Outline Drawings section. ▪ Rebranded document to Renesas template.
May 19, 2016	Product Discontinuation Notice - Last time buy expires May 6, 2017. (83940DKILF) PDN CQ-16-01.
March 20, 2013	Deleted “PROPOSED” stamp.
November 27, 2012	Removed leaded orderables from Ordering Information table.
September 7, 2010	Pin Characteristics Table - R_{OUT} error, typical spec deleted. Updated Wiring the Differential Input to Accept Single-Ended Levels. Updated 32 VFQFN Package Outline.
August 13, 2009	Added 32 Lead VFQFN Pin Assignment. Added *VFQFN Thermal Release Path* section. Added 32 VFQFN Thermal Table. Added 32 Lead VFQFN Package and Dimensions Table. Ordering Information Table - added 32 Lead VFQFN ordering information. Converted datasheet format.
February 21, 2007	Absolute Maximum Ratings - corrected Storage Temperature from “-40°C to 125°C” to “-65°C to 150°C”.
November 27, 2006	Features Section - added Lead-Free bullet. Application Information Section - added Recommendations for Unused Input and Output Pins. Application Information Section - added LVPECL Clock Input Interface. Ordering Information Table - added Lead-Free part number, marking, and note. Updated datasheet format.
December 12, 2002	Pin Characteristics table - changed R_{OUT} 25Ω maximum to 28Ω maximum. Delete R_{PULLUP} row. 3.3V Output Load AC Test Circuit diagram - corrected GND equation to read -1.65V... from -1.165V... Added LVTTL to title. Updated format.

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32-LQFP, Package Outline Drawing

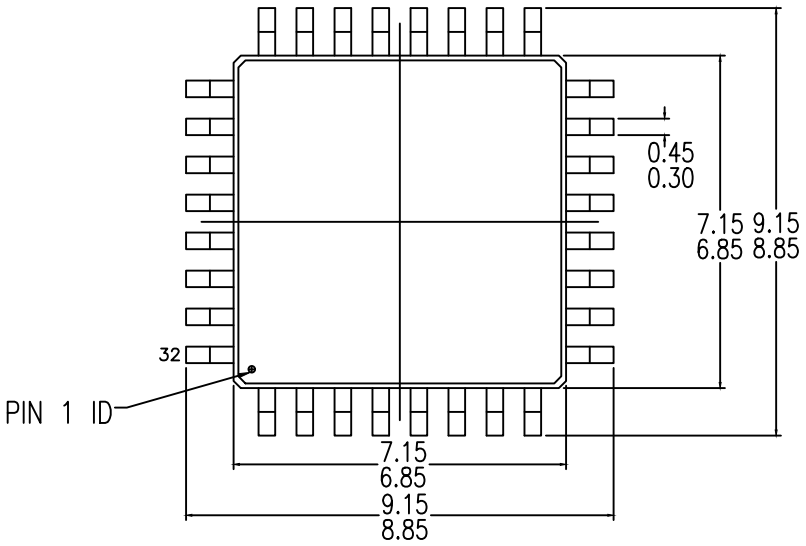
7.0 x 7.0 x 1.4 mm Body, 1.0/.10 Form

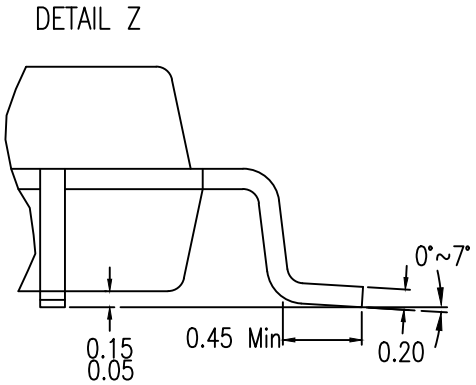
PRG32D1, PSC-4052-01, Rev 01, Page 1

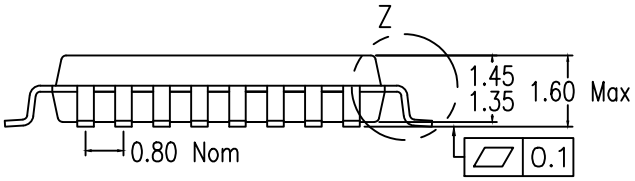
DIMENSIONS IN MILLIMETERS

BASED ON JEDEC JEP95:MO-136 BC

1. DIMENSIONS







2. WEIGHT ≤ 0.2 g
3. BODY MATERIAL LOW STRESS EPOXY
4. LEAD MATERIAL FeNi-ALLOY or Cu-ALLOY
5. LEAD FINISH SOLDER PLATING
6. LEAD FORM Z-BENDS

Package Revision History		
Date Created	Rev No.	Description
Jan. 22, 2020	01	New Format
Feb 2, 2016	00	Initial release