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PRELIMINARY

PSoC® 4: CY8C4045XXX-DS400 Datasheet

Programmable System-on-Chip (PSoC)

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an ARM® Cortex™-M0 CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing.

The PSoC CY8C4045XXX-DS400 product family is a member of the PSoC 4 platform architecture family. It provides a compact (1.6 mm × 2 mm) 32-bit microcontroller solution in a 20-ball WLCSP package.

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU
- 32-KB Flash
- 4-KB SRAM

Low-Power Operation

- 1.7-V to 5.5-V operation
- Independent supply voltage pin for GPIO that allows 1.71-V to 5.5-V signaling on the I/Os
- Deep Sleep current of 2.5 µA

Clock Sources

- ±2 % Internal Main Oscillator (IMO)
- Internal Low-power Oscillator (ILO)

Timing and Pulse-Width Modulation

- Six 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Quadrature decoder
- Comparator-based triggering of Kill signals for motors

Serial Communication

- Two independent run-time reconfigurable Serial Communication Blocks (SCBs) with re-configurable I^2C, SPI, or UART functionality

Package

- 1.63 mm × 2.03 mm, 20-ball wafer-level CSP (WLCSP) with 0.4-mm ball pitch
- Up to nine GPIO pins
- Supports industrial (–40 °C to +85 °C) temperature range

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
  - AN85951: PSoC 4 and PSoC Analog Coprocessor Capsense Design Guide
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

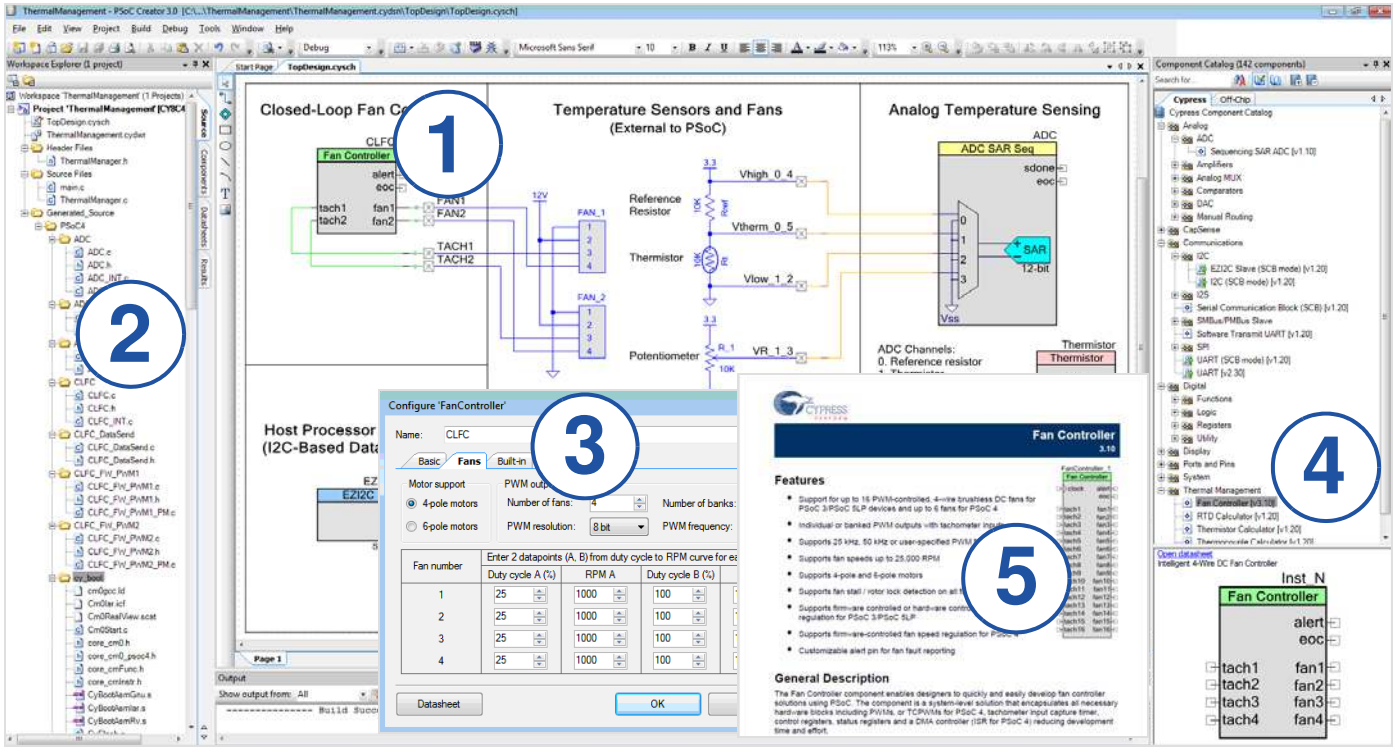
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

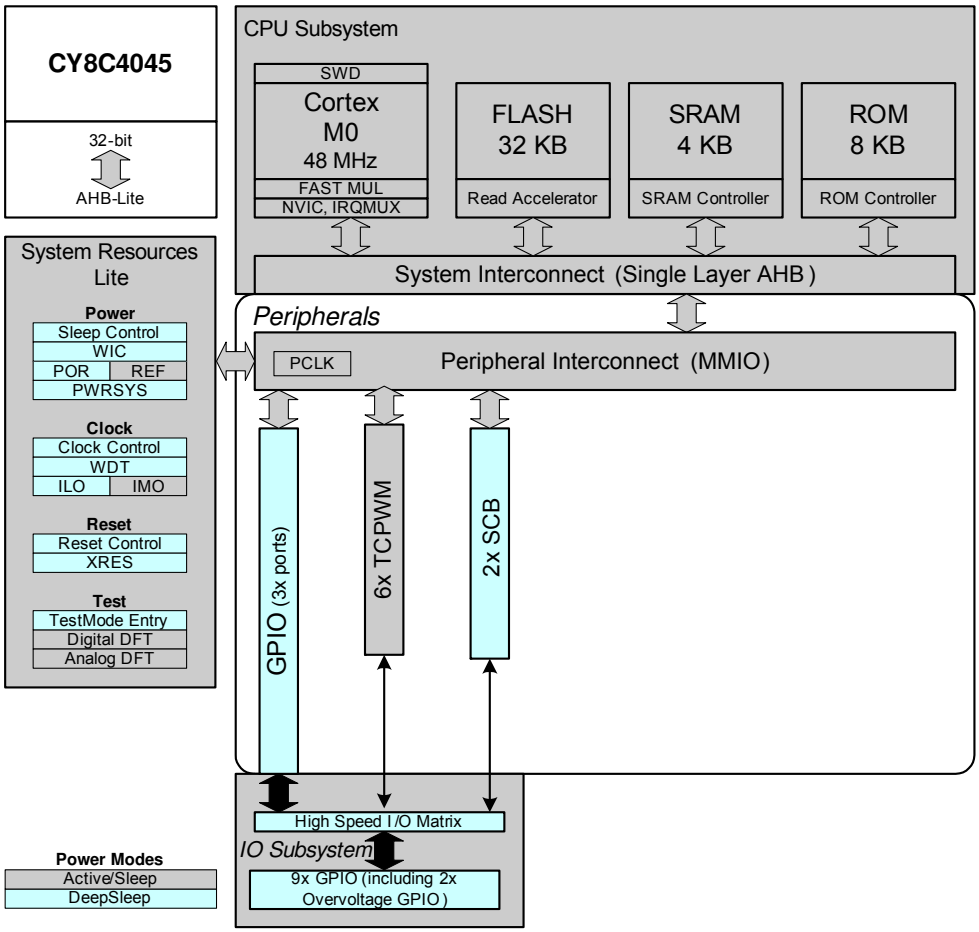
1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Contents

Figure 2. CY8C4045XXX-DS400 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in CY8C4045XXX-DS400 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for CY8C4045XXX-DS400 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The CY8C4045XXX-DS400 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

4 KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

An 8-KB supervisory ROM that contains boot and configuration

System Resources

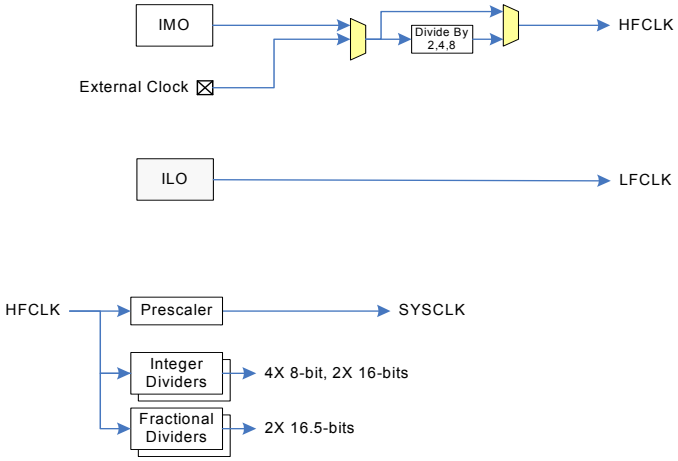
Power System

The power system is described in detail in the section Power on page 8. It provides assurance that voltage levels are as required for each respective mode and will delay active mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper functionality or generate reset (Brown-Out Detect (BOD)). CY8C4045XXX-DS400 can operate over the range of 1.7 to 5.5 V and has three different power modes (Active, Sleep, and Deep Sleep) transitions between which are managed by the power system.

Clock System

The clock system for CY8C4045XXX-DS400 consists of the Internal Main Oscillator (IMO) and the Internal Low-power Oscillator (ILO). The IMO operates over a range of 24 to 48 MHz. There are eight clock dividers that generate peripheral clocks by dividing the IMO clock: four 8-bit dividers, two 16-bit dividers, and two fractional (16.5) dividers.

Figure 3. MCU Clocking Architecture



Peripherals

Serial Communication Blocks (SCB)

CY8C4045XXX-DS400 has two SCBs (SCB[0] and SCB[1]), which can be configured to implement an I^{2}C, SPI, or UART interface. The hardware I^{2}C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^{2}C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^{2}C that creates a mailbox address range in the memory of CY8C4045XXX-DS400 and effectively reduces I^{2}C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^{2}C peripherals are compatible with the I^{2}C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^{2}C-bus specification and user manual (UM10204). The I^{2}C bus I/Os are implemented with GPIO in open-drain modes. The I^{2}C signals of SCB[0] can be connected to Port pins P0.0 and P0.1 which are overvoltage-tolerant.

Non-overvoltage tolerant pins (all except P0.0 and P0.1) are not completely compliant with the I^{2}C spec in the following respects:

- They cannot be hot-swapped or powered up independently of the rest of the I^{2}C system.
- Fast-mode Plus has an IOL specification of 20 mA at a VOL of 0.4 V. The GPIO cells can sink a maximum of 8-mA IOL with a VOL maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode

Timer/Counter/PWM Block (TCPWM)

CY8C4045XXX-DS400 has six TCPWM blocks, each of which implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals

GPIO

CY8C4045XXX-DS400 has up to nine GPIOs including the SWD pins, which can also be used as GPIOs if not being used for Debug and programming purposes. Pins P0.0 and P0.1 are overvoltage-tolerant. The number of available GPIOs vary with the package. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
  - Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

The following table provides the pin list for the 20-ball CSP. Pins Px.y are GPIO pins with multiple functions, "x" indicates the port number and "y" the particular pin on that port. Note that XRES has no internal pullup and, if a pullup is required, an external pullup of typically 5 KΩ is recommended. Port pin functionality is described in the next table.

Ball Location (20-CSP)	Description
B4	DNC (Do Not Connect). Leave floating.
A4	DNC (Do Not Connect). Leave floating.
B3	DNC (Do Not Connect). Leave floating.
C3	P2.1
D3	P1.7
C2	P1.3
D2	P1.0
B2	P1.5
A3	P0.1 (Overvoltage Tolerant)
A2	P0.0 (Overvoltage Tolerant)
E2	P1.1 (SWD DATA)
D1	P1.2 (SWD CLK)
B1	XRES (Reset input)
E4	DNC (Do Not Connect). Leave floating.
C4	DNC (Do Not Connect). Leave floating.
E1	VDDIO (1.71 V to 5.5 V power supply for GPIO)
A1	VCCD (Internal Regulator output to bypass Cap.)
E3	VDDD (1.71 V to 5.5 V chip power supply)
D4	VSS (Ground)
C1	VSS (Ground)

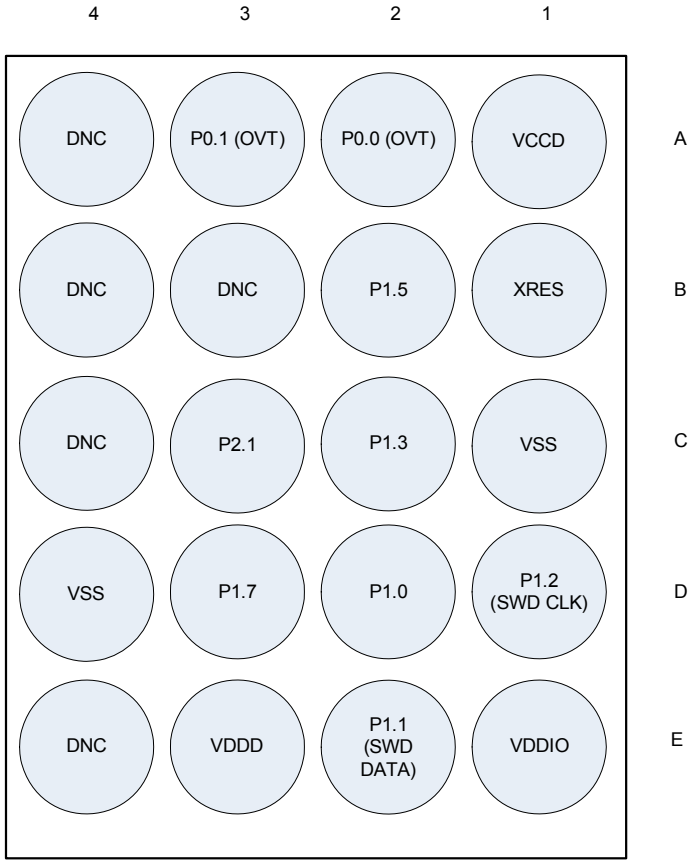
Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions. The pin assignments are shown in the following table.

Port Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #0	DS #1	DS #2	DS #3
P1.0	tcpwm.line[0]	tcpwm.tr_compare_match[0]	scb[1].uart_tx	tcpwm.tr_overflow[0]		-	scb[1].spi_clk	scb[1].i2c_scl
P1.1	tcpwm.line[1]	tcpwm.tr_compare_match[1]	scb[1].uart_cts	tcpwm.tr_overflow[1]	swd_data	-	scb[1].spi_mosi	-
P1.2	tcpwm.line[2]	tcpwm.tr_compare_match[2]	-	tcpwm.tr_overflow[2]	swd_clk		-	-
P1.3	ext_clk:0	-	scb[1].uart_rx	-	-		scb[1].spi_miso	scb[1].i2c_sda
P1.5	tcpwm.line[3]	tcpwm.tr_compare_match[3]	scb[1].uart_rts	tcpwm.tr_overflow[3]			scb[1].spi_select0	-
P1.7	tcpwm.line[4]	tcpwm.tr_compare_match[4]	scb[0].uart_tx	tcpwm.tr_overflow[4]		scb[0].spi_mosi	-	
P0.0	ext_clk:1	-	scb[0].uart_cts	-		scb[0].spi_select0:0	-	scb[0].i2c_sda:0
P0.1	-	-	scb[0].uart_rts	-		scb[0].spi_miso:0	-	scb[0].i2c_scl:0
P2.1	tcpwm.line[5]	tcpwm.tr_compare_match[5]	scb[0].uart_rx	tcpwm.tr_overflow[5]		scb[0].spi_clk	-	

Port pins P0.0 and P0.1 are overvoltage-tolerant (OVT). ACT and DS in the table above refer to Active and Deep Sleep modes respectively.

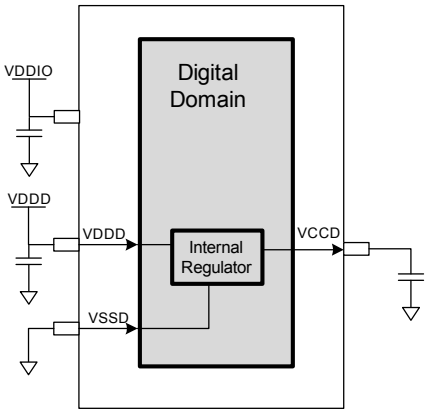
Figure 4. 20-ball WLCSP CY8C4045XXX-DS400 Ball Map (Bottom (Balls Up) View)



Power

The following power system diagram shows the set of power supply pins as implemented in CY8C4045XXX-DS400. A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 to 5.5 V. The VDDIO pin must be equal to or less than the voltages connected to the VDDD pin. VDDIO and VDDD can be shorted together if separate levels are not required.

Figure 5. Power Supply Connections

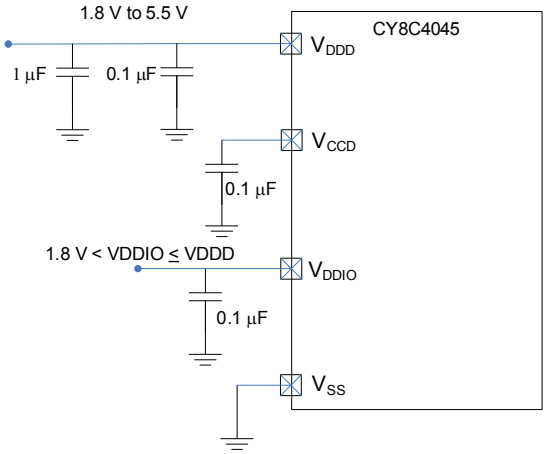


Mode 1: 1.8 V to 5.5 V External Supply

In this mode, the CY8C4045XXX-DS400 is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the CY8C4045XXX-DS400 supplies the internal logic and its output is connected to the VCCD pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else. An example of a Bypass scheme is shown in Figure 6.

Figure 6. CY8C4045XXX-DS400 Power and Bypass Scheme Example (1.8 V to 5.5 V)

Power supply connections when $1.8 \leq V_{DDD} \leq 5.5$ V



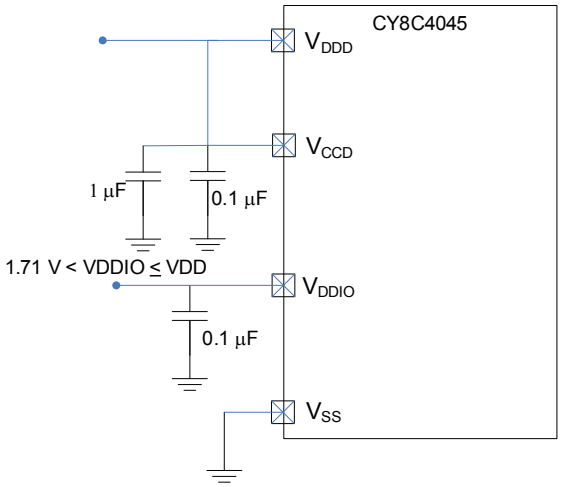
Mode 2: 1.8 V ±5% External Supply

In this mode, the CY8C4045XXX-DS400 is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple voltage. In this mode, the VDDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in Figure 7.

Figure 7. CY8C4045XXX-DS400 Power and Bypass Scheme Example (1.71 V to 1.89 V)

Power supply connections when $1.71 \leq V_{DDD} \leq 1.89$ V



Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	Absolute max
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5	V	Absolute max
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	Absolute max
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Typical values are measured at 25 °C unless otherwise noted.

Table 2. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	1.71	–	5.5	V	
SID.PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5	V	VDDIO voltage must be less than or equal to VDDD
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	Internal regulator output
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	–	0.1	–	µF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DDD} = 1.71 to 5.5 V. Typical values measured at V_{DD} = 3.3 V							
SID.PWR#12	I_{DD12}	Supply current	–	4	–	mA	CPU at 12 MHz. IMO at 48 MHz.
SID.PWR#12A	I_{DD12A}	Supply current	–	8	–	mA	CPU at 24 MHz. IMO at 48 MHz.
SID.PWR#12B	I_{DD12B}	Supply current	–	13	–	mA	CPU at 48 MHz. IMO at 48 MHz.
Sleep Mode, V_{DDD} = 1.71 to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup. WDT ON. IMO at 48 MHz	–	2.0	3.0	mA	CPU at 12 MHz
Deep Sleep Mode, V_{DDD} = 1.71 to 5.5 V							
SID_DS	I_{DD_DS}	I2C Wakeup and WDT on.	–	2.5	–	µA	V_{DDD} = 1.8 to 5.5 V
SID_DS_1	$I_{DD\_DS\_1}$	Internal Regulator bypassed. I^2C Wakeup and WDT on.	–	2.5	–	µA	V_{DDD} = 1.71 to 1.89 V
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 3. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V ≤ V_{DDD} ≤ 5.5 V
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	24-MHz IMO. Guaranteed by characterization
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	Guaranteed by characterization

I/O

Table 4. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH}[2]	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	V_{IH}[2]	LVTTL input, V_{DDIO} < 2.7 V	0.7× V_{DDIO}	–	–	V	–
SID.GIO#40	V_{IL}	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	V_{IH}[2]	LVTTL input, $V_{DDIO} \geq$ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V_{IL}	LVTTL input, $V_{DDIO} \geq$ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDIO}
SID.GIO#5	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#6	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDIO} = 3.0 V. Guaranteed by characterization
SID.GIO#17	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDIO} \geq$ 2.7 V. Guaranteed by characterization.
SID.GPIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDIO}	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DDIO}/V_{SS}	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	Guaranteed by characterization

Table 5. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF

Note
2. V_{IH} must not exceed V_{DDIO} + 0.2 V.

XRES

Table 6. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	0.05 × V_{DDIO}	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 7. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	Fc	–	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	2/Fc	–	ns	For all Trigger Events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	2/Fc	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	1/Fc	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	1/Fc	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	1/Fc	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 8. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kbps	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kbps	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 9. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

UART

Table 10. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	125	µA	Guaranteed by characterization
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	Guaranteed by characterization

Table 11. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	Guaranteed by characterization

SPI

Table 12. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	Guaranteed by characterization
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	Guaranteed by characterization
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	Guaranteed by characterization

Table 13. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	Guaranteed by characterization

Table 14. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	Guaranteed by characterization
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling. Guaranteed by characterization
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge. Guaranteed by characterization

Table 15. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock Capturing edge	40	–	–	ns	Guaranteed by characterization
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	42 + 3 * T_{CPU}	ns	TCPU = 1/FCPU. Guaranteed by characterization.
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	Guaranteed by characterization
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	Guaranteed by characterization
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	Guaranteed by characterization

Memory

Table 16. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#4	$T_{ROWWRITE}$[3]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID.MEM#3	$T_{ROWERASE}$[3]	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$[3]	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$[3]	Bulk erase time (32 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$[3]	Total device program time	–	–	7.5	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET1}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization

Note

3. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Power-on-Reset (POR) with Brown Out

Table 17. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization

Table 18. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5	V	Guaranteed by characterization

SWD Interface

Table 19. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \le V_{DDIO} \le 5.5\ V$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\ V \le V_{DDIO} \le 3.3\ V$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 20. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO}	IMO operating current at 48 MHz	–	–	250	µA	–

Table 21. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	Guaranteed by characterization
F_{IMO}	–	IMO frequency	24	–	48	MHz	–

Internal Low-Speed Oscillator

Table 22. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 23. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	ILO Frequency	20	40	80	kHz	–

Ordering Information

The CY8C4045XXX-DS400 part numbers and features are listed in the following table.

MPN	Features						Packages
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	TCPWM Blocks	SCB Blocks	GPIO	
CY8C4045FNI-DS400	48	32	4	6	2	9	20-pin WLCSP

Packaging

Table 24. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	°C
T_J	Operating junction temperature	Industrial	–40	–	100	°C
		Extended Industrial			125	°C
T_{JA}	Package θ_{JA} (20-ball WLCSP)	–	–	66	–	°C/W
T_{JC}	Package θ_{JC} (20-ball WLCSP)	–	–	0.7	–	°C/W

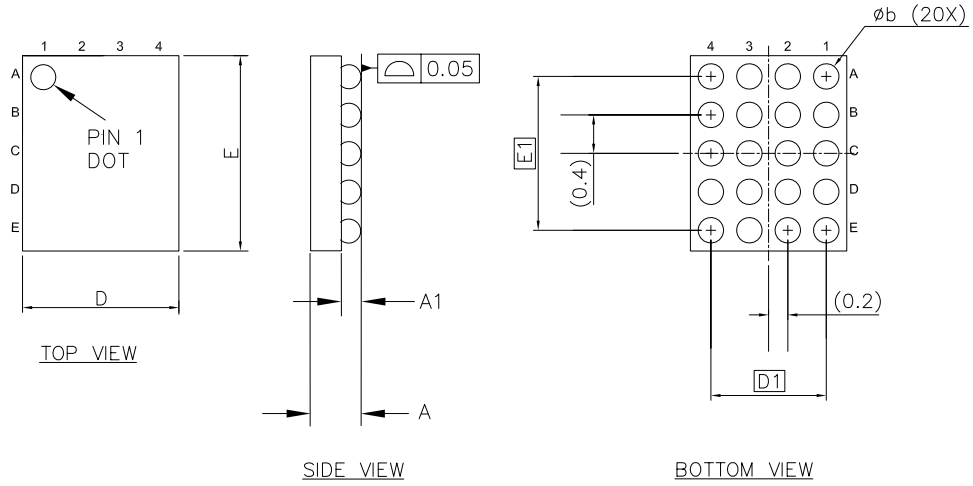
Table 25. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
20-ball WLCSP	260 °C	30 seconds

Table 26. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
20-ball WLCSP	MSL 1

Figure 8. 20-ball WLCSP (1.63 × 2.03 × 0.55 mm) FN20B Package Outline, 001-95010



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.55
A1	0.18	0.21	0.24
D	1.605	1.63	1.655
E	2.005	2.03	2.055
D1		1.2 BSC	
E1		1.6 BSC	
n		20	
Øb	0.23	0.26	0.29

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18

001-95010 *B

Acronyms

Table 27. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG2	Cable Controller Generation 2
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DFT	design for testability
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt

Table 27. Acronyms Used in this Document *(continued)*

Acronym	Description
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 28. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Description Title: PSoC® 4: CY8C4045XXX-DS400 Datasheet Programmable System-on-Chip (PSoC) Document Number: 002-20919				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5865280	WKA	12/18/2017	New datasheet.

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