ANALOG DEVICES

High Speed 64-Bit IEEE Floating-Point Multiplier

ADSP-3211

1.1 Scope.

This specification covers the detail requirements for a CMOS monolithic 32-bit and 64-bit IEEE Standard 754 format floating-point multiplier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-3211SG/883B
−2	ADSP-3211TG/883B
−3	ADSP-3211UG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-144A.

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3 V to 7 V
Input Voltage	−0.3 V to V_{DD}
Output Voltage	−0.3 V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

ADSP-3211 – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2, 3	2.0	2.0	2.0			V_{DD} = max	V min
Digital Input High Voltage, CLK and Asynchronous Controls RESET, MSWSEL, OEN	V_{IHA}	−1, 2, 3	3.0	3.0	3.0			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2, 3	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2, 3	2.4	2.4	2.4			V_{DD} = min I_{OH} = −1 mA	V min
Digital Output Low Voltage	V_{OL}	−1, 2, 3	0.4	0.6	0.6			V_{DD} = min I_{OH} = +4 mA	V max
Digital Input High Current	I_{IH}	−1, 2, 3	10	10	10			V_{DD} = max V_{IN} = +5.0 V	µA max
Digital Input Low Current	I_{IL}	−1, 2, 3	10	10	10			V_{DD} = max V_{IN} = 0.0 V	µA max
Three-State Leakage Current	I_{OZ}	−1, 2, 3	50	50	50			V_{DD} = max High Z, V_{IN} = 0 V or max	µA max
Supply Current	I_{DD1}	−1, 2, 3	150	200	200			@ max Clock Rate, TTL Inputs	mA max
	I_{DD2}		50	60	60			All V_{IN} = 2.4 V	mA max
Clock Cycle	t_{CY}	−1	125			150	150	Note 2	ns max
		−2	100			125	125		
		−3	60			75	75		
Clock LO	t_{CL}	−1, 2, 3	20			30	30	Note 2	ns min
Clock HI	t_{CH}	−1, 2, 3	20			30	30	Note 2	ns min
Data & Control Setup	t_{DS}	−1	20			25	25	Note 2	ns min
		−2, 3	15			20	20		
Data & Control Hold	t_{DH}	−1, 2, 3	3			3	3	Note 2	ns min
Data Output Delay	t_{DO}	−1	30			35	35	Note 2	ns max
		−2, 3	25			30	30		
Status Output Delay	t_{SO}	−1	30			35	35	Note 2	ns max
		−2, 3	25			30	30		
MSWSEL-to-Data Delay	t_{ENO}	−1	25			30	30	Note 2	ns max
		−2, 3	20			25	25		
Three-State Disable Delay	t_{DIS}	−1	18			25	25	Notes 2 & 3	ns max
		−2, 3	15			20	20		
Three-State Enable Delay	t_{ENA}	−1	25			30	30	Notes 2, 3 & 5	ns max
		−2, 3	20			25	25		
RESET Setup	t_{SU}	−1	20			25	25	Note 2	ns min
		−2, 3	15			25	25		
RESET Pulse Duration	t_{RS}	−1, 2, 3	50			75	75	Note 2	ns min

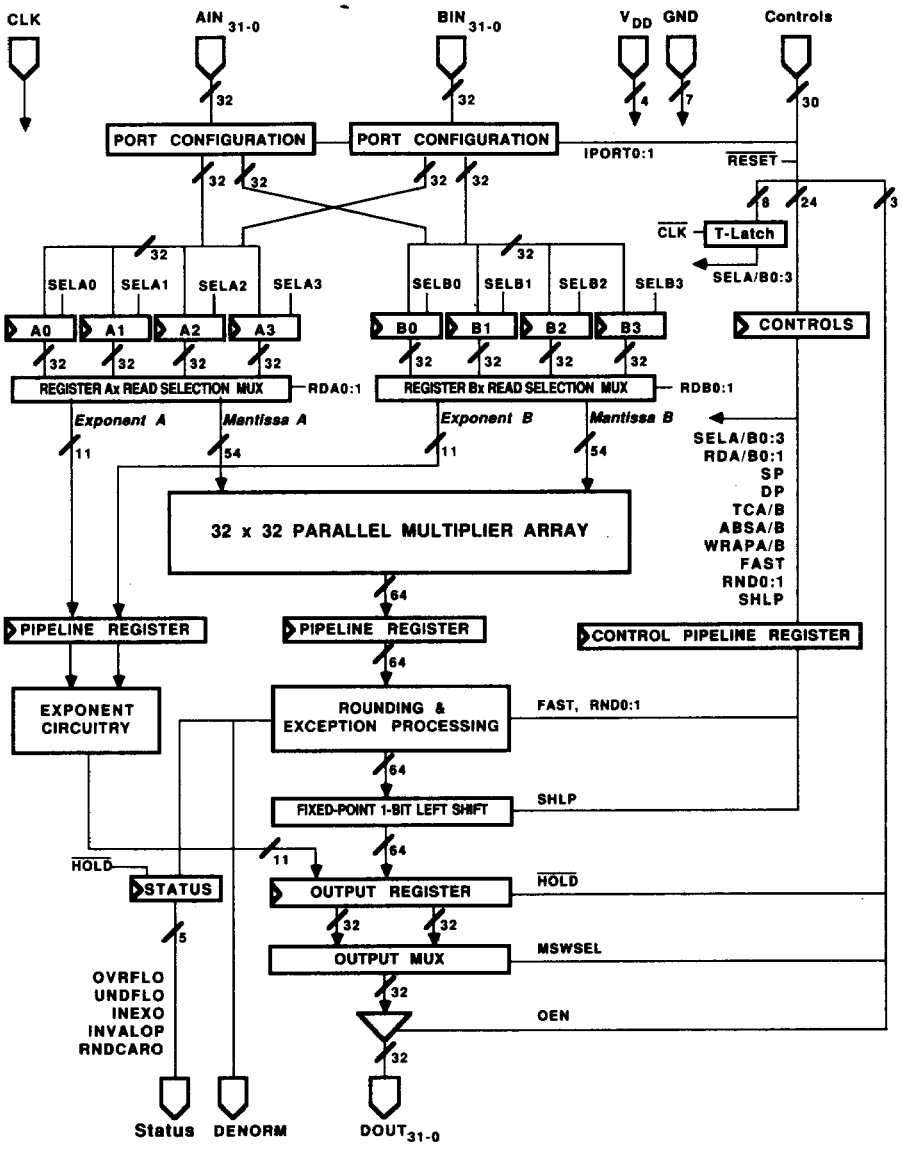
Table 1. (Continued on next page)

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Operation Time (With or Without Direct Operand Feed):	t_{OPD}							Note 2	ns max
32-Bit Multiplication		−1	125			150	150		
		−2	100			125	125		
		−3	60			70	70		
64-Bit Multiplication		−1	500			600	600	Note 2	ns max
		−2	400			500	500		
		−3	240			280	280		
Hold Setup	t_{HS}	−1	20			22	22	Note 2	ns min
		−2	15			18	18		
		−3	15			20	20		
Hold Hold	t_{HH}	−1, 2, 3	3			3	3	Note 2	ns min
Total Latency[4] (With Direct Operand Feed):	t_{LAD}							Note 2	ns max
32-Bit Multiplication		−1	300			360	360		
		−2	240			300	300		
		−3	140			190	190		
64-Bit Multiplication		−1	738			885	885	Note 2	ns max
		−2	590			738	738		
		−3	315			400	400		

NOTES
[1]T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).
[2]Input levels are GND and +3.0 V; V_{DD} = +4.5 V, and timing transitions, per Figures 1 through 7, measured at +1.5 V.
[3]Transitions measured per Figure 1.
[4]Total latency = (data setup + processing + output delay of MSW) in Direct Operand Feed Mode.
[5]3 ns minimum.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

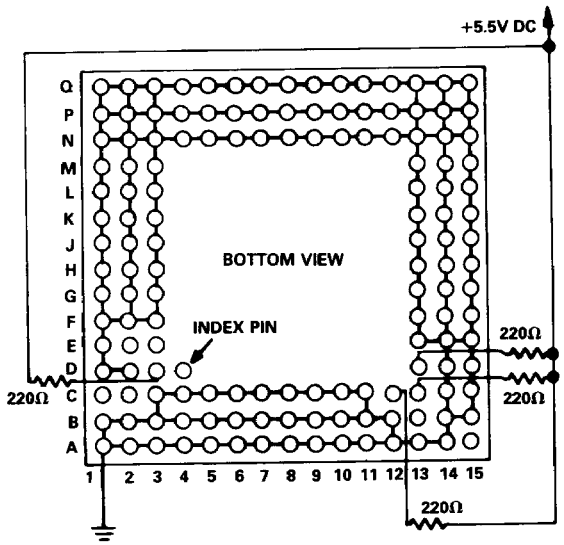
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A1	DOUT31	P5	AIN11	G13	RDB1
A2	DOUT27	N5	AIN13	F15	WRAPB
A3	DOUT23	Q6	AIN4	F14	CLK
B1	GND	P6	AIN8	F13	GND
B2	DOUT30	N6	AIN9	E15	SP
B3	DOUT26	Q7	AIN3	E14	DP
C1	OVRFLO	P7	AIN6	E13	GND
C2	DENORM	N7	AIN5	D15	RND1
C3	DOUT29	Q8	AIN1	D14	$\overline{\text{RESET}}$
D1	TCA	P8	AIN2	D13	V_{DD}
D2	GND	N8	AIN0	C15	RND0
D3	V_{DD}	Q9	BIN30	C14	GND
E1	SHLP	P9	BIN28	C13	V_{DD}
E2	UNDFLO	N9	BIN31	B15	$\overline{\text{TCB}}$
E3	INVALOP	Q10	BIN29	B14	$\overline{\text{HOLD}}$
F1	ABSA	P10	BIN27	B13	INEXO
F2	MSWSEL	N10	BIN26	A15	RNDCARO
F3	OEN	Q11	BIN25	A14	DOUT0
G1	RDA0	P11	BIN24	A13	DOUT3
G2	FAST	N11	BIN20	A12	DOUT5
G3	WRAPA	Q12	BIN23	B12	DOUT1
H1	SELA0	P12	BIN21	C12	V_{DD}
H2	RDA1	N12	BIN17	A11	DOUT8
H3	SELA2	Q13	BIN22	B11	DOUT4
J1	SELA3	P13	BIN19	C11	DOUT2
J2	IPORT1	N13	BIN16	A10	DOUT11
J3	SELA1	Q14	BIN18	B10	DOUT7
K1	IPORT0	P14	BIN15	C10	DOUT6
K2	AIN31	N14	BIN12	A9	DOUT12
K3	AIN30	Q15	BIN14	B9	DOUT9
L1	AIN29	P15	BIN11	C9	DOUT10
L2	AIN28	N15	BIN8	A8	DOUT14
L3	AIN24	M15	BIN6	B8	DOUT13
M1	AIN27	M14	BIN10	C8	GND
M2	AIN25	M13	BIN13	A7	DOUT15
M3	AIN21	L15	BIN3	B7	DOUT17
N1	AIN26	L14	BIN7	C7	GND
N2	AIN23	L13	BIN9	A6	DOUT16
N3	AIN20	K15	BIN0	B6	DOUT18
P1	AIN22	K14	BIN4	C6	DOUT19
P2	AIN19	K13	BIN5	A5	DOUT20
P3	AIN16	J15	SELB3	B5	DOUT21
Q1	AIN18	J14	BIN2	C5	DOUT25
Q2	AIN15	J13	BIN1	A4	DOUT22
Q3	AIN12	H15	SELB2	B4	DOUT24
Q4	AIN10	H14	SELB1	C4	DOUT26
P4	AIN14	H13	SELB0	D4	INDEX
N4	AIN17	G15	RDB0		
Q5	AIN7	G14	ABSB		

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



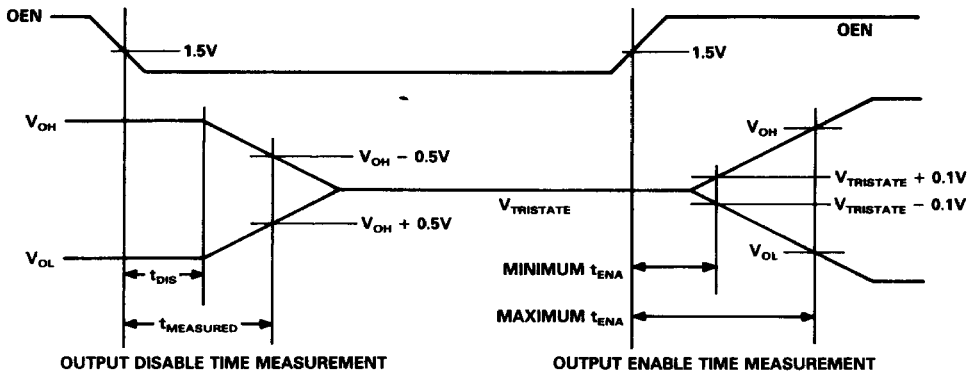


Figure 1. ADSP-3211 Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The minimum output enable time, minimum t_{ENA}, is the earlist that outputs begin to drive. It is measured from the control signal OEN reaching 1.5 V to the point at which the fastest outputs have changed by 0.1 V from $V_{TRISTATE}$ toward their final output voltages. Minimum enable times are shortest at the lowest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

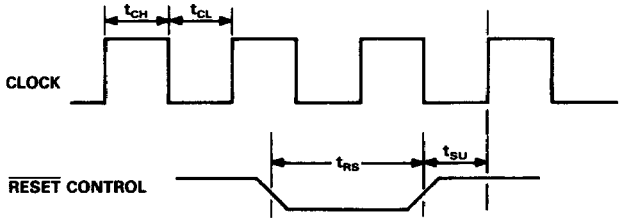


Figure 2. ADSP-3211 Reset Timing

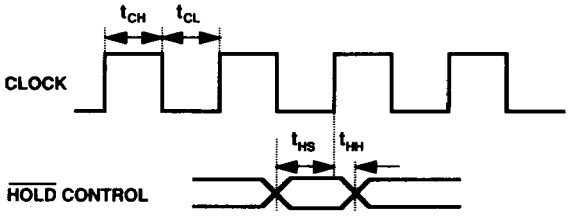


Figure 3. ADSP-3211 Multiplier Output Register Hold Timing

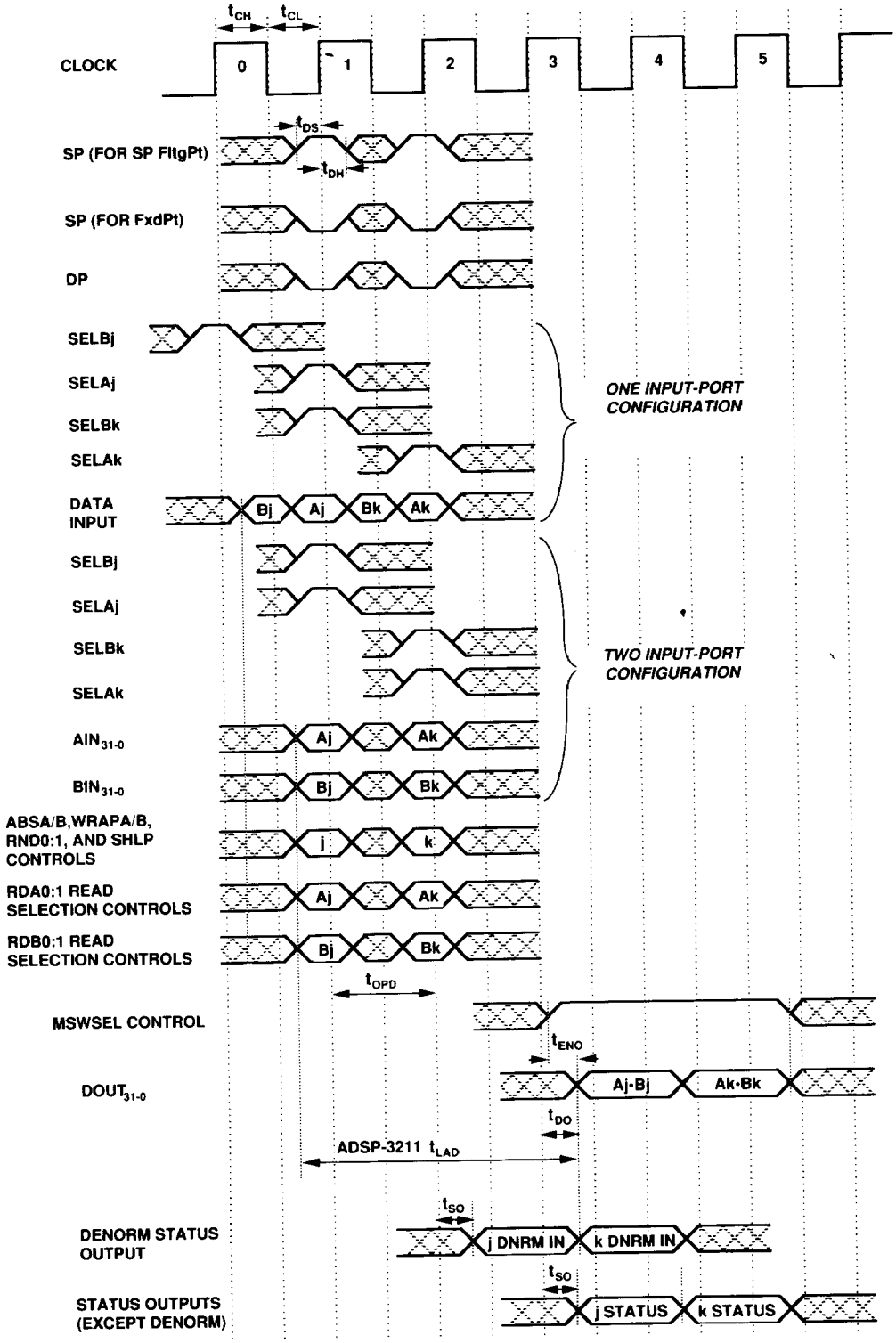


Figure 4. ADSP-3211 32-Bit Single-Precision Floating-Point and Fixed-Point Multiplications

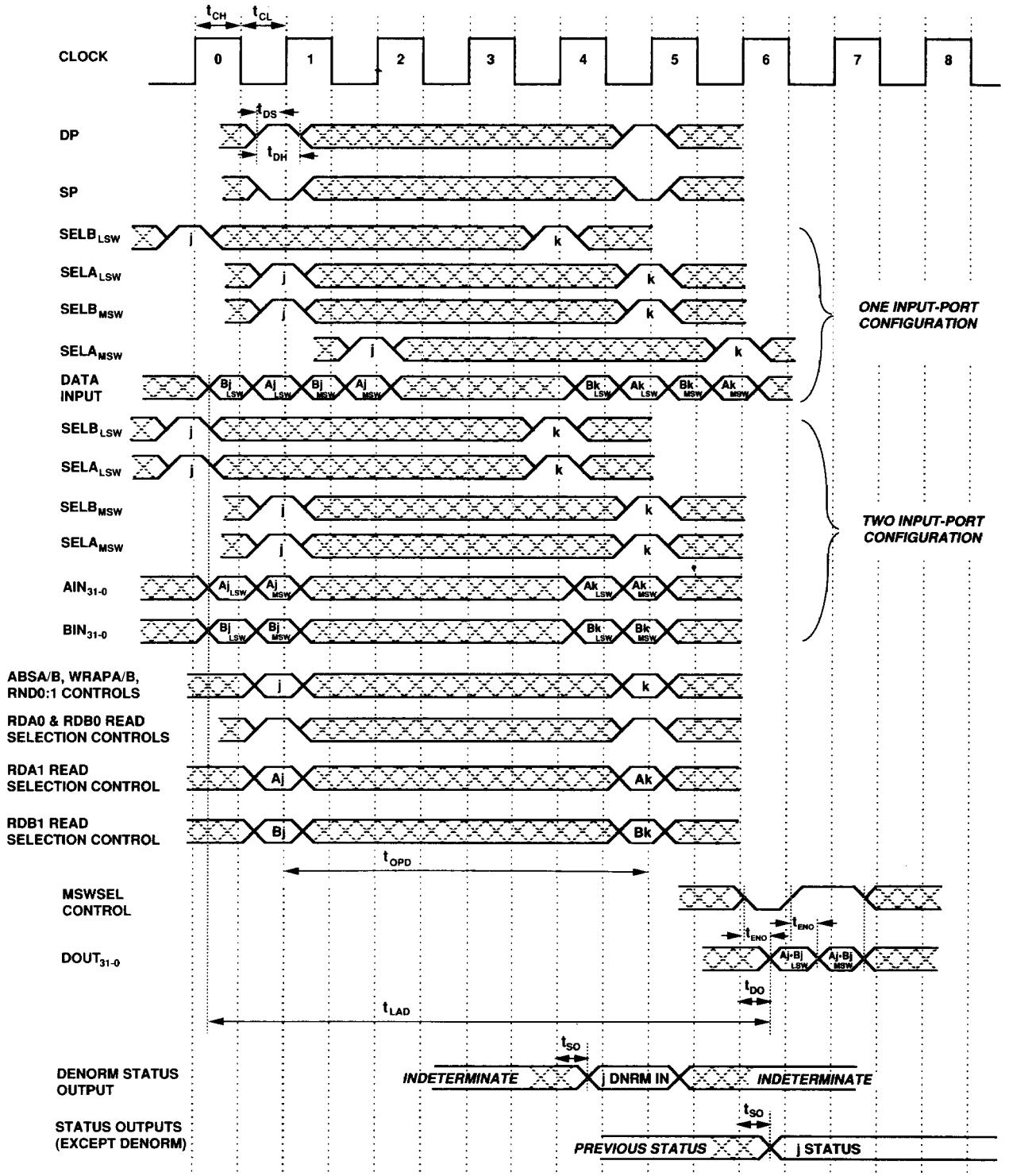


Figure 5. ADSP-3211 64-Bit Double-Precision Floating-Point Multiplications

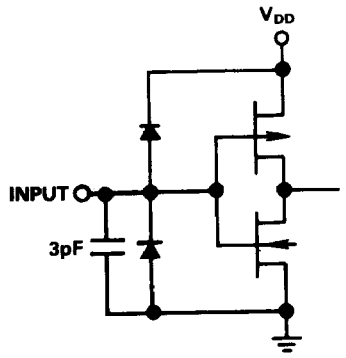


Figure 6. Equivalent Input Circuits

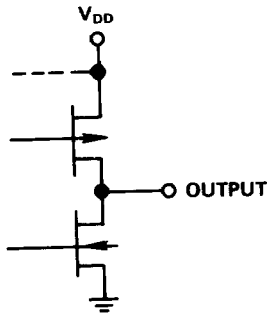


Figure 7. Equivalent Output Circuits

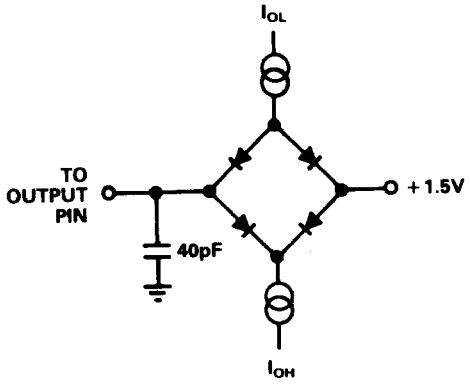


Figure 8. Normal Load for AC Measurements

INSTRUCTION	WRAPA	WRAPB	COMMENT
A*B	0	0	Multiply Normalized Floating Point Operands A times B.
WA*B	1	0	Multiply Wrapped Operand A Times Operand B.
A*WB	0	1	Multiply Operand A Times Wrapped Operand B.
WA*WB	1	1	Multiply Wrapped Operand A Times Wrapped Operand B.

Table 2. ADSP-3211 Instruction Set

5.0 Notation Used in the Tables Below:

RN	=	Round to the Nearest Number
RP	=	Round toward Plus Infinity
RM	=	Round toward Minus Infinity
RZ	=	Round toward Zero
NORM	=	Normalized Number
DNRM	=	Denormalized Number. A Denormalized Number Is Treated as Zero Internally.
WNRM	=	Wrapped Number. A Wrapped Number Is a Number with a Normalized Fraction and an Exponent that Has Been Decremented through Zero to Take on a Twos Complement Negative Value.
UNRM	=	Unnormalized Number. An Unnormal Is an Underflowed and Wrapped Number. An UNRM Can Result from a Multiplication of 1 or 2 Wrapped Numbers.
NORM.MAX	=	Maximum Normalized Number Representable in the Destination Format
NORM.MIN	=	Minimum Normalized Number Representable in the Destination Format
OVF	=	Overflowed Number
UNDF	=	Underflowed Number
INV	=	Invalid Operand
INF	=	Infinity
OK	=	No Exception Status Generated

In the tables below, the first mnemonic in each box describes the flag that is set, the second is the result on the DOUT pins.

A operand \ B operand	ZERO		DNRM		WRAP		NORM		INF		NAN	
	result	*status*	*result*	*status*	*result*	*status*	*result*	*status*	*result*	*status*	*result*	*status*
ZERO	ZERO		ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	ZERO	DENORM	INF		NAN	INVALOP
WRAP	ZERO		ZERO	DENORM	UNRM	UNDFLO	NORM WRAP UNRM	 UNDFLO UNDFLO	INF		NAN	INVALOP
NORM	ZERO		ZERO	DENORM	NORM WRAP UNRM	 UNDFLO UNDFLO	INF,NORM.MAX [1] NORM WRAP	OVRFLO UNDFLO	INF		NAN	INVALOP
INF	NAN	INVALOP	INF		INF		INF		INF		NAN	INVALOP
NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode.

Table 3. ADSP-3211 Floating-Point Multiplication (IEEE Mode)

A operand \ B operand	ZERO		DNRM		NORM		INF		NAN	
	result	*status*	*result*	*status*	*result*	*status*	*result*	*status*	*result*	*status*
ZERO	ZERO		ZERO		ZERO		NAN	INVALOP	NAN	INVALOP
DNRM	ZERO		ZERO	DENORM	ZERO	DENORM	NAN	INVALOP	NAN	INVALOP
NORM	ZERO		ZERO	DENORM	INF,NORM.MAX [1] NORM ZERO	OVRFLO UNDFLO	INF		NAN	INVALOP
INF	NAN	INVALOP	INF	INVALOP	INF		INF		NAN	INVALOP
NAN	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP	NAN	INVALOP

1. Either INF or NORM.MAX, depending on rounding mode. See "Round Controls."
2. In FAST mode, WRAP inputs are illegal.

Table 4. ADSP-3211 Floating-Point Multiplication (FAST Mode)